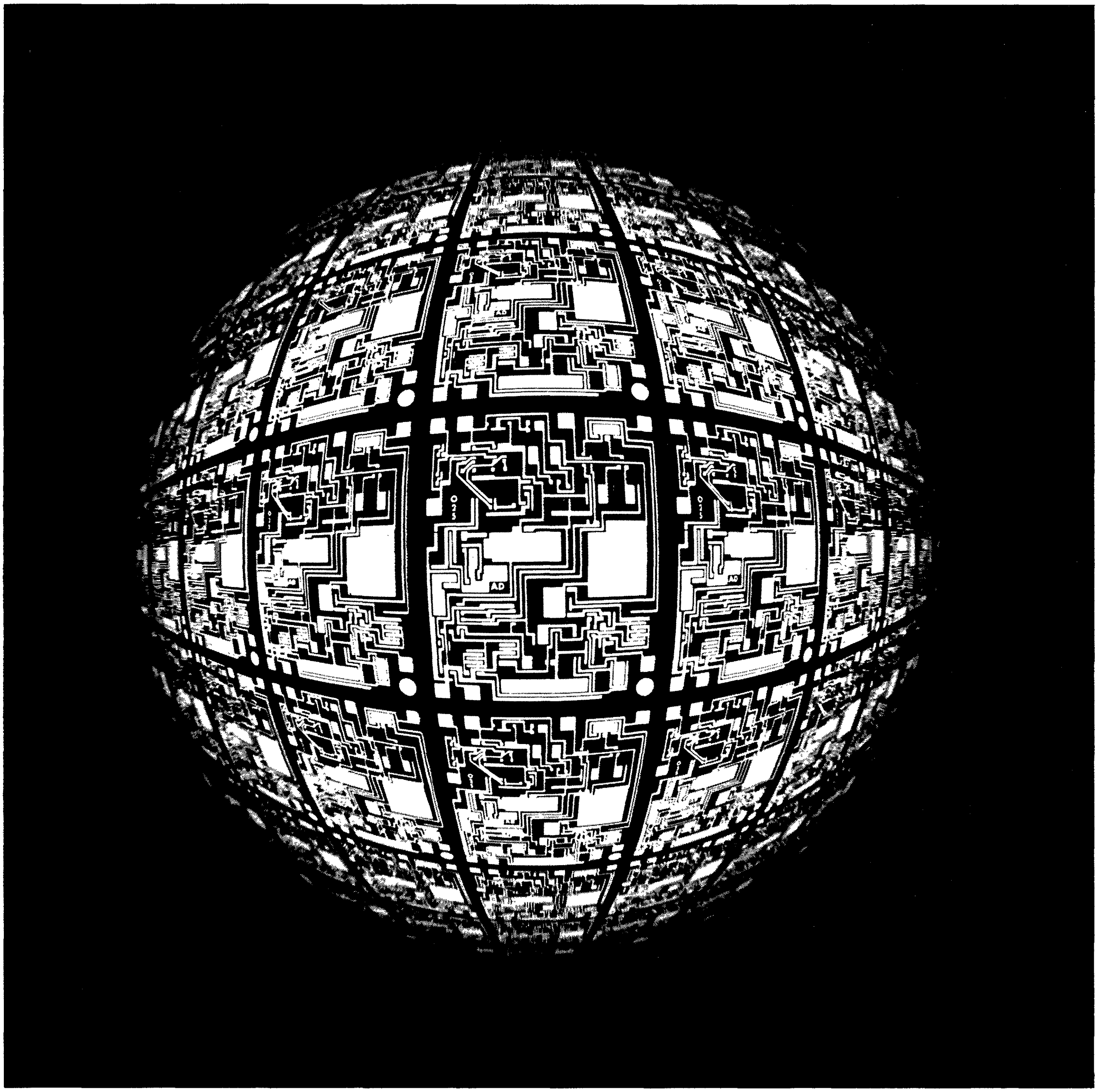
National Semiconductor Corporation

LINEAR APPLICATIONS



NATIONAL LINEAR APPLICATIONS HANDBOOK

January 1972

PREFACE

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index composed of approximately 1000 references to the main body of the text. This Subject Index provides the key to efficient access to the applications experience accumulated over the last five years by National Semiconductor.

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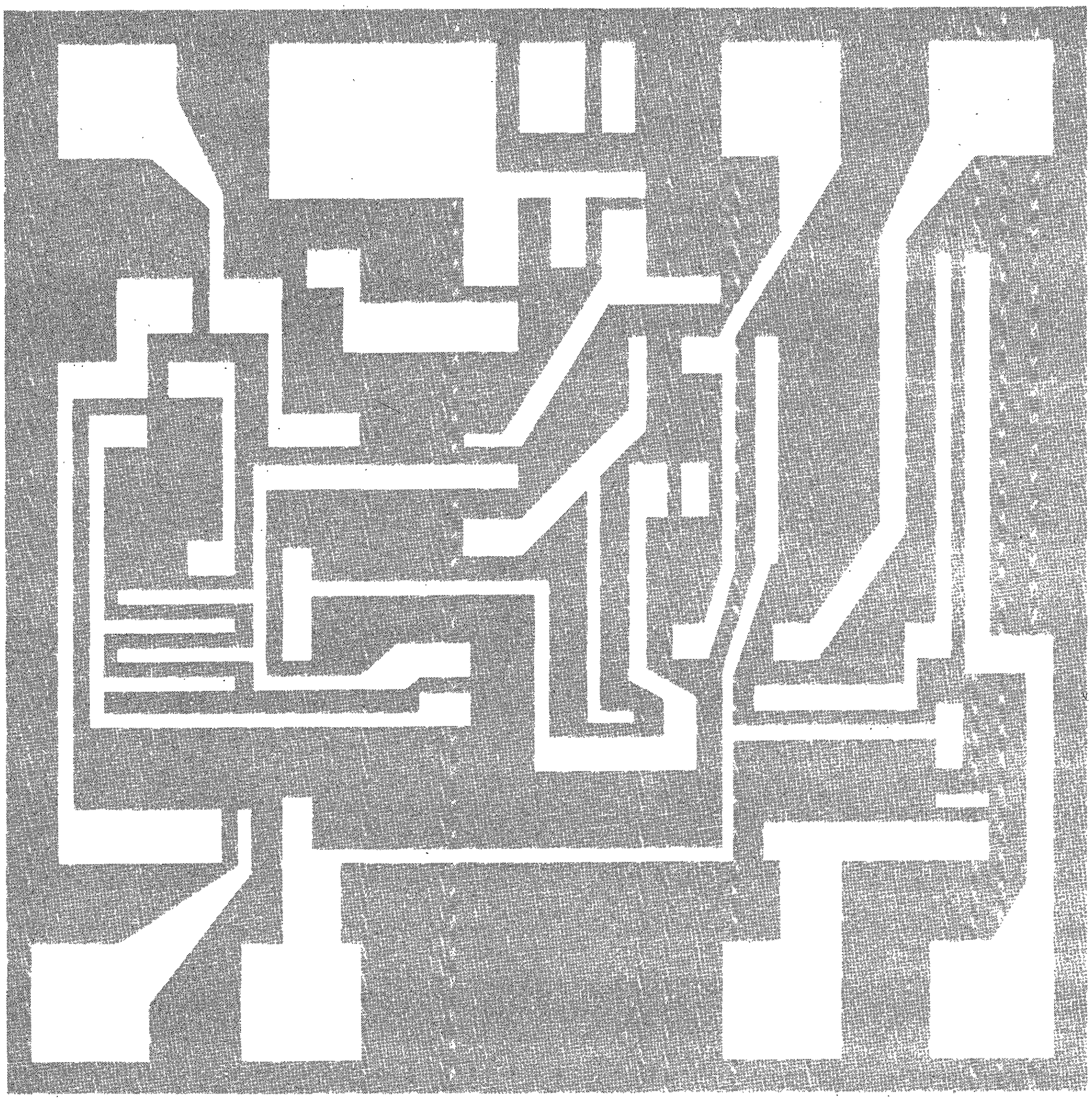
November 1967

A VERSATILE, MONOLITHIC VOLTAGE REGULATOR



INTRODUCTION

The great majority of linear integrated circuits being produced today are DC amplifiers, particularly operational amplifiers. This has come about both because the DC operational amplifier is a basic analog building block and because this device makes good use of the well-matched characteristics of monolithic components, characteristics which are normally expensive to duplicate with discrete parts. A voltage regulator is a circuit which requires similar precision. As shown in the diagram of Figure 1, a basic regulator circuit employs an operational amplifier to compare a reference voltage with a fraction of the output voltage and control a series-pass element to regulate the output.

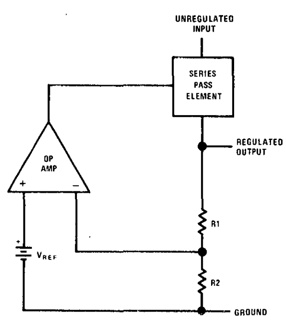


FIGURE 1. Basic Series-Regulator Circuit

Perhaps the reason that monolithic regulators have not appeared sooner is because it is difficult to make one design flexible enough to satisfy an appreciable percentage of the market. Different systems require vastly different output voltages and currents, as well as varying degrees of regulation. In addition, the current handling ability of monolithic circuits is limited because of the large physical die size of high-current transistors. Power dissipation is also a factor, since there are no readily available multi-lead power packages for integrated circuits.

A design is presented here which is versatile enough to overcome many of these problems. It is able to deliver regulated voltages which are externally adjustable from 2V to 30V, operating as either a linear, dissipating regulator or a high efficiency switching regulator. This covers the range from low-level logic circuits to the majority of solid-state linear systems. Although the output current of the integrated circuit is limited (12 mA), an external transistor can be added for currents to 250 mA. A second external power transistor will enable the regulator to deliver currents in excess of 2A.

The regulation is better than 1-percent for widely varying load and line conditions. The device also features 1-percent temperature stability over the full military temperature range, externally adjustable short-circuit-current limiting, fast response to both load and line transients, a small standby power dissipation, freedom from oscillations with varying resistive and reactive loads, and the ability to self start with any load.

VOLTAGE REFERENCE

The voltage reference of a regulator is normally a temperature compensated avalanche diode. Commercially available diodes have a breakdown voltage temperature coefficient of 0.01-percent/°C to 0.0005/°C, depending on selection. Normal integrated circuit processing yields an avalanche diode with acceptable characteristics for this application. The reversed-biased emitter-base junction of the transistors has a breakdown voltage of approximately 6.5V and an unusually uniform temperature coefficient of +2.3 mV/°C. Hence, the positive temperature coefficient of the avalanche diode can be very nearly balanced out by a forward biased, diode-connected transistor to produce a temperature compensated reference. However, exact compensation requires surface impurity concentrations in the transistor-base diffusion which are higher than desired to produce optimized transistors. One design objective of an integrated regulator is, then, to develop a reference element which permits nearly-exact compensation without requiring process alteration.

Another design objective is also centered around the reference. In the regulator circuit of Figure 1, the output voltage can be adjusted down to, but not lower than, the reference voltage. This means that, unless additional circuitry is incorporated, the reference restricts the use of the regulator to applications requiring output voltages above about 8V. It is therefore desirable to obtain as low as possible a reference voltage.

A circuit which provides a simple solution to the temperature compensation problem in addition to supplying a low reference voltage is shown in Figure 2. In this circuit, the breakdown diode is supplied by a current source from the unregulated supply. An emitter follower, Q_1, buffers the output voltage of the diode. The positive temperature coefficient of this buffered output is increased to approximately 7 mV/°C by the addition of the diode connected transistor, Q_2.

A resistor divider reduces this voltage as well as the temperature coefficient to exactly compensate for the negative temperature coefficient of Q_3, producing a temperature compensated output. With the integrated circuit process used, this output voltage is about 1.8V for optimum compensation.

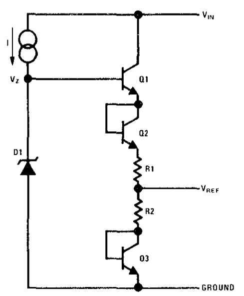


FIGURE 2. Voltage Reference Circuitry

One feature of this integrated reference is that the reverse emitter base breakdown, must have an extremely sharp knee (even in the 1 μA region) in order for the transistors in the circuit to be acceptable. Therefore, the diodes can be reliably operated at low currents where the noise is low and has a nearly uniform frequency spectrum. At higher currents (above about 100 μA for these particular devices) the noise becomes a sensitive function of current with low-repetition-rate pulsations. At even higher currents, the noise reduces in amplitude and loses its current sensitivity but still retains a heavy fluctuation component.

REGULATOR CIRCUIT

A simplified schematic of the regulator is shown in Figure 3. It is a single-stage differential amplifier with a Darlington, emitter-follower output.

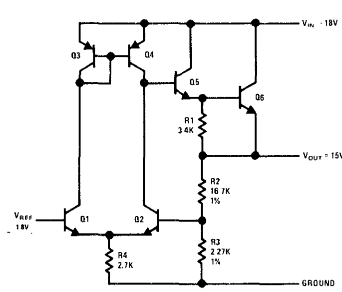


FIGURE 3. Simplified Schematic of the Regulator

The gain of this stage is made much higher than would normally be expected by the use of Q_3 and Q_4 as collector loads. If very large PNP current gain and good matching are assumed, the collector current of Q_4 will be equal to the collector current of Q_1. Therefore, the differential stage will be in balance independent of the magnitude of the collector currents of Q_1 and Q_2 and for the complete range of output voltage settings and input voltage variations. Even this simple circuit gives a no load to full load regulation of 0.2-percent and a line regulation of 0.05-percent per volt.

The complete schematic of the regulator in Figure 4 shows several additions. First, an emitter follower,

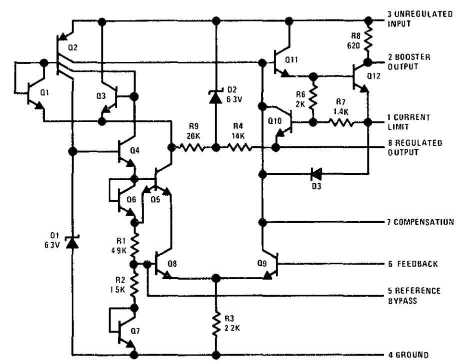


FIGURE 4. Complete Schematic of the LM100

Q_3, and a level-shifting diode, Q_1, have been added to increase the effective current gain of the PNP transistor, Q_2. This device is a lateral PNP which has a low current gain (0.5 to 5) but has the advantage that it can be made without adding any steps or process controls to the normal NPN integrated circuit process. One collector of the PNP serves as a collector load for the error-sensing transistor, Q_9. A second collector supplies current for the breakdown diode, D_1. A third collector, which determines the output current of the other two, maintains a current nearly equal to the collector current of Q_4 by means of negative feedback to the PNP base through Q_3 and Q_1.

The collector current of Q_4 is established at a known fraction of the resistive divider current through R_1 and R_2 by the second emitter on Q_5. This emitter-base junction of Q_5, which is five times larger than that of Q_6, bypasses most of the divider current, at a ratio determined by the relative geometries, to the collector of Q_5. This current, combined with the collector current of Q_8 through the other emitter of Q_5, supplies current for the emitter of Q_3 to drive the base of Q_2.

R_4 and R_9 serve the sole purpose of starting the regulator. They only need to supply enough base current to Q_2 to bring the breakdown diode, D_1, up to voltage. Since it can supply many times the required current under worst-case conditions, starting is ensured.

The clamp diode, D_2, reduces the current variation seen by Q_3 with changes in input voltage, improving line regulation. R_9 is a pinch resistor[2] which has a sheet resistivity more than two orders of magnitude higher than diffused base resistors, so it can be made quite small physically. Pinch resistors do have the disadvantages of non-linear voltage-current characteristic, a large temperature coefficient, a low breakdown voltage and rather large production variations in sheet resistivity. However, as shown in Reference 3, these characteristics can be designed around and actually put to good use, as they are here.

The start-up network is connected to the regulator output terminal, rather than ground, so that the internal power dissipation is minimized without requiring large resistance values. Because of this, the load current of the regulator cannot drop below the current supplied from the unregulated input through R_4. If it does, the circuit will no longer regulate. This is not usually a problem, since the resistive divider which sets the output voltage will normally draw enough current. However, it should be kept in mind in applications where the regulator might be lightly loaded and the difference between the unregulated input voltage and the regulated output voltage is apt to be high.

The collector of the output transistor, Q_{12}, is brought out separately to permit the addition of an external PNP transistor for higher currents. An emitter-base resistor for the external PNP, R_8, is also included. This resistor is shorted out when the regulator is used without the external transistor.

The output of the voltage reference is brought out so that the inherent noise of the breakdown diode can be bypassed out. Since the low operating current of the diode minimizes low-frequency noise, adequate bypassing can be provided by a capacitor as small as 0.1 μF.

The purpose of the clamp diode, D_3, is to keep Q_9 from saturating when the circuit is used as a switching regulator. It plays no functional role in linear operation.

Output-current limiting is provided by Q_{10}. The value of current limit is determined by an external resistor between the current limit, and regulated output terminals. When the voltage drop across this resistor becomes high enough to turn on Q_{10}, it removes base drive from Q_{11} to prevent any further increase in output current. It can be seen from Figure 4 that the voltage turning on Q_{10} is the voltage drop across the external current limit resistor plus a fraction of the emitter-base voltage of the series pass transistor, Q_{12}. This arrangement was used for two reasons. First, less voltage is dropped across the current limit resistor, permitting the circuit to regulate with lower input voltages. Second, since in current limit Q_{12} is operated at a much higher emitter-current density than is Q_{10}, it has a lower negative temperature coefficient of emitter-base voltage. The negative temperature coefficient of the emitter-base voltage of Q_{10} along with this difference in temperature coefficients causes the current limit to decrease by a factor of 2 as the chip temperature increases from 25°C to 150°C. This enables the regulator to deliver maximum current to room temperature but still be protected when the output is shorted and the dissipation increases: the current will decrease as the chip heats, holding the dissipation to a safe level.

It is interesting to note that this current limit scheme will only work when the two transistors are in close thermal contact, as they are in a monolithic integrated circuit.

Since a regulator is an operational amplifier with a large amount of feedback, frequency compensation is required to prevent oscillations. However, a voltage regulator has compensation problems in addition to those encountered in an operational amplifier. For one, the compensation method must provide a high degree of rejection to input voltage transients. Secondly, it must be stable with reactive loads which are far heavier than those normally encountered with operational amplifiers. Thirdly, it must minimize the overshoot caused by large load and line transients.

A compensation method satisfying those requirements is shown in Figure 5. The operational amplifier is connected as an integrator and isolated

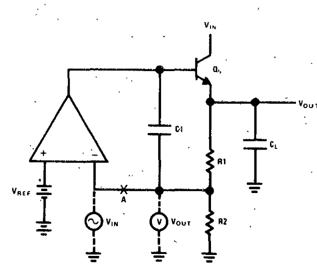


FIGURE 5. Simplified Schematic Showing Regulator Frequency Compensation

from the load with an emitter follower, which serves as a series pass transistor. If the feedback loop is opened at point A and the frequency response measured, it can be seen that the feedback at high frequencies where the loop response must be controlled is through C_F. Reactive loads have little effect since they are isolated from the high frequency feedback path by Q_5.

This compensation method provides excellent response to load transients. That part of a load transient which is not absorbed by the output capacitor, C_L, sees the output impedance of Q_5 which is quite low since it is driven by an operational amplifier with a low AC output impedance.

In the actual regulator (Figure 4) the operational amplifier is a single stage amplifier (Q_9). Hence, it is stable in the integrator connection, with a collector base capacitor on Q_9, without additional compensation which might degrade either the load or line transient response. The series pass transistor is a compound emitter follower to insure isolation from reactive loads. In addition, the stability of the circuit is not dependent on the output impedance of the unregulated supply. It is also stable with no bypass capacitance on the output (if external booster transistors are not used) so it is possible to obtain extremely rapid current limiting as might be required with sensitive transistor loads.

A photomicrograph of the monolithic regulator die is shown in Figure 6. Since the design requires a minimum of resistance, substituting active devices where possible, the entire circuit has been constructed on a 38-mil-square die. This die size is comparable to that of a single silicon transistor.

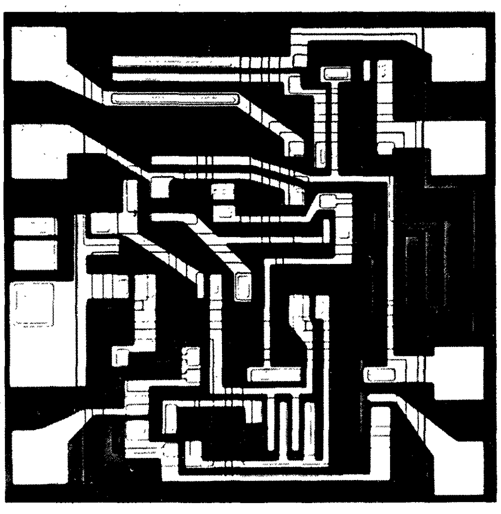


FIGURE 6. Photomicrograph of the LM100 Regulator

APPLICATIONS

The basic regulator circuit for the LM100 is shown in Figure 7. The output voltage is set by R_1 and

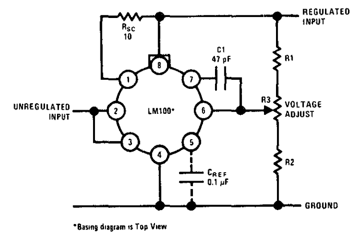


FIGURE 7. Basic Regulator Circuit

R_2, with a fine adjustment provided by the potentiometer, R_3. The resistance seen by the feedback terminal should be approximately 2.2k to minimize drift caused by the bias current on this terminal. Figure 8 is based on this and gives the optimum

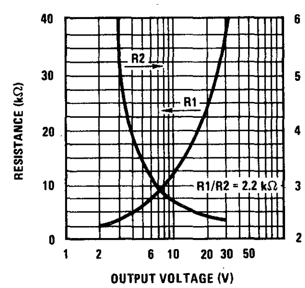


FIGURE 8. Optimum Divider Resistance Values as a Function of Output Voltage

values for R_1 and R_2 as a function of design-center output voltage. The potentiometer should be least 1/4 of R_2 to insure that the output can be set to the desired voltage.

It is possible to operate the regulator with or without internal current limiting. If current limiting is not needed, improved load regulation can be realized by shorting together the current limit terminals ($R_{SC} = 0$). Figure 9 gives the load regulation for this condition. Short circuit protection is obtained by connecting a resistor between the current limit terminals. The resistor value is determined from the current limit sense voltage which is plotted as a function of temperature in Figure 10, for low output currents which corresponds to the case where external booster transistors are used. The current limit sense voltage is the voltage across the current limit terminals when the regulator is current limiting with the output shorted. The regulation and current limit characteristics with a 10Ω current limit resistor are given in Figures 11 and 12, respectively.

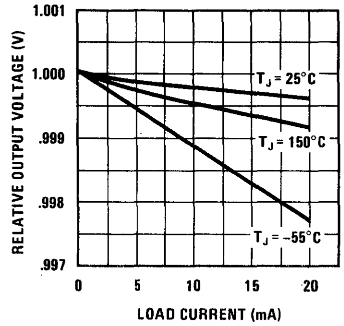


FIGURE 9. Regulation Characteristics Without Current Limiting

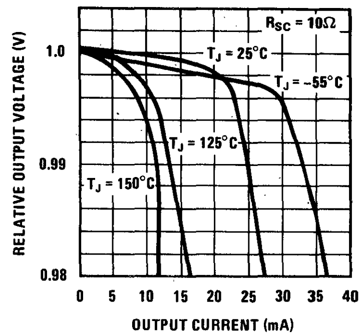


FIGURE 11. Regulation Characteristics with Current Limiting

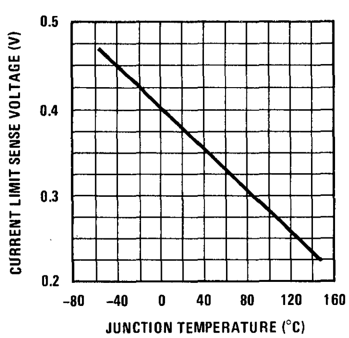


FIGURE 10. Current Limit Sense Voltage as a Function of Junction Temperature

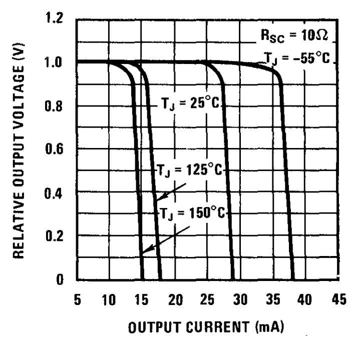


FIGURE 12. Current Limiting Characteristics

A bypass capacitor is not required on the regulator output in the circuit of Figure 7. This permits extremely fast current limiting. The output impedance as a function of frequency is plotted in Figure 13 for this condition. The output impedance at high frequencies can be reduced somewhat by the addition of a bypass, as shown in Figure 13. However, it is necessary to use a low-inductance capacitor (such as a solid-tantalum capacitor) to gain any real advantage. Similarly, bypassing on the unregulated input is not normally needed, although it may be advisable to use a small (0.01 μF) ceramic capacitor when the regulator is fed through long leads which can look like a high-Q resonant circuit.

A reduction in the output noise can be realized by the addition of a 0.1 μF capacitor on the reference bypass terminal. This reduces the noise inherent in the reference diode.

The transient response of the regulator is shown in Figures 14 and 15. Figure 14 shows the response to a current step from 3 mA to 15 mA, without any output bypass capacitor and with a 10Ω current limit resistor. The overshoot can be reduced both by the addition of an output bypass capacitor and by the removal of the current limit resistor since the overshoot is developed across the resistor. The response to a line voltage transient is shown in Figure 15. Neither the line transient response nor the load transient response is affected by the output voltage setting. Therefore, the overshoot becomes a smaller percentage of the output voltage as this voltage is increased.

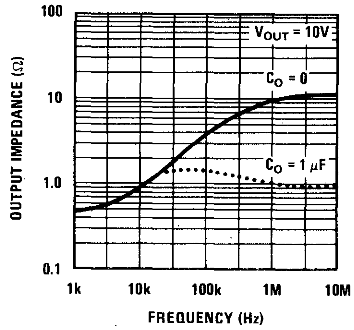


FIGURE 13. Output Impedance as a Function of Frequency

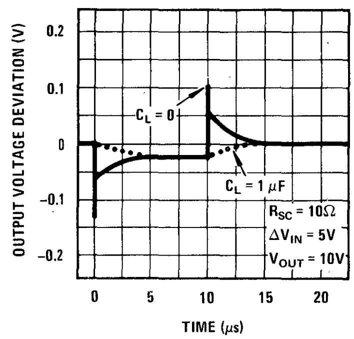


FIGURE 15. Line Transient Response

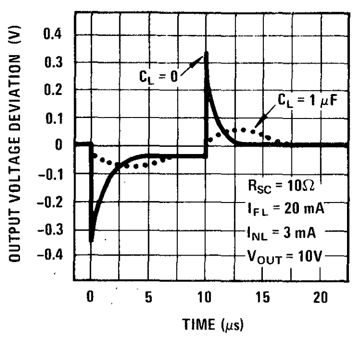


FIGURE 14. Load Transient Response

The regulator provides a line regulation of 0.1-percent per volt change in input voltage. The full-load regulation is better than 0.5-percent. The output voltage drift is less than 1-percent for a temperature change from +25°C to either the −55°C or +125°C temperature extreme. The regulator will operate within specifications for output voltages between 2V and 30V, for input voltages between 8.5V and 40V, for a difference between the input and output voltage between 3V and 30V and over −55°C to +125°C temperature range. This applies whether the regulator is used alone or with external current-boosting transistors.

The load and line regulation given above is for a constant chip temperature on the integrated circuit. Temperature drift effects caused by internal heating must be taken into account separately when the device is operated under conditions of high dissipation.

HIGH POWER REGULATORS

Increased output current capability and improved load regulation can be obtained by the addition of external transistors. The output currents achievable are in fact limited only by the power dissipating and current handling capabilities of the external transistors. The use of these external transistors as the series pass elements also reduces internal dissipation in the integrated circuits and prevents the temperature drift mentioned above.

One circuit which is capable of up to 200 mA load current with 1-percent regulation is shown in Figure 16. The load characteristics are essentially the same as those given in Figures 11 and 12 except that the current scale is multiplied by a factor of 10.

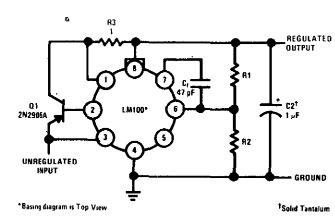


FIGURE 16. Regulator Connected for 200 mA Output Current

When external transistors are used, it is necessary to bypass the output terminal close to the integrated circuit. This is required to suppress oscillations in the minor feedback loop around the external transistor and the output transistor of the integrated circuit (Q_{12} in Figure 4). Since the instability is inclined to occur at high frequencies, a low inductance (solid tantalum) capacitor must be used. Electrolytic capacitors which have a high equivalent series resistance at high frequencies are not effective.

It is not always necessary to bypass the input of the regulator in Figure 16, although it would be advisable if the regulator were being operated from long supply leads or from a source with unknown output impedance characteristics. Again, if a bypass is used, it should be of the low-inductance variety and located close to the regulator.

If output currents much greater than about 200 mA are required, it becomes necessary to add a second external transistor to provide more current gain. The method of accomplishing this is shown in Figure 17. The PNP transistor, Q_2, is used to drive

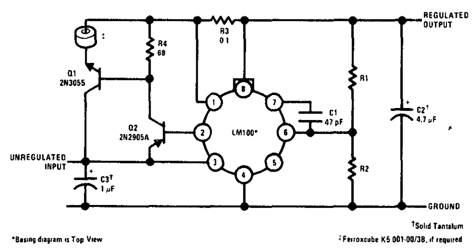


FIGURE 17. Regulator Connected for 2A Output Current

a NPN power transistor, Q_1. With this circuit it is necessary to bypass both the input and output terminals of the regulator, as indicated, with low inductance capacitors to prevent oscillation in the minor feedback loop through Q_2, Q_1 and the output transistor of the integrated circuit. In addition, with certain types of NPN power transistors, it may be necessary to install a ferrite bead[4] in the emitter lead of the device to suppress parasitic oscillations in the power transistor.

The load characteristics of the circuit are again essentially the same as those given in Figures 11 and 12 except that the current scale is multiplied by a factor of 100. As before, the line regulation, temperature drift, etc., are all the same as for the basic regulator.

Another high-power regulator is shown in Figure 18. This circuit is a minor variation of that described previously and is useful when low output voltages

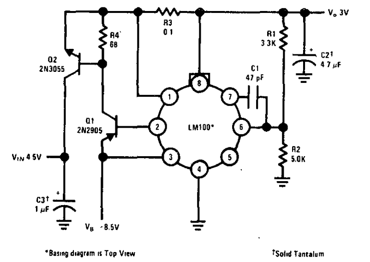


FIGURE 18. Circuit for Obtaining Higher Efficiency Operation with Low Output Voltages

are required. Here, the series pass transistor, Q_2, and the regulator are operated from separate supplies. The series pass transistor is run off of a low voltage main supply which minimizes the input-output differential for increased efficiency. The regulator, on the other hand, operates from a low power bias supply with an output greater than 8.5V.

With this circuit, care must be taken that Q_2 never saturates. Otherwise, Q_1 will try to supply the entire load current and destroy itself, unless the bias supply is current limited.

SWITCHBACK CURRENT LIMITING

With high power regulators it is possible to run into excessive power dissipation when the output is shorted, even though the regulator has current limiting. This happens, with normal current limiting, because the series pass transistor must dissipate the power generated by the full input voltage at a current slightly above the full load current. This dissipation can easily be three times the worst case dissipation in normal operation at full load.

This problem can be overcome by reducing the short circuit current to a value substantially less than the full load current. A circuit for doing this with the LM100 is shown in Figure 19, along with the current limit characteristics obtained. As can be seen from the schematic, two components are added to achieve this — R_4 and R_5. These resistors supply a voltage which bucks out the voltage drop across the current limit sense resistor, R_3, thereby increasing the maximum load current from 0.5A to 2.0A. When the output is shorted, however, this bucking voltage is no longer generated so the short circuit current is only 0.5A.

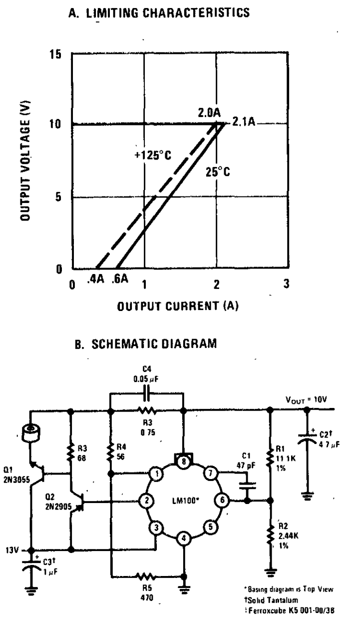


FIGURE 19. Circuit for Obtaining Switchback Current Limiting with the LM100

In this circuit, the voltage drop across the current-sense resistor at full load is 1.5V as compared to about 0.37V when the bucking arrangement is not used. However, this does not increase the minimum input-output voltage differential since the output of the LM100 does not see this increased voltage. With a 10V output and a 2A load, the circuit will still work with input voltages down to 13V, worst case.

In addition to providing the switchback characteristics, R_4 and R_5 also give a 20 mA preload on the regulator so that it can be operated without a load.

NEGATIVE VOLTAGE REGULATORS

A schematic diagram for using the LM100 as both a positive and a negative regulator is shown in Figure 20. With this circuit, the inputs and outputs of both regulators have a common ground.

The positive regulator is identical to those described previously. For the negative regulator, the normal output terminal (pin 8) of the LM100 is grounded, and the ground terminal (pin 4) is connected to the regulated negative output. Hence, as in the usual mode of operation, it regulates the voltage between the output and ground terminals. A PNP booster transistor, Q_2, is connected in the normal manner; and it drives a NPN series-pass transistor, Q_3. The additional components (R_7, R_8, R_9, R_{10} and Q_4) are included to provide current limiting.

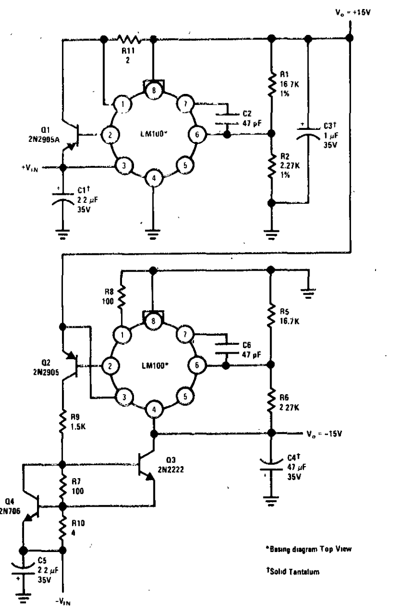


FIGURE 20. Positive and Negative Regulators using the LM100

Figure 21 shows a somewhat simpler circuit. Split secondaries are used on a power transformer to create a floating voltage source for the negative regulator. With this floating source, the conventional regulator is used, except that the output is grounded.

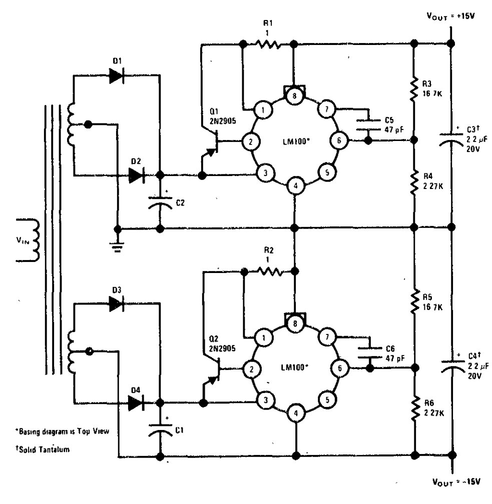


FIGURE 21. Circuit for using the LM100 as Both a Positive and a Negative Regulator

TEMPERATURE COMPENSATING REGULATORS

In the majority of applications, it is desired that the output voltage of the regulator be constant over the operating temperature range of equipment. However, in some applications, improved performance can be realized if the output voltage of the regulator changes with temperature in such a way as to operate the load at its optimum voltage.

An example of this in integrated logic circuitry. Optimum performance can be realized by powering the devices with a voltage that decreases with increasing temperature. A circuit which does this is shown in Figure 22. Silicon diodes are used in

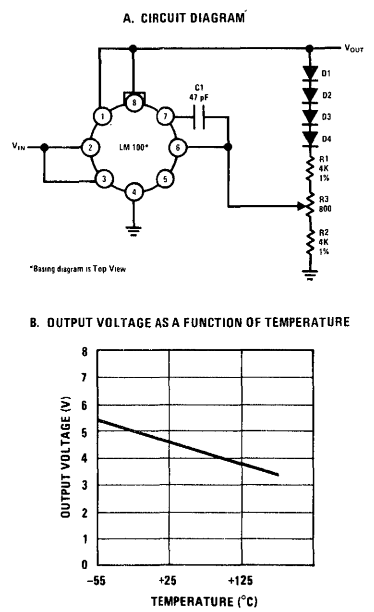


FIGURE 22. Temperature Compensating Voltage Regulator with Negative Temperature Coefficient

the feedback divider to give the required negative temperature coefficient. The advantage of using diodes, rather than thermistors or other temperature sensitive resistors, is that their temperature coefficient is quite predictable so it is not necessary to make cut-and-try adjustments in temperature testing. Reference 6 gives a method of predicting the voltage change in the emitter base voltage of a transistor within 5 mV over a 100°C temperature change. Diodes are not quite this predictable, but diode connected transistors (base shorted to collector) can be used if greater accuracy is required.

SWITCHING REGULATORS

The dissipating-type regulators described already have the advantages of fast response to load transients as well as low noise and ripple. However, since they must dissipate the difference between the unregulated supply power and the output power, they sometimes have a low efficiency. This is not always a problem with AC line-operated equipment because the power loss is easily afforded, because the input voltage is already fairly well regulated, and because losses can be minimized by adjustment of transformer ratios in the power supply. In systems operating from a fixed DC input voltage, the situation is often much different. It might be necessary to regulate a 28V input voltage down to 10V. In this case the power loss can quickly become excessive. This is true even if efficiency is not one of the more important criteria, since the high power dissipation requirements will necessitate expensive power transistors and elaborate heat sinking methods.

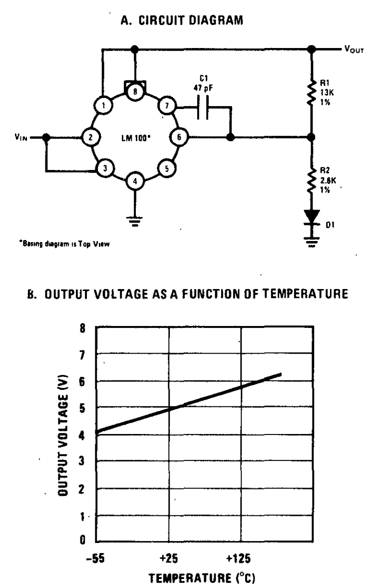


FIGURE 23. Temperature Compensating Voltage Regulator with Positive Temperature Coefficient

One way of overcoming this difficulty is to go to a switching regulator. With switching regulators, efficiencies approaching 90-percent can be realized even though the regulated output voltage is only a fraction of the input voltage. By proper design, transient response and ripple can also be made quite acceptable.

A circuit using the LM100 as a switching regulator is given in Figure 24. It is designed for an application where a 28V DC power source must supply a system operating at 10V.

As shown in Figure 24, the LM100 is connected in much the same way as a linear regulator when

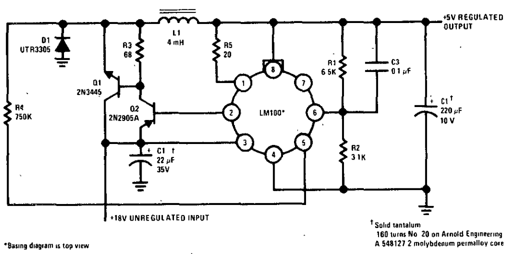


FIGURE 24. High Current Switching Regulator

it is used as a switching regulator. Two external transistors, a NPN and a PNP, are connected in cascade to handle the output current. The regulated output is fed back through a resistive divider which determines the output voltage in the normal manner. The regulator is made to oscillate by applying positive feedback to the reference terminal through R_4 (from Figure 4, the reference terminal is the non-inverting side of the input differential amplifier).

In operation, the switching transistors, Q_1 and Q_2, turn on when the voltage on the feedback terminal is less than that on the reference terminal. This action raises the reference voltage since current is fed into this point from the switch output through R_4. The switching transistors remain on until the voltage on the feedback terminal increases to the higher reference voltage. The regulator then switches off, lowering the reference voltage. It remains off until the voltage on the feedback terminal falls to the lower reference voltage.

When the switch transistors are on, power is delivered from the power source to the load through L_1. When the transistors turn off, the inductor continues to deliver current to the load with D_1 supplying a return path. Since fairly fast rise and fall times are involved, D_1 cannot be an ordinary silicon rectifier. A fast-switching diode must be used to prevent excessive switching transients and large power losses.

Additional details of the circuit are that R_5 limits the output current of the LM100, which drives the base of Q_2. C_3 causes the full output ripple to be delivered to the feedback terminal of the regulator. The bypass capacitor, C_1, is used on the input line both to minimize the voltage transients on this line and to reduce power losses in the line resistance.

A far more complete description of switching regulators is given in Reference 7.

CONCLUSIONS

A regulated power supply is required in practically every piece of electronic equipment. A monolithic integrated circuit was described here which covers an extremely wide voltage range and can supply virtually unlimited power by the addition of external transistors. As indicated in Table 1, its performance is more than adequate for the majority of applications. It is flexible enough to be used as either a linear dissipating regulator or as a high efficiency switching regulator without sacrificing performance in either application. The LM100 also has fast transient response in that overshoot and recovery time can be made vanishingly small in most applications. In addition, the frequency stability is indicated by the fact that it is virtually impossible to make the regulator oscillate in a properly designed circuit.

The suitability of the design to monolithic construction is demonstrated by the fact that it is built on a 38-mil-square silicon die – a size comparable to modern silicon transistors. This small size helps to achieve high yields which are necessary to realize low manufacturing costs and insure off-the-shelf availability.

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TABLE 1. Typical Performance of the National LM100 Voltage Regulator

PARAMETER	CONDITIONS	VALUE
Input Voltage Range		8.5 – 40V
Output Voltage Range		2.0 –30V
Output-Input Voltage Differential		3.0 –30V
Load Regulation	$R_{SC} = 0$, $I_O < 15$ mA	0.1%
Line Regulation		0.05%/V
Temperature Stability	$-55^\circ C \leq T_A \leq +125^\circ C$	0.3%
Output Noise Voltage		0.005%
Long Term Stability		0.1%
Standby Current Drain		1 mA
Minimum Load Current		1.5 mA

March 1969

DESIGNING SWITCHING REGULATORS

INTRODUCTION

The series pass element in a conventional series regulator operates as a variable resistance which drops an unregulated input voltage down to a fixed output voltage. This element, usually a transistor, must be able to dissipate the voltage difference between the input and output at the load current. The power generated can become excessive, particularly when the input voltage is not well regulated and the difference between the input and output voltages is large.

Switching regulators, on the other hand, are capable of high efficiency operation even with large differences between the input and output voltages. The efficiency is, in fact, negligibly affected by the voltage difference since this type of regulator acts as a continuously-variable power converter.

Switching regulators are, therefore, useful in battery-powered equipment where the required output voltage is considerably lower than the battery voltage. An example of this is a missile with a 30V battery as its only power source, containing a large number of integrated logic circuits which require a 5V supply. Switching regulators are also useful in space vehicles where conservation of power is extremely important. In addition, they are frequently the most economical solution in commercial and industrial applications where the increased efficiency reduces the cost of the series-pass transistors and simplifies heat sinking.

One of the disadvantages of switching regulators is that they are more complex than linear regulators, but this is often a substitution of electrical complexity for the thermal and mechanical complexity of high power linear regulators. Another disadvantage is higher output ripple. However, this can be held to a minimum (about 10 mV) and it is at a high enough frequency so that it can be easily filtered out. Another limitation is that the response to load transients is not always as fast as with linear regulators, but this can be largely overcome by proper design. The rejection of line transients, however, is every bit as good if not better than linear regulators. Lastly, switching regulators throw current transients back into the unregulated supply which are somewhat larger than the maximum load current. These, in some cases, can be troublesome unless adequate filtering is used.

This article will demonstrate the use of a monolithic voltage regulator in a number of switching regulator applications. These include both self-oscillating and synchronously driven regulators in the 0.1A to 5A range. Circuits are shown for both positive and negative regulators with output voltages in the 2V to 30V range. Methods of isolating the integrated circuit from the input voltage are given, permitting input voltages in excess of 100V. Further, current limiting schemes which keep peak currents and dissipation well within safe limits for both over-load and short-circuit conditions are presented. Finally, component selection details peculiar to switching regulators are covered.

SWITCHING REGULATOR OPERATION

The method by which a switching regulator produces a voltage conversion with high efficiency can be explained with the aid of Figure 1. Q_1 is a switch transistor which is turned on and off by a pulse waveform with a given duty cycle, and D_1 is a catch diode which provides a continuous path for the inductor current when Q_1 turns off. The voltage waveform on the collector of Q_1 will be as shown in the figure. The output of the LC filter will be the average value of the switched waveform, V_1. If the voltage drops across the transistor and diode are neglected, the output voltage will be

$$V_{OUT} = V_{IN} \frac{t_{on}}{T}; \qquad (1)$$

and it is independent of the load current. It is obvious from the equation that changes in input voltage can be compensated for by varying the duty cycle of the switched waveform. This is what is done in a switching regulator.

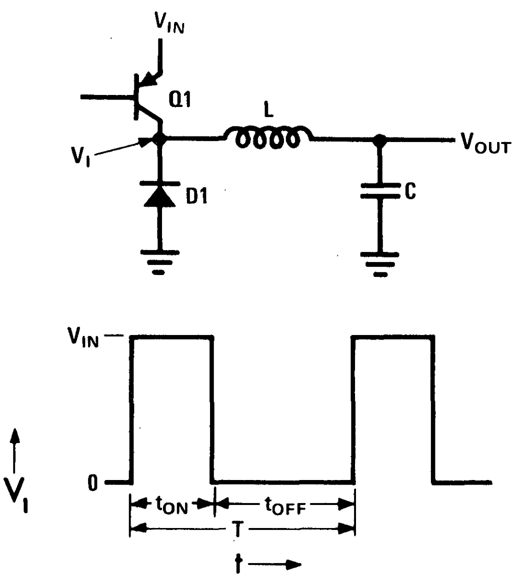


FIGURE 1
Switching Circuit for Voltage Conversion

Figure 2 shows a self-oscillating switching regulator which produces this duty-cycle control. A reference voltage, V_{ref}, equal to the desired output voltage, is supplied to one input of an operational amplifier, A_1. The operational amplifier, in turn, drives the switch transistor. The resistive divider, arranged such that $R_1 >> R_2$, provides a slight amount of positive feedback at high frequencies to make the circuit oscillate. At lower frequencies where the attenuation of the LC filter is less than the attenuation of the resistive divider, there is net negative feedback to the inverting input of the operational amplifier.

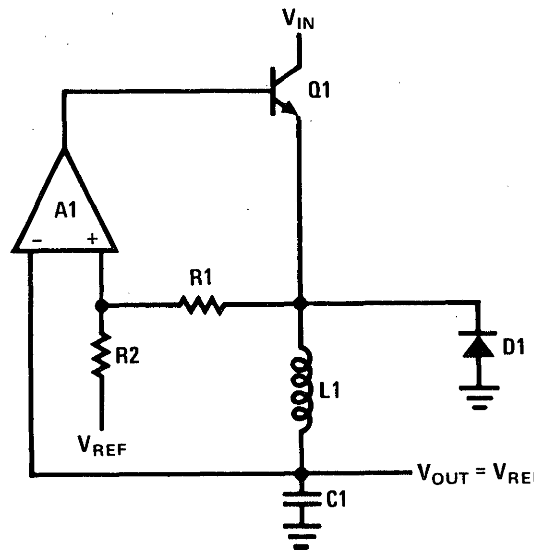


FIGURE 2
Self-oscillating Switching Regulator

In operation, when the circuit is first turned on, the output voltage is less than the reference voltage so the switch transistor is turned on. When this happens, current flow through R_1 raises the voltage on the non-inverting input of the operational amplifier slightly above the reference voltage. The circuit will remain switched on until the output rises to this voltage. The amplifier now goes into the active region, causing the switch to turn off. At this point, the reference voltage seen by the amplifier is *lowered* by feedback through R_1, and the circuit will stay off until the output voltage drops to this lower voltage. Hence, the output voltage oscillates about the reference voltage. The amplitude of this oscillation (or the output ripple) is nearly equal to the voltage fed back through R_1 to R_2 and can be made quite small.

THE LM100

The switching regulator circuits described here use the LM100 integrated voltage regulator as the control element. This device contains, on a single silicon chip, the voltage reference, the operational amplifier and the circuitry for driving a PNP switch transistor. Discrete switch transistors, catch diodes and reactive elements are employed since these components are not easily integrated.

A complete circuit description of the LM100 is given in Application Note AN-1 along with a number of its applications as a linear regulator. However, a brief description will be included here in order to facilitate understanding of the regulator circuits which follow.

Figure 3 shows a schematic diagram of the LM100. The voltage reference portion of the circuit starts with a breakdown diode, D_1, which is supplied by a current source from the unregulated input (one of the collectors of Q_2). The output of the reference diode, which has a positive temperature coefficient of 2.4 mV/°C, is buffered by an emitter follower, Q_4, which increases the temperature coefficient to +4.7 mV/°C. This is further increased to 7 mV/°C by the diode-connected transistor, Q_6. A resistor divider reduces this voltage as well as the temperature coefficient to exactly compensate for the negative temperature coefficient of Q_7, producing a temperature-compensated output of 1.8V.

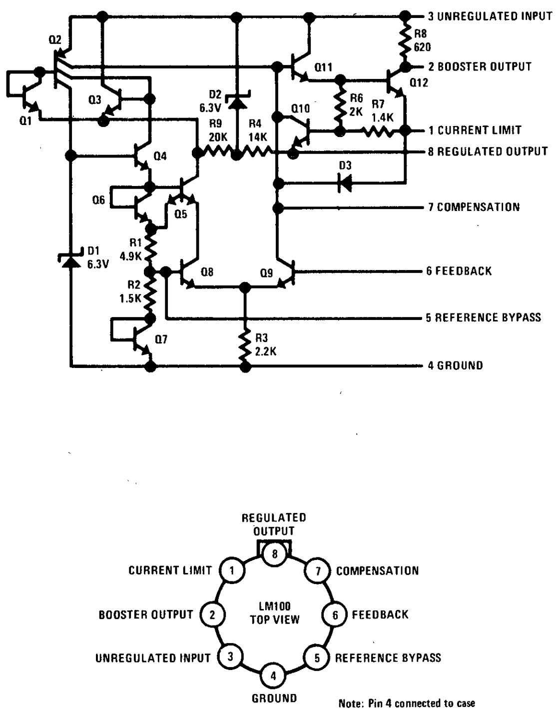


FIGURE 3

Schematic and Connection Diagrams of the LM100 Voltage Regulator

The transistor pair, Q_8 and Q_9, form the input stage of the operational amplifier. The gain of the stage is made high by the use of a current source, one of the collectors of Q_2, as a collector load. The output of this stage drives a compound emitter follower, Q_{11} and Q_{12}. The output of Q_{12} is taken across R_8 to drive the PNP switch transistor. An additional transistor, Q_{10}, is used to limit the output current of Q_{12} to the value required for driving a PNP transistor connected on the booster output. This current is determined by a resistor placed between the current limit and regulated output terminals. The value of the drive current can be determined from Figure 4 which plots the output current as a function of temperature for various current limit resistors.

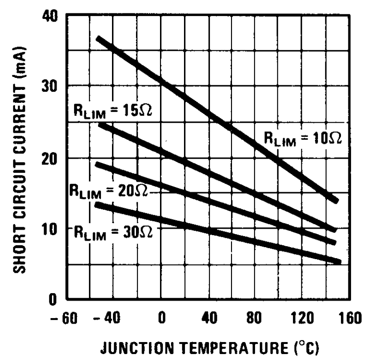


FIGURE 4

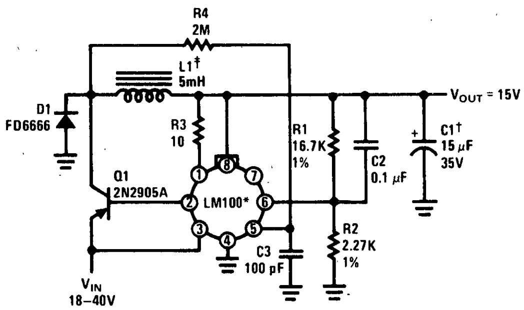
Switched Output Current as a Function of Temperature for Various Values of Current Limit Resistors

As for the remaining details of the circuit, Q_5, Q_3 and Q_1 are part of a bias stabilization circuit for Q_2 to set its collector currents at the desired value. R_9, R_4 and D_2 serve the sole function of starting the regulator. Lastly, D_3 is a clamp diode which keeps Q_9 from saturating when it is switching.

SWITCHING REGULATOR CIRCUITS

Figure 5 demonstrates the use of the LM100 as a switching regulator. Feedback to the inverting input of the operational amplifier (Pin 6 of the LM100) is obtained through a resistive divider which can be used to set the output voltage anywhere in the 2-30V range. R_3 determines the base drive for the switch transistor, Q_1, providing enough drive to saturate it with maximum load current. R_4 works into the 1 kΩ impedance at the reference terminal, producing the positive feedback. C_2 serves to minimize output ripple by causing the full ripple to appear on the feedback terminal. The remaining capacitor, C_3, removes the fast-risetime transients which would otherwise be coupled into Pin 5 through the shunt capacitance of R_4. It must be made small enough so that it does not seriously integrate the waveform at this point.

The circuit shown in Figure 5 is suitable for output currents as high as 500 mA. This limit is set by the output current available from the LM100 to saturate the switch transistor, Q_1. For lower currents, the value of R_3 should be increased so that the base of Q_1 is not driven unnecessarily hard.



*Basing diagram is Top View

†Solid tantalum

‡125 turns #22 on Arnold Engineering A262123-2 molybdenum permalloy core.

FIGURE 5

Switching Regulator Using the LM100

The optimum switching frequency for these regulators has been determined to be between 20 kHz and 100 kHz. At lower frequencies, the core becomes unnecessarily large; and at higher frequencies, switching losses in Q_1 and D_1 become excessive. It is important, in this respect, that both Q_1 and D_1 be fast-switching devices to minimize switching losses.

The output ripple of the regulator at the switching frequency is mainly determined by R_4. It should be evident from the description of circuit operation that the peak-to-peak output ripple will be nearly equal to the peak-to-peak voltage fed back to Pin 5 of the LM100. Since the resistance looking into Pin 5 is approximately 1000Ω, this voltage will be

$$\Delta V_{ref} \simeq \frac{1000\ V_{IN}}{R_4}. \tag{2}$$

In practice, the ripple will be somewhat larger than this. When the switch transistor shuts off, the current in the inductor will be greater than the load current so the output voltage will continue to rise above the value required to shut off the regulator. An important consideration in choosing the value of the inductor is that it be large enough so that the current through it does not change drastically during the switching cycle. If it does, the switch transistor and catch diode must be able to handle peak currents which are significantly larger than the load current. The change in inductor current can be written as

$$\Delta I_L \simeq \frac{V_{OUT} t_{off}}{L}. \tag{3}$$

In order for the peak current to be about 1.2 times the maximum load current, it is necessary that

$$L_1 = \frac{2.5\ V_{OUT} t_{off}}{I_{OUT\ (max)}}. \tag{4}$$

A value for t_{off} can be estimated from

$$t_{off} = \frac{1}{f}\left(1 - \frac{V_{OUT}}{V_{IN}}\right), \tag{5}$$

where f is the desired switching frequency and V_{IN} is the nominal input voltage.

The size of the output capacitor can now be determined from

$$C_1 = \left(\frac{V_{IN} - V_{OUT}}{2L_1 \Delta V_{OUT}}\right)\left(\frac{V_{OUT}}{fV_{IN}}\right)^2, \tag{6}$$

where ΔV_{OUT} is the peak-to-peak output ripple and V_{IN} is the nominal input voltage.

It now remains to determine if the component values obtained above give satisfactory load-transient response. The overshoot of the regulator can be determined from

$$\Delta V_{OUT} = \frac{L_1 (\Delta I_L)^2}{C_1 (V_{IN} - V_{OUT})} \tag{7}$$

for increasing loads, and

$$\Delta V_{OUT} = \frac{L_1 (\Delta I_L)^2}{C_1 V_{OUT}} \tag{8}$$

for decreasing loads, where ΔI_L is the load-current transient. The recovery time is

$$t_r = \frac{2L_1 \Delta I_L}{V_{IN} - V_{OUT}} \tag{9}$$

and

$$t_r = \frac{2L_1 \Delta I_L}{V_{OUT}} \tag{10}$$

for increasing and decreasing loads respectively.

In order to improve the load transient response, it is necessary to allow larger peak to average current ratios in the switch transistor and catch diode. Reducing the value of inductance given by Equation (4) by a factor of 2 will reduce the overshoot by 4 times and halve the response time. This, of course, assumes that the output capacitance is doubled to maintain a constant switching frequency.

The above equations outline a design procedure for determining the value for R_4, L_1, and C_1, given the switching frequency and the output ripple. These equations are not exact, but they do provide a starting point for designing a regulator to fit a given application.

As an example, this design method will be applied to a regulator which must deliver 15V at a maximum current of 300 mA from a 28V supply. To start, a 40 kHz switching frequency will be selected along with an output ripple of 14 mV, peak-to-peak.

From (2), R_4 is calculated to be 2 MΩ. In determining L_1, t_{off} is found to be 11.6 μs from (5). Inserting this into (4) gives a value of 1.45 mH for L_1. The value of C_1 obtained from (6) is then 57.5 μF.

In the actual circuit of Figure 5, a standard value of 47 μF is used for C_1; and L_1 is adjusted to 1.7 mH. The switching frequency obtained experimentally on this circuit is 60 kHz and the peak-to-peak output ripple is 20 mV. The fairly-large disagreement between the calculated and experimental values is not alarming since many simplifying assumptions were made in the derivation of the equations. They do, however, provide a convenient method of handling a large number of mutually-dependent variables to arrive at a working circuit.

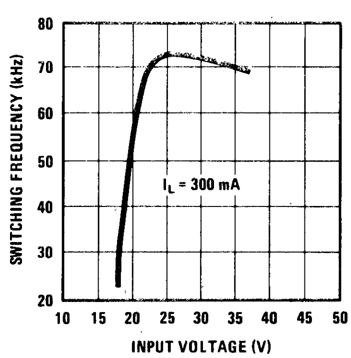


FIGURE 6

Switching Frequency as a Function of Input Voltage

More exact expressions would involve a design procedure which is too cumbersome to be of practical value.

The variation of switching frequency with input voltage and load current is shown in Figures 6 and 7. The sharp rise in frequency at low output currents happens because the output transistor of the LM100 (Q_{12}) begins to supply an appreciable portion of the load current directly.

The efficiency of the regulator over a wide range of input voltages and output currents is given in Figures 8 and 9.

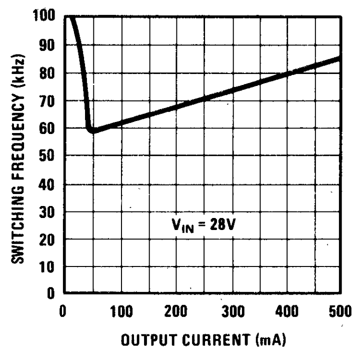


FIGURE 7

Switching Frequency as a Function of Output Current

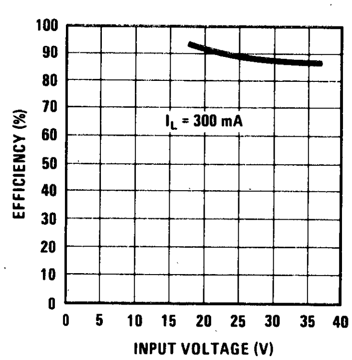


FIGURE 8

Efficiency as a Function of Input Voltage

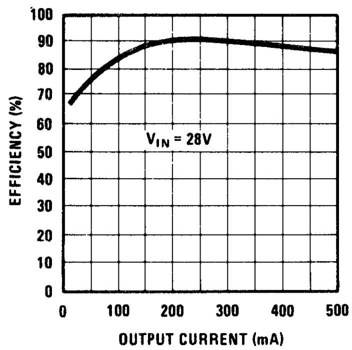


FIGURE 9
Efficiency as a Function of Output Current

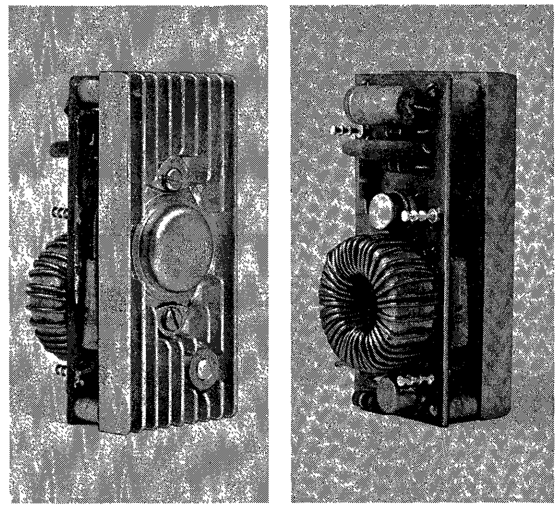


FIGURE 11
High Current Switching Regulator

HIGHER CURRENT REGULATORS

If output currents greater than about 500 mA are required, it is necessary to add another switch transistor to obtain more current gain. This is illustrated in Figure 10. With the exception of the added NPN power switch, Q_2, this circuit is the same as that described previously.

A photograph of a high-current regulator is shown in Figure 11. It is capable of delivering output currents of 3A continuously with only a small heat sink. Figure 12 shows that the efficiency is better than 80 percent at this level. Output currents to 5A can be obtained at reduced efficiency. However, the case temperature of the power switch and catch diode approach 100°C under this condition, so continuous operation is not recommended unless more heat sink is provided.

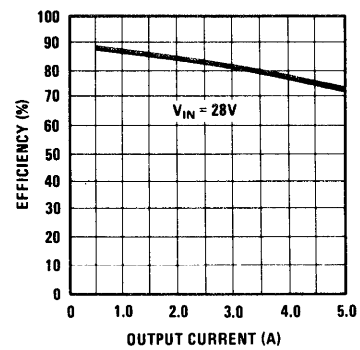
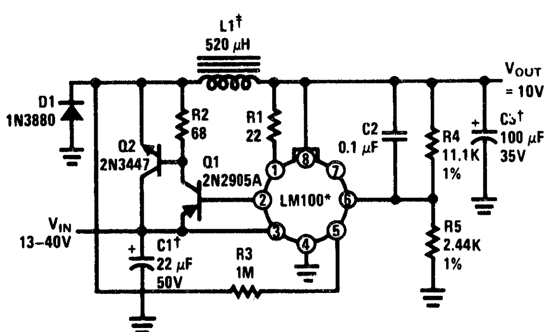


FIGURE 12
Efficiency as a Function of Output Current



*Basing diagram is Top View
†Solid tantalum
‡60 turns =20 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 10
Switching Regulator for Higher Output Currents

Figure 13 shows that the efficiency is not significantly affected by input voltage. In Figure 14 it can be seen that the switching frequency is fairly constant over a wide range of input voltages. Figure 15 shows that the switching frequency increases with increasing load current. The higher dc current through the inductor reduces the incremental inductance causing the frequency to go up. The last graph, Figure 16, illustrates the line regulation of the device. this can be improved by putting a small capacitor (0.01 μF) in series with the positive feedback resistor, R_3, to isolate the reference terminal from the dc input voltage changes.

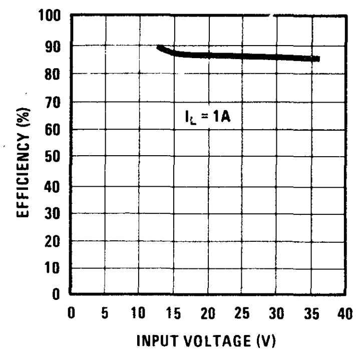


FIGURE 13
Efficiency as a Function of Input Voltage

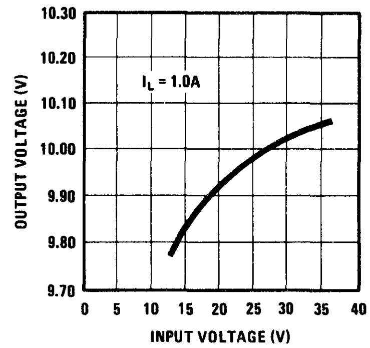


FIGURE 16
Line Regulation

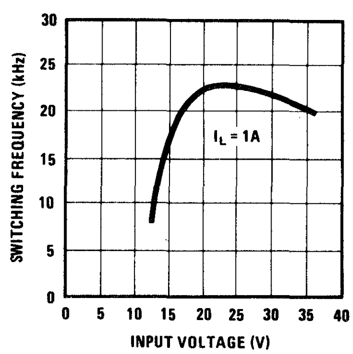


FIGURE 14
Variation of Switching Frequency with Input Voltage

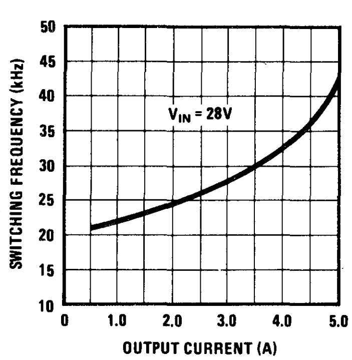


FIGURE 15
Variation of Switching Frequency with Output Current

At low output currents the inductor current can drop to zero at some time after the switch transistor turns off. When this happens, ringing occurs on the switching waveform. This is perfectly normal and causes no ill effects.

The use of solid tantalum capacitors for C_1 and C_3 is recommended when the regulator is expected to perform over the full military temperature range. The reason for using 35V capacitors on the output, even though the output voltage is only 10V, is that the 40 mV peak-to-peak ripple on the output would, for example, exceed the ratings of a 100 μF, 15V capacitor.

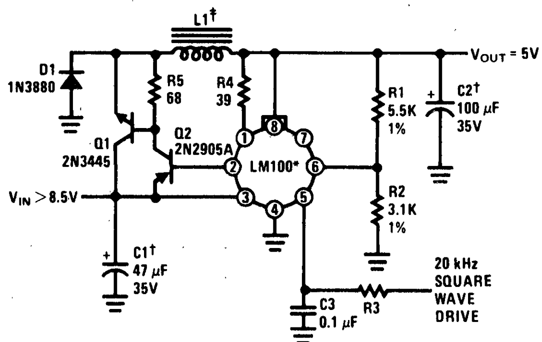
Aluminum electrolytic capacitors have been used successfully over a limited temperature range. And there is basically no reason why wet foil or wet slug tantalums could not be used as long as their equivalent series resistance is low enough so that they behave like capacitors with the high frequency switched-current waveform. It is also important that manufacturer's data be consulted to insure that they can withstand the high frequency ripple.

As was mentioned with the low current regulator, it is necessary to use fast-switching diodes and transistors in these circuits. Ordinary silicon rectifiers or low-frequency power transistors will operate at drastically-reduced efficiencies and will quickly overheat in these circuits.

DRIVEN SWITCHING REGULATOR

When a number of switching regulators are used together in a system it is sometimes desirable to synchronize their operation to more uniformly distribute the switched current waveforms on the input line. Synchronous operation is also wanted when a switching regulator is operated in conjunction with a power converter.

A circuit for synchronizing the switching regulator with a square wave drive signal is shown in Figure 17. In this circuit, positive feedback is not used. Instead, the square wave drive signal is integrated; and the resulting triangular wave (about 40 mV peak-to-peak) is applied to the reference bypass terminal of the LM100. This triangular wave will cause the regulator to switch since its gain is so high that the waveform overdrives it. The duty cycle of the switched waveform is controlled by the voltage on the feedback terminal, Pin 6. If this voltage goes up, the duty cycle will decrease since it is picking off a smaller portion of the triangular wave on Pin 5. By the same token, the duty cycle will decrease if the voltage on Pin 6 drops.



*Basing diagram is Top View
†Solid tantalum
‡100 turns #22 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 17
Driven Switching Regulator

This action produces the desired regulation: if the output voltage starts to go up, it will raise the voltage on Pin 6 such that a smaller portion of the triangular wave is picked off. This reduces the duty cycle, counteracting the output voltage increase.

In order for this circuit to work properly, the ripple voltage on Pin 6 should be less than a quarter of the peak-to-peak amplitude of the triangular wave. If this condition is not satisfied, the regulator will try to oscillate at its own frequency. Further, since the resistance looking into Pin 5 is about 1 kΩ, the integrating capacitor, C_3, should have a capacitive reactance of less than 100Ω at the drive frequency. The value of R_3 is determined so that the amplitude of the triangular wave on Pin 5 is about 40 mV.

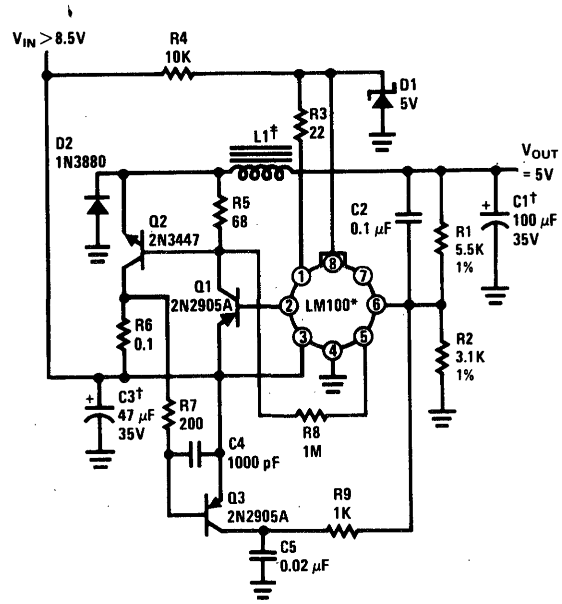
Driven regulators also have other advantages. For one, it is possible to design the LC filter independent of switching frequency considerations. Hence, lower output ripple and better transient response can be realized. A second advantage is the frequency stability. In a self-oscillating regulator, the switching frequency is controlled by a relatively large number of factors. As a result, it is not well determined when normal tolerances are taken into account. With low and medium power regulators, this is not usually a problem since the efficiency does not vary greatly with frequency. However, high power regulators tend to be more frequency sensitive and it is desirable to operate them at constant frequency.

CURRENT LIMITING

In the circuits described previously, the regulator is not protected from overloads or short-circuited output. Providing short-circuit protection is no simple problem, since it is necessary to keep the regulator switching when the output is shorted. Otherwise, the dissipation will become excessive even though the current is limited.

A circuit that does this is shown in Figure 18. The peak current through the switch transistor is sensed by R_6. When the voltage drop across this resistor becomes large enough to turn on Q_3, the output voltage begins to fall since current is being supplied to the feedback terminal of the regulator from the collector of Q_3 so less has to be supplied from the output through R_1. Furthermore, the circuit will continue to oscillate, even with a shorted output, because of positive feedback through R_6 and the relatively-long discharge time constant of C_2.

It is necessary to put a resistor, R_7, in series with the base of Q_3 to insure that excessive current will not be driven into the base. In addition, a capacitor, C_4, must be added across the input of Q_3 so that it does not turn on prematurely on the large current spike (about twice the load current) through the switch transistor caused by pulling the stored charge out of the catch diode. A zener diode bias supply must also be used on the output of the LM100 since the current limiting will not work if the voltage on this point drops below about 1V.



*Basing diagram is Top View
†Solid tantalum
‡70 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 18
Switching Regulator with Current Limiting

The current limiting characteristics of this circuit are shown in Figure 19. Figure 20 shows how the average input current actually drops off as the circuit goes into current limiting.

This current limiting scheme protects the switching transistors from overload or short-circuited output. However, the drop-out current and short-circuit current are not well controlled, so it is

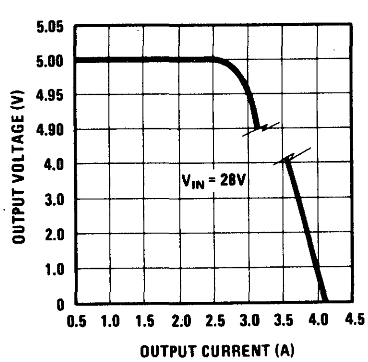


FIGURE 19
Current Limiting Characteristics

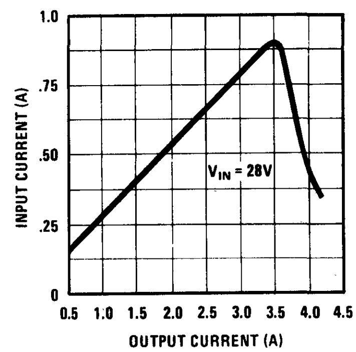
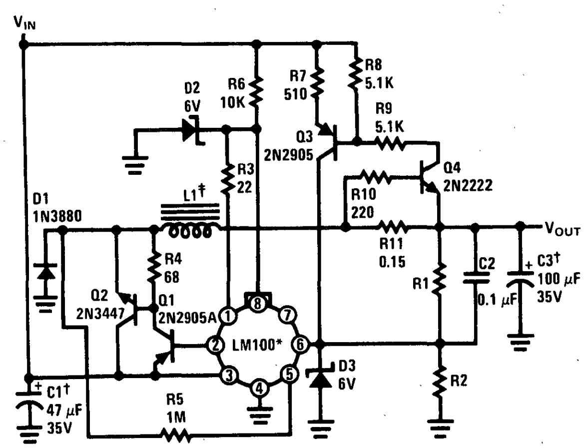


FIGURE 20
Illustrating Drop in Input Current as Regulator Goes Into Limiting

difficult to prove that the circuit will sustain a continuous short circuit under worst-case conditions. This is particularly true with high current regulators where the required amount of overdesign can become quite expensive.

Figure 21 shows a circuit which is more easily designed for continuous short-circuit protection under worst-case conditions. In this circuit, the current-sensing resistor is located in series with the inductor. Therefore, the peak-limiting current can be more precisely determined since the current spike generated by pulling the stored charge out of the catch diode does not flow through the sense resistor.



*Basing diagram is Top View
†Solid tantalum
‡70 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 21
Switching Regulator with Continous Short-Circuit Protection

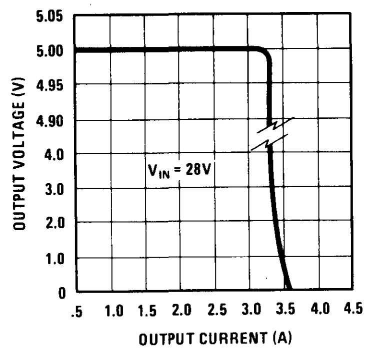


FIGURE 22
Current Limiting Characteristics

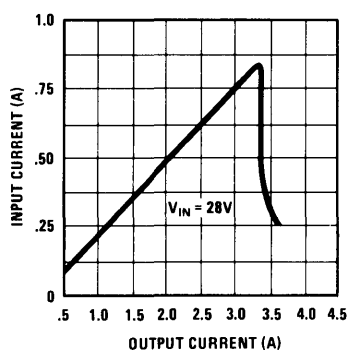


FIGURE 23
Plot of Input Current as Regulator Goes Into Limiting

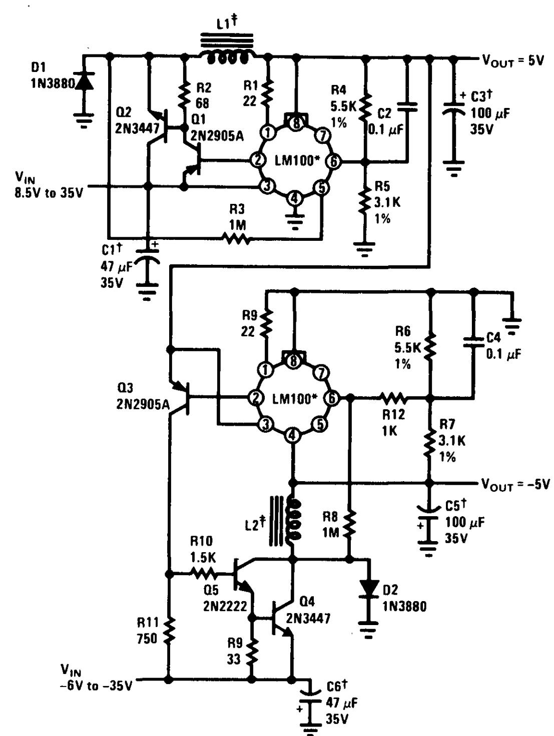
Operation of this circuit is essentially the same as the previous one in that an NPN transistor, Q_4, senses the overcurrent condition and turns on Q_3 which supplies the current-limit signal to the feedback terminal. The zener diode, D_3, is required on the feedback terminal to guarantee that this terminal cannot go more than 0.5V higher than Pin 1. If this does happen, the circuit can latch up and burn out. The performance of this current-limiting scheme is illustrated in Figures 22 and 23.

With this circuit it is not only possible to more accurately determine the limiting current, but as can be seen from Figures 22 and 23, the limiting characteristic is considerably sharper. One disadvantage of this circuit is that the load current flows continuously through the current sense resistor, reducing efficiency. As an example, with a 5V regulated output the efficiency will be reduced by 10 percent at full load.

NEGATIVE REGULATORS

All circuits discussed thus far are for regulators with positive outputs. Although negative regulators can be obtained by floating the unregulated supply and grounding the output, this is not always convenient.

Figure 24 shows a circuit for a negative switching regulator where the unregulated input and regulated output have a common ground. The only limitation of the circuit is that there must be a positive voltage greater than 3V available in order to properly bias the negative regulator.



*Basing diagram is Top View
†Solid tantalum

†60 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core

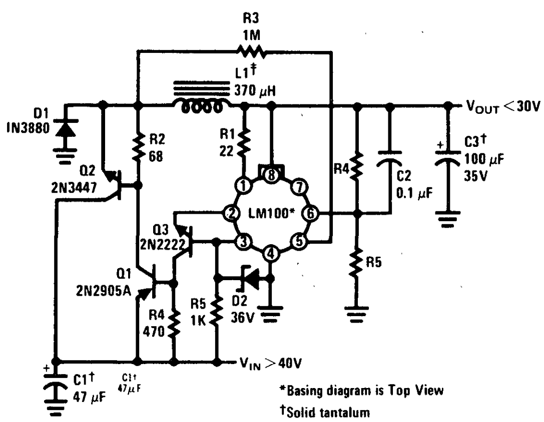
FIGURE 24
Positive and Negative Switching Regulators

In this circuit, the normal output terminal of the LM100 (Pin 8) is grounded and the ground terminal (Pin 4) is connected to the regulated negative output. Hence, as before, it regulates the voltage between the output and ground terminals. The unregulated input terminal (Pin 3) is run from a positive voltage for proper biasing. A PNP booster transistor, Q_3, is connected in the normal manner; and it drives a Darlington-connected NPN switch. Positive feedback is developed by the resistive divider, R_8 and R_{12}.

It is necessary to use a Darlington switch even though the current gain is not needed. The power switch transistor, Q_4, cannot be operated with a fixed base drive: if the base drive is made large enough to insure saturation at maximum load current, it will overstore so badly at lower currents that the output ripple will increase radically. With the extra transistor, however, it is kept out of saturation at lower output currents, eliminating the problem.

HIGH VOLTAGE REGULATORS

With switching regulators, an application can easily arise where the input voltage can be higher than the 40V maximum rating of the LM100, even though the output voltage is within the 30V maximum. As shown in Figure 25, it is possible to isolate the LM100 from the unregulated supply so that it can be used with input voltages limited only by the switch transistors and the catch diode.



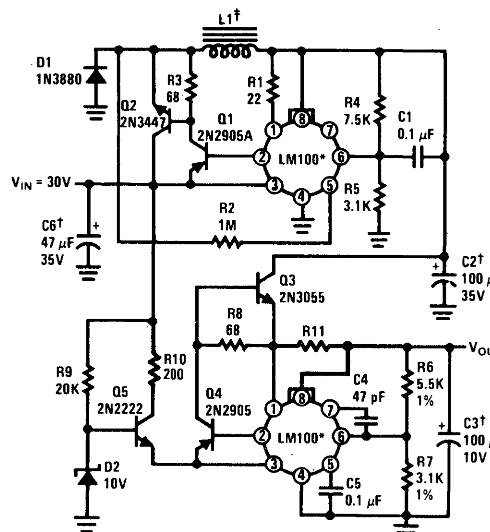
*Basing diagram is Top View
†Solid tantalum
†50 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 25
Switching Regulator for High-voltage Inputs

In this circuit, the voltage seen by the LM100 is maintained at a fixed level within ratings by the zener diode, D_2. The zener voltage must be at least 3V greater than the output voltage. The output of the LM100 is level-shifted up to the input voltage by an additional NPN transistor, Q_3, which is operated common base. This drives the PNP switch driver in the normal manner.

SWITCHING AND LINEAR REGULATOR COMBINATION

In certain applications, the output ripple and load transient response requirements rule out the use of a switching regulator, yet the input-output voltage differential is still high. In this case, a power converter might be used to reduce the input voltage and this reduced voltage would be regulated by a linear regulator. This arrangement, however, is not nearly as efficient as the switching and linear regulator combination shown in Figure 26. The switching regulator not only reduces the input voltage with high efficiency, but it also regulates it. Therefore, the linear regulator operates with a fixed input-output voltage differential which holds dissipation to a minimum.



*Basing diagram is Top View
†Solid tantalum
†60 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 26
Switching and Linear Regulator Combination for Obtaining Very Low Ripple and Fast Transient Response

In this circuit, the linear regulator is biased by a zener pre-regulator (R_9, D_2 and Q_5) to isolate it from noise on the unregulated supply. This separate bias supply permits the linear pass transistor, Q_3, to operate right down into saturation. The collector of Q_3 is supplied by the output of a switching regulator which is made enough higher than the linear regulator output to allow for the maximum overshoot of the switching regulator plus the saturation of Q_3.

SUMMARY

A number of switching regulator circuits which use a readily-available monolithic voltage regulator as the voltage reference and control circuitry have been described. These regulators are useful over a 2V to 30V range for either positive or negative supplies. Although the discussion was limited to circuits providing maximum output currents from 100 mA to 5A, it is possible to obtain even higher output currents. The output current is, in fact, limited by the discrete components – not by the basic design or the integrated circuit.

The majority of the circuits shown were self-oscillating regulators; however, a method of driving the regulator in synchronism with an external clock signal was given. In addition, circuits which provide overload protection, limiting both the output current as well as the power dissipation, were presented. The performance of the regulator circuits was described in detail, and a design procedure was outlined. Suggestions were also made on the selection of components for switching regulators.

The circuits which have been described here for the LM100 work equally well with the LM200 or the LM300. These devices are identical, except that the LM200 is specified over a –25°C to 85°C temperature range and the LM300 is specified from 0°C to 70°C instead of the –55°C to 125°C temperature range for the LM100.

November 1967

DRIFT COMPENSATION TECHNIQUES FOR INTEGRATED DC AMPLIFIERS

INTRODUCTION

With DC amplifiers, it is usually possible to substantially improve drift performance by using additional circuitry along with some form of adjustment. In fact, one of the reasons that discrete-component operational amplifiers have better input current specifications than monolithic amplifiers is that current compensation is used. Monolithic circuits cannot incorporate these techniques because it is not possible to select components or make adjustments. These adjustments can, however, be made external to the amplifier. This article will discuss a number of compensation methods which can substantially reduce the input currents of monolithic amplifiers, especially in limited-temperature-range applications.

Bias current compensation reduces offset and drift when the amplifier is operated from high source resistances. With low source resistances, such as a thermocouple, the drift contribution due to bias current can be made quite small. In this case, the offset voltage drift becomes important.

A technique is presented here by which offset voltage drifts better than 0.5 $\mu V/^{\circ}C$ can be realized. The compensation technique involves only a single room-temperature balance adjustment. Therefore, chopper-stabilized performance can be realized, with low source resistances, in a fairly-simple amplifier without tedious cut-and-try compensation methods.

BIAS CURRENT COMPENSATION

The simplest and most effective way of compensating for bias currents is shown in Figure 1. Here,

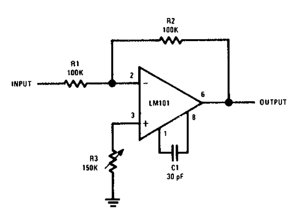


FIGURE 1. Summing Amplifier with Bias-Current Compensation for Fixed Source Resistances.

the offset produced by the bias current on the inverting input is cancelled by the offset voltage produced across the variable resistor, R_3. The main advantage of this scheme, besides its simplicity, is that the bias currents of the two input transistors tend to track well over temperature so that low drift is also achieved. The disadvantage of the method is that a given compensation setting works only with fixed feedback resistors, and the compensation must be readjusted if the equivalent parallel resistance of R_1 and R_2 is changed.

Figure 2 shows a similar circuit for a non-inverting amplifier. The offset voltage produced across the DC resistance of the source due to the input

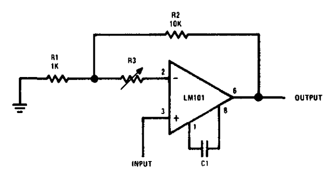


FIGURE 2. Non-Inverting Amplifier with Bias-Current Compensation for Fixed Source Resistances.

current is cancelled by the drop across R_3. For proper adjustment range, R_3 should have a maximum value about three times the source resistance and the equivalent parallel resistance of R_1 and R_2 should be less than one-third the input source resistance.

This circuit has the same advantages as that in Figure 1, however, it can only be used when the input source has a fixed DC resistance, In many applications, such as long-interval integrators, sample-and-hold circuits, switched-gain amplifiers or voltage followers operating from unknown source, the source impedance is not defined. In these cases other compensation schemes must be used.

Figure 3 gives a compensation technique which does not depend upon having a fixed source resistance. A current is injected into the input terminal from the base of a PNP transistor. Since NPN input transistors are used on the integrated amplifier,* the base current of the PNP balances out the base current of the NPN. Further, since a silicon-planar PNP transistor has approximately the same current-gain versus temperature characteristic as the integrated transistors, an improvement in temperature drift will also be realized.† However, perfect

*This is true for all monolithic operational amplifiers presently available.

†If the operational amplifier uses a Darlington input stage, however, the drift compensation will not be nearly as good.

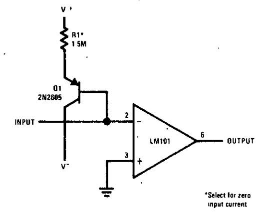


FIGURE 3. Summing Amplifier with Bias-Current Compensation.

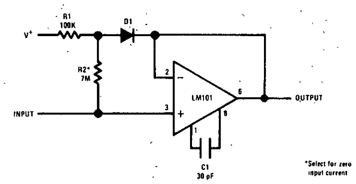


FIGURE 5. Voltage Follower with Bias-Current Compensation.

compensation should not be expected because of unit-to-unit variations in the temperature characteristics of both the PNP transistor and the integrated circuit.

Although the circuit in Figure 3 works well for the summing amplifier connection, it does have limitations in other applications, It could, for example, be used for the voltage follower configuration by connecting the base of the PNP to the non-inverting input. However, this would reduce the input impedance (to about 150 MΩ) because the current supplied by the PNP will vary with the input voltage level.

If this characteristic is objectionable, the more-complicated circuit shown in Figure 4 can be used.

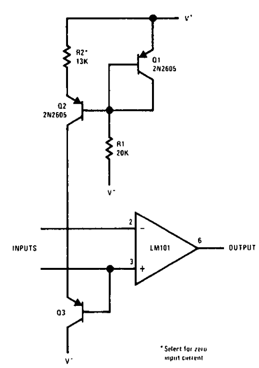


FIGURE 4. Bias-Current Compensation for Non-Inverting Amplifier Operated Over Large Common Mode Range.

The emitter of the PNP transistor is fed from a current source so that the compensating current does not vary with input-voltage level. The design of the current source is such as to give it about the same characteristics as those on the input stage of the better monolithic amplifiers‡ to give closer compensation with changes in temperature and supply voltage. The circuit makes use of the emitter base voltage differential between two transistors operated at different collector currents.[1,2] Although it is recommended in the references that these transistors be well matched, it is not really necessary since the devices are operated at much different collector currents.

Figure 5 shows another compensation scheme for the voltage follower connection. This circuit is much simpler than that shown in Figure 4, but the temperature compensation is not quite as good. The compensating current is obtained through a resistor connected across a diode which is bootstrapped to the output. The diode acts as a regulator so that the compensating current does not change appreciably with signal level, giving input impedances about 1000 MΩ. The negative temperature coefficient of the diode voltage also provides some temperature compensation.

All the circuits discussed thus far have been tailored for particular applications. Figure 6 shows a completely-general scheme wherein both inputs are

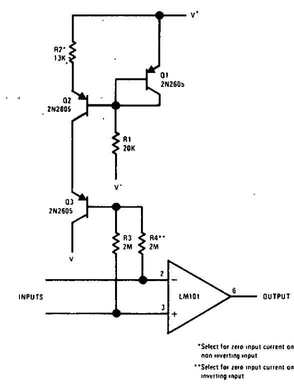


FIGURE 6. Bias-Current Compensation for Differential Inputs.

current compensated over the full common mode range as well as against power supply and temperature variations. This circuit is suitable for use either as a summing amplifier or as a non-inverting amplifier. It is not required that the DC impedance seen by both inputs be equal, although lower drift can be expected if they are.

As was mentioned earlier, all the bias compensation circuits require adjustment. With the circuits in Figures 1 and 2, this is merely a matter of adjusting the potentiometer for zero output with zero input. It is not so simple with the other circuits, however. For one, it is difficult to use potentiometers because a very wide range of resistance values are required to accommodate expected unit-to-unit variations. Resistor selection must therefore be used. Test circuits for selecting bias compensation resistors are given in Figure 7.

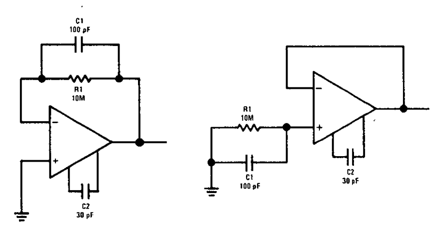


FIGURE 7. Test Circuits for Selecting Bias-Compensation Resistors.

‡The 709 and the LM101.

OFFSET VOLTAGE COMPENSATION

The highly predictable behavior of the emitter-base voltage of transistors has suggested a unique drift compensation method; it is shown in Reference 3 that the offset voltage drift of a differential transistor pair can be reduced by about an order of magnitude by unbalancing the collector currents such that the initial offset voltage is zero. The basis for this comes from the equation for the emitter-base voltage differential of two transistors operating at the same temperature:

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{S2}}{I_{S1}} - \frac{kT}{q} \log_e \frac{I_{C2}}{I_{C1}} \qquad (1)$$

where k is Boltzmann's constant, T is the absolute temperature, q is the charge of an electron, I_S is a constant which depends only on how the transistor is made and I_C is the collector current. This equation is derived in Reference 2.

It is worthwhile noting here that these expressions make no assumptions about the current gain of the transistors. It is shown in Reference 5 and 6 that the emitter-base voltage is a function of collector current not emitter current. Therefore, the balance will not be upset by base current (except for interaction with the DC-source resistance).

The first term in Equation (1) is the offset voltage of the two transistors for equal collector currents. It can be seen that this offset voltage is directly proportional to the absolute temperature – a fact which is substantiated by experiment.[4] The second term is the change of offset voltage which arises from operating the transistors at unequal collector currents. For a fixed ratio of collector currents, this is also proportional to absolute temperature. Hence, if the collector currents are unbalanced in a fixed ratio to give a zero emitter-base voltage differential, the temperature drift will also be zero.

Experiment indicates that this is indeed true. Thermal drifts less than 100 μV over the −55°C to +125°C temperature range have been realized consistently. In order to obtain these low drifts, however, it is almost necessary to use a monolithic transistor pair, since a 0.05°C temperature differential will give a 100 μV drift. With a monolithic pair, the physical proximity of the devices as well as the high thermal conductivity of silicon holds this differential to an absolute minimum.

For low drift, the transistors must operate from a low enough source resistance that the voltage drop across the source due to base current (or base current differential if both bases see the same resistance) is insignificant. Furthermore, the transistors must be operated at a low enough collector current that the emitter-contact and base-spreading resistances are negligible, since Equation (1) assumes that they are zero.

A complete amplifier using this principle is shown in Figure 8. A monolithic transistor pair is used as a preamplifier for a conventional operational amplifier. A null potentiometer, which is set for zero

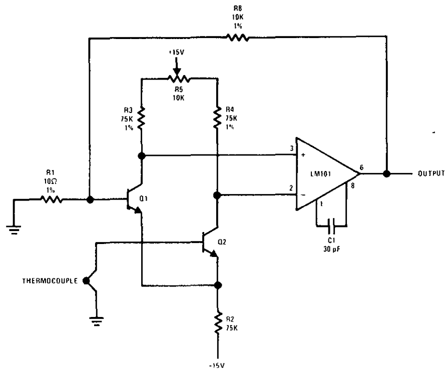


FIGURE 8. Example of a DC Amplifier Using the Drift-Compensation Technique.

output for zero input, unbalances the collector load resistors of the transistor pair such that the collector currents are unbalanced for zero offset. This gives minimum drift. An interesting feature of the circuit is that the performance is relatively unaffected by supply voltage variations: a 1V change in either supply causes an offset voltage change of about 10 μV. This happens because neither term in Equation (1) is affected by the magnitude of the collector currents.

In order to get low drift, it is necessary that the gain of the preamplifier be high enough so that the drift of the operational amplifier does not degrade performance. The gain can be determined from the expression for the transconductance of the input transistors:

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{qI_C}{kT} \qquad (2)$$

The voltage gain is

$$A_V = \frac{\partial V_{OUT}}{\partial V_{IN}} \qquad (3)$$

$$= \frac{\partial I_C}{\partial V_{BE}} R_L \qquad (4)$$

where R_L is the average value of the two collector load resistors on the input stage and I_C is the average of the two collector currents.

Substituting Equation (2), this becomes

$$A_V = \frac{qI_C R_L}{kT} \qquad (5)$$

$$= \frac{qV_{RL}}{kT} \qquad (6)$$

The input referred drift is then

$$\Delta V_{IN} = \frac{\Delta V_{OS} + R_L \, \Delta I_{OS}}{A_V}$$

where ΔV_{OS} is the offset voltage drift of the operational amplifier and ΔI_{OS} is its offset current drift.

Using Equation (7),

$$\Delta V_{IN} = \frac{kT\,(\Delta V_{OS} + R_L \Delta I_{OS})}{qV_{RL}} \tag{8}$$

With the circuit shown in Figure 8, Equation (8) gives a 25 μV input-referred drift for every 10 mV of offset voltage drift or for every 100 nA of offset current drift. It is obvious from this that the offset current drift is most important if an operational amplifier with bipolar input transistors is used.

Another important consideration is the matching of the collector load resistors on the preamplifier stage. A 0.1-percent imbalance in the load resistors due to thermal mismatches or any other cause will produce a 25 μV shift in offset. This includes the balancing potentiometer which can introduce an error that will depend on how far it is set off mid-point if it has a different temperature coefficient than the resistors.

The most obvious use of this type of low drift amplifier is with thermocouples, magnetometers, current shunts, wire strain gauges or similar signal sources where very low drift is required and the source resistance is low enough that the bias currents do not cause a problem. The 0.5 to 1 μV/°C drift* realized with this relatively simple amplifier over a −55°C to +125°C temperature range compares favorably with the drift figures achieved with chopper amplifiers: 0.4 μV/°C for mechanical choppers, 0.5 μV/°C with photoelectric choppers over a 0°C to 55°C temperature range and 2 μV/°C with field-effect-transistor choppers over a −55°C to +125°C temperature range. In order to give some appreciation of the level of performance, it is interesting to note that no substantial improvement in performance would be realized by operating the amplifier in a temperature-controlled oven. Any improvement would be masked by various thermoelectric effects not directly associated with the amplifier unless extreme care were taken in the choice of input lead material, the method of making connections and the balancing of thermal paths. These factors are, in fact, important when making oven tests to verify the drift of the amplifier since thermoelectric effects can easily produce drift voltages larger than those of the amplifier if they are not properly handled.

*Drifts of 0.05 μV/°C over a 0-50°C temperature range were reported in Reference 3 using matched discrete transistors in one can.

SUMMARY

A number of compensation circuits designed to increase the DC resolution of monolithic operational amplifiers have been presented. Both current compensation techniques for high impedance levels as well as methods of achieving chopper-stabilized drift performance at low impedance levels have been covered.

Fairly-simple current compensation which requires that the impedance levels be fixed have been described along with compensation which is effective in cases where the source impedance is not well defined. This latter category includes long-interval integrators, sample-and-hold circuits, switched-gain amplifiers or voltage followers which operate from an unknown source. The application of these schemes is generally limited to integrated amplifiers since modular amplifiers almost always incorporate current compensation.

The drift-reduction techniques provide stabilities better than 0.5 μV/°C for low impedance sources, such as thermocouples, current shunts or strain gauges. With a properly designed circuit, compensation depends only on a single room temperature adjustment, so excellent performance can be obtained from a fairly-simple amplifier.

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April 1968

MONOLITHIC OPERATIONAL AMPLIFIERS – THE UNIVERSAL LINEAR COMPONENT

INTRODUCTION

Operational amplifiers are undoubtedly the easiest and best way of performing a wide range of linear functions from simple amplification to complex analog computation. The cost of monolithic amplifiers is now less than $2.00, in large quantities, which makes it attractive to design them into circuits where they would not otherwise be considered. Yet low cost is not the only attraction of monolithic amplifiers. Since all components are simultaneously fabricated on one chip, much higher circuit complexities than can be used with discrete amplifiers are economical. This can be used to give improved performance. Further, there are no insurmountable technical difficulties to temperature stabilizing the amplifier chip, giving chopper-stabilized performance with little added cost.

Operational amplifiers are designed for high gain, low offset voltage and low input current. As a result, dc biasing is considerably simplified in most applications; and they can be used with fairly simple design rules because many potential error terms can be neglected. This article will give examples demonstrating the range of usefulness of operational amplifiers in linear circuit design. The examples are certainly not all-inclusive, and it is hoped that they will stimulate even more ideas from others. A few practical hints on preventing oscillations in operational amplifiers will also be given since this is probably the largest single problem that many engineers have with these devices.

Although the designs presented use the LM101 operational amplifier and the LM102 voltage follower produced by National Semiconductor, most are generally applicable to all monolithic devices if the manufacturer's recommended frequency compensation is used and differences in maximum ratings are taken into account. A complete description of the LM101 is given elsewhere;[1] but, briefly, it differs from most other monolithic amplifiers, such as the LM709,[2] in that it has a ±30V differential input voltage range, a +15V, −12V common mode range with ±15V supplies and it can be compensated with a single 30 pF capacitor. The LM102,[3] which is also used here, is designed specifically as a voltage follower and features a maximum input current of 10 nA and a 10V/µs slew rate.

OPERATIONAL-AMPLIFIER OSCILLATOR

The free-running multivibrator shown in Figure 1 is an excellent example of an application where one does not normally consider using an operational amplifier. However, this circuit operates at low frequencies with relatively small capacitors because it can use a longer portion of the capacitor time constant since the threshold point of the operational amplifier is well determined. In addition, it has a completely-symmetrical output waveform along with a buffered output, although the symmetry can be varied by returning R2 to some voltage other than ground.

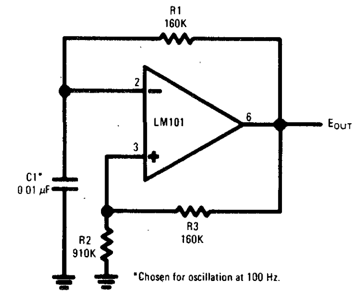


FIGURE 1. Free-Running Multivibrator

Another advantage of the circuit is that it will always self start and cannot hang up since there is more dc negative feedback than positive feedback. This can be a problem with many "textbook" multivibrators.

Since the operational amplifier is used open loop, the usual frequency compensation components are not required since they will only slow it down. But even without the 30 pF capacitor, the LM101 does have speed limitations which restrict the use of this circuit to frequencies below about 2 kHz.

The large input voltage range of the LM101 (both differential and single ended) permits large voltage swings on the input so that several time constants of the timing capacitor, C1, can be used. With most other amplifiers, R2 must be reduced to keep from exceeding these ratings, which requires that C1 be increased. Nonetheless, even when large values are needed for C1, smaller polarized capacitors may be used by returning them to the positive supply voltage instead of ground.

LEVEL SHIFTING AMPLIFIER

Frequently, in the design of linear equipment, it is necessary to take a voltage which is referred to some dc level and produce an amplified output which is referred to ground. The most straightforward way of doing this is to use a differential amplifier similar to that shown in Figure 2a. This circuit, however, has the disadvantages that the signal source is loaded by current from the input divider, R3 and R4, and that the feedback resistors must be very well matched to prevent erroneous outputs from the common mode input signal.

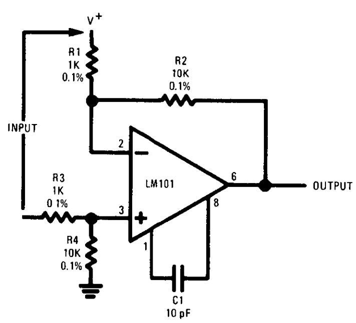
A circuit which does not have these problems is shown in Figure 2b. Here, an FET transistor on the output of the operational amplifier produces a voltage drop across the feedback resistor, R1, which is equal to the input voltage. The voltage across R2 will then be equal to the input voltage multiplied by the ratio, R2/R1; and the common mode rejection will be as good as the basic rejection of the amplifier, independent of the resistor tolerances. This voltage is buffered by an LM102 voltage follower to give a low impedance output.

An advantage of the LM101 in this circuit is that it will work with input voltages up to its positive supply voltages as long as the supplies are less than ±15V.

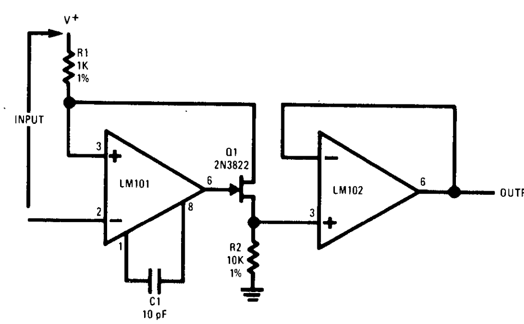
VOLTAGE COMPARATORS

The LM101 is well suited to comparator applications for two reasons: first, it has a large differential input voltage range and, second, the output is easily clamped to make it compatible with various driver and logic circuits. It is true that it doesn't have the speed of the LM710[4] (10 μs versus 40 ns, under equivalent conditions); however, in many linear applications speed is not a problem and the lower input currents along with higher voltage capability of the LM101 is a tremendous benefit.

Two comparator circuits using the LM101 are shown in Figure 3. The one in Figure 3a shows a clamping scheme which makes the output signal directly compatible with DTL or TTL integrated circuits. An LM103 breakdown diode clamps the output at 0V or 4V in the low or high states, respectively. This particular diode was chosen because it has a sharp breakdown and low equivalent capacitance. When working as a comparator, the amplifier operates open loop so normally no frequency compensation is needed. Nonetheless, the stray capacitance between Pins 5 and 6 of the amplifier should be minimized to prevent low level oscillations when the comparator is in the active region. If this becomes a problem, a 3 pF capacitor on the normal compensation terminals will eliminate it.

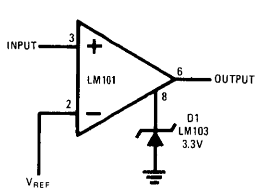


a. Standard Differential Amplifier

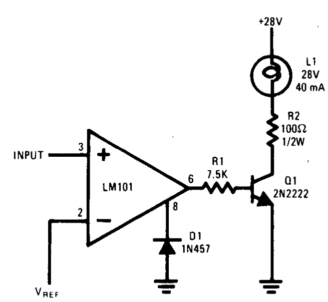


b. Level-Isolation Amplifier

FIGURE 2. Level-Shifting Amplifiers



a. Comparator for Driving DTL and TTL Integrated Circuits



b. Comparator and Lamp Driver

FIGURE 3. Voltage Comparator Curcuits

Figure 3b shows the connection of the LM101 as a comparator and lamp driver. Q1 switches the lamp, with R2 limiting the current surge resulting from turning on a cold lamp. R1 determines the base drive to Q1 while D1 keeps the amplifier from putting excessive reverse bias on the emitter-base junction of Q1 when it turns off.

MORE OUTPUT CURRENT SWING

Because almost all monolithic amplifiers use class-B output stages, they have good loaded output voltage swings, delivering ±10V at 5 mA with ±15V supplies. Demanding much more current from the integrated circuit would require, for one, that the output transistors be made considerably larger. In addition, the increased dissipation could give rise to troublesome thermal gradients on the chip as well as excessive package heating in high-temperature applications. It is therefore advisable to use an external buffer when large output currents are needed.

A simple way of accomplishing this is shown in Figure 4. A pair of complementary transistors are used on the output of the LM101 to get the increased current swing. Although this circuit does have a dead zone, it can be neglected at frequencies below 100 Hz because of the high gain of the amplifier. R1 is included to eliminate parasitic oscillations from the output transistors. In addition, adequate bypassing should be used on the collectors of the output transistors to insure that the output signal is not coupled back into the amplifier. This circuit does not have current limiting, but it can be added by putting 50Ω resistors in series with the collectors of Q1 and Q2.

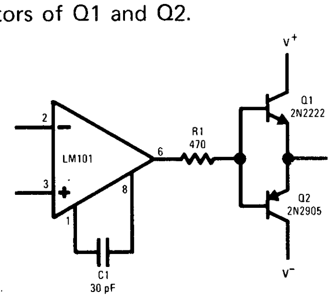


FIGURE 4. High Current Output Buffer

AN FET AMPLIFIER

For ambient temperatures less than about 70°C, junction field effect transistors can give exceptionally low input currents when they are used on the input stage of an operational amplifier. However, monolithic FET amplifiers are not now available since it is no simple matter to diffuse high quality FET's on the same chip as the amplifier. Nonetheless, it is possible to make a good FET amplifier using a discrete FET pair in conjunction with a monolithic circuit.

Such a circuit is illustrated in Figure 5. A matched FET pair, connected as source followers, is put in front of an integrated operational amplifier. The

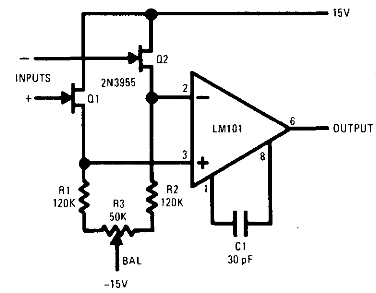


FIGURE 5. FET Operational Amplifier

composite circuit has roughly the same gain as the integrated circuit by itself and is compensated for unity gain with a 30 pF capacitor as shown. Although it works well as a summing amplifier, the circuit leaves something to be desired in applications requiring high common mode rejection. This happens both because resistors are used for current sources and because the FET's by themself do not have good common mode rejection.

STORAGE CIRCUITS

A sample-and-hold circuit which combines the low input current of FET's with the low offset voltage of monolithic amplifiers is shown in Figure 6. The circuit is a unity gain amplifier employing an operational amplifier and an FET source follower. In operation, when the sample switch, Q2, is turned on, it closes the feedback loop to make the output equal to the input, differing only by the offset voltage of the LM101. When the switch is opened, the charge stored on C2 holds the output at a level equal to the last value of the input voltage.

Some care must be taken in the selection of the holding capacitor. Certain types, including paper and mylar, exhibit a polarization phenomenon which causes the sampled voltage to drop off by about 50 mV, and then stabilize, when the capacitor is exercised over a 5V range during the sample interval. This drop off has a time constant in the order of seconds. The effect, however, can be minimized by using capacitors with teflon, polyethylene, glass or polycarbonate dielectrics.

Although this circuit does not have a particularly low output resistance, fixed loads do not upset the accuracy since the loading is automatically compensated for during the sample interval. However, if the load is expected to change after sampling, a buffer such as the LM102 must be added between the FET and the output.

A second pole is introduced into the loop response of the amplifier by the switch resistance and the holding capacitor, C2. This can cause problems with overshoot or oscillation if it is not compensated for by adding a resistor, R1, in series with the LM101 compensation capacitor such that the breakpoint of the R1C1 combination is roughly equal to that of the switch and the holding capacitor.

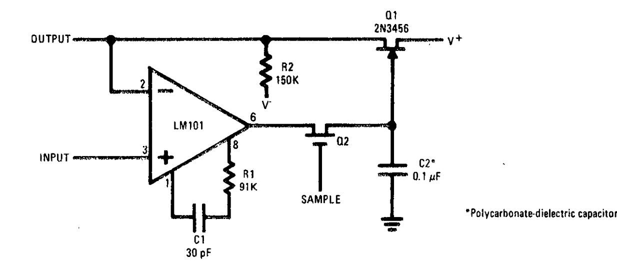


FIGURE 6. Low Drift Sample and Hold

It is possible to use an MOS transistor for Q1 without worrying about the threshold stability. The threshold voltage is balanced out during every sample interval so only the short-term threshold stability is important. When MOS transistors are used along with mechanical switches, drift rates less than 10 mV/min can be realized.

Additional features of the circuit are that the amplifier acts as a buffer so that the circuit does not load the input signal. Further, gain can also be provided by feeding back to the inverting input of the LM101 through a resistive divider instead of directly.

The peak detector in Figure 7 is similar in many respects to the sample-and-hold circuit. A diode is used in place of the sampling switch. Connected as shown, it will conduct whenever the input is greater than the output, so the output will be equal to the peak value of the input voltage. In this case, an LM102 is used as a buffer for the storage capacitor, giving low drift along with a low output resistance.

As with the sample and hold, the differential input voltage range of the LM101 permits differences between the input and output voltages when the circuit is holding.

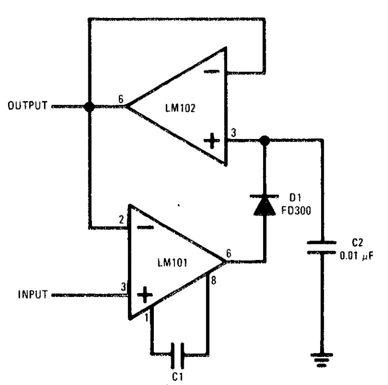


FIGURE 7. Positive Peak Detector with Buffered Output

NON-LINEAR AMPLIFIERS

When a non-linear transfer function is needed from an operational amplifier, many methods of obtaining it present themself. However, they usually require diodes and are therefore difficult to temperature compensate for accurate breakpoints. One way of getting around this is to make the output swing so large that the diode threshold is negligible by comparison, but this is not always practical.

A method of producing very sharp, temperature-stable breakpoints in the transfer function of an operational amplifier is shown in Figure 8. For small input signals, the gain is determined by R1 and R2. Both Q2 and Q3 are conducting to some degree, but they do not affect the gain because their current gain is high and they do not feed any appreciable current back into the summing mode. When the output voltage rises to 2V (determined by R3, R4 and V^-), Q3 draws enough current to saturate, connecting R4 in parallel with R2. This cuts the gain in half. Similarly, when the output voltage rises to 4V, Q2 will saturate, again halving the gain.

Temperature compensation is achieved in this circuit by including Q1 and Q4. Q4 compensates the emitter-base voltage of Q2 and Q3 to keep the voltage across the feedback resistors, R4 and R6, very nearly equal to the output voltage while Q1 compensates for the emitter base voltage of these transistors as they go into saturation, making the voltage across R3 and R5 equal to the negative supply voltage. A detrimental effect of Q4 is that it causes the output resistance of the amplifier to increase at high output levels. It may therefore be necessary to use an output buffer if the circuit must drive an appreciable load.

SERVO PREAMPLIFIER

In certain servo systems, it is desirable to get the rate signal required for loop stability from some sort of electrical, lead network. This can, for example, be accomplished with reactive elements in the feedback network of the servo preamplifier.

Many saturating servo amplifiers operate over an extremely wide dynamic range. For example, the maximum error signal could easily be 1000 times the signal required to saturate the system. Cases like this create problems with electrical rate networks because they cannot be placed in any part

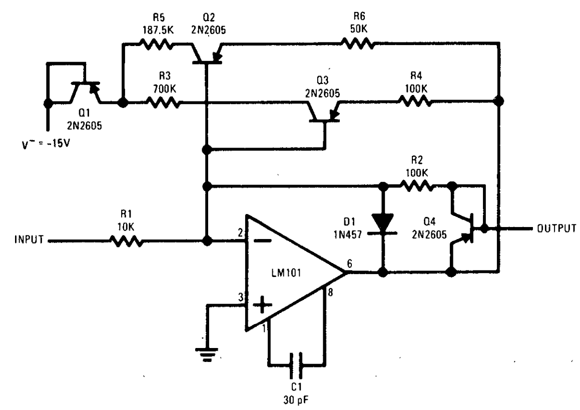


FIGURE 8. Nonlinear Operational Amplifier with Temperature-Compensated Breakpoints

of the system which saturates. If the signal into the rate network saturates, a rate signal will only be developed over a narrow range of system operation; and instability will result when the error becomes large. Attempts to place the rate networks in front of the error amplifier or make the error amplifier linear over the entire range of error signals frequently gives rise to excessive dc error from signal attenuation.

These problems can be largely overcome using the kind of circuit shown in Figure 9. This amplifier operates in the linear mode until the output voltage reaches approximately 3V with 30 μA output current from the solar cell sensors. At this point the breakdown diodes in the feedback loop begin to conduct, drastically reducing the gain. However, a rate signal will still be developed because current is being fed back into the rate network (R1, R2 and C1) just as it would if the amplifier had remained in the linear operating region. In fact, the amplifier will not actually saturate until the error current reaches 6 mA, which would be the same as having a linear amplifier with a ±600V output swing.

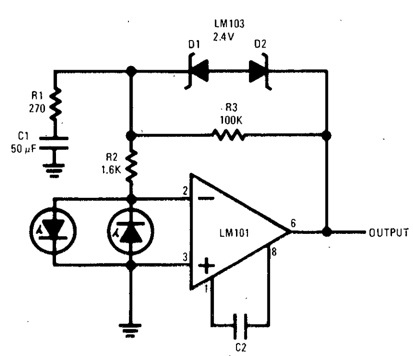


FIGURE 9. Saturating Servo Preamplifier with Rate Feedback

COMPUTING CIRCUITS

In analog computation it is a relatively simple matter to perform such operations as addition, subtraction, integration and differentiation by incorporating the proper resistors and capacitors in the feedback circuit of an amplifier. Many of these circuits are described in reference 5. Multiplication and division, however, are a bit more difficult. These operations are usually performed by taking the logarithms of the quantities, adding or subtracting as required and then taking the antilog.

At first glance, it might appear that obtaining the log of a voltage is difficult; but it has been shown[6] that the emitter-base voltage of a silicon transistor follows the log of its collector current over as many as nine decades. This means that common transistors can be used to perform the log and antilog operations.

A circuit which performs both multiplication and division in this fashion is shown in Figure 10. It gives an output which is proportional to the product of two inputs divided by a third, and it is about the same complexity as a divider alone.

The circuit consists of three log converters and an antilog generator. Log converters similar to these have been described elsewhere,[7] but a brief description follows. Taking amplifier A1, a logging transistor, Q1, is inserted in the feedback loop such that its collector current is equal to the input voltage divided by the input resistor, R1. Hence, the emitter-base voltage of Q1 will vary as the log of the input voltage, E1.

A2 is a similar amplifier operating with logging transistor, Q2. The emitter-base junctions of Q1 and Q2 are connected in series, adding the log voltages. The third log converter produces the log of E3. This is series-connected with the antilog transistor, Q4; and the combination is hooked in parallel with the output of the other two log convertors. Therefore, the emitter-base of Q4 will see the log of E3 subtracted from the sum of the logs of E1 and E2. Since the collector current of a transistor varies as the exponent of the emitter-base voltage, the collector current of Q4 will be proportional to the product of E1 and E2 divided by E3. This current is fed to the summing amplifier, A4, giving the desired output.

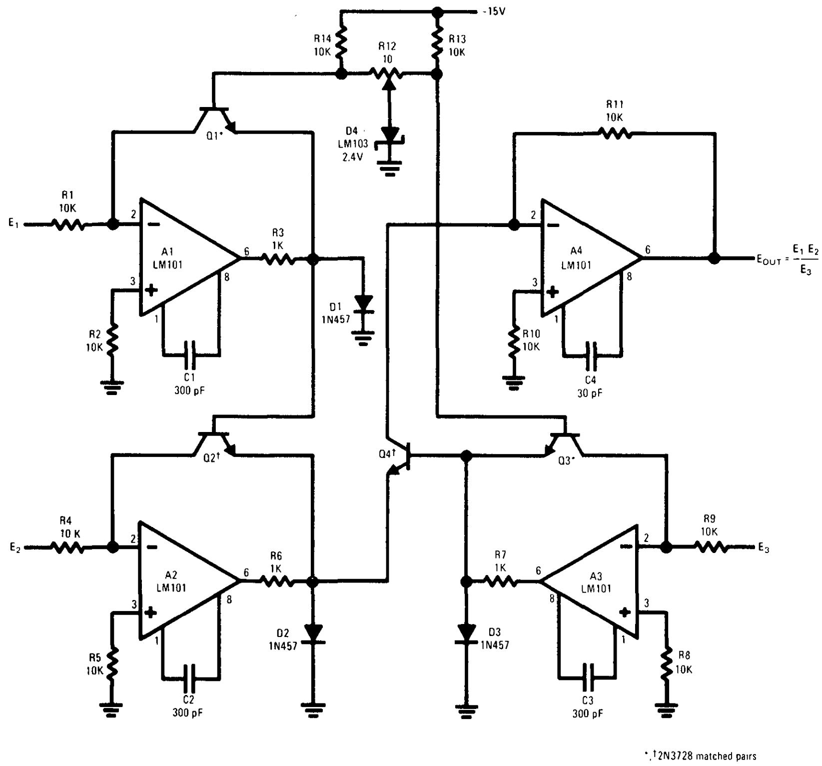


FIGURE 10. Analog Multiplier/Divider

This circuit can give 1-percent accuracy for input voltages from 500 mV to 50V. To get this precision at lower input voltages, the offset of the amplifiers handling them must be individually balanced out. The zener diode, D4, increases the collector-base voltage across the logging transistors to improve high current operation. It is not needed, and is in fact undesirable, when these transistors are running at currents less than 0.3 mA. At currents above 0.3 mA, the lead resistances of the transistors can become important (0.25Ω is 1-percent at 1 mA) so the transistors should be installed with short leads and no sockets.

An important feature of this circuit is that its operation is independent of temperature because the scale factor change in the log converter with temperature is compensated by an equal change in the scale factor of the antilog generator. It is only required that Q1, Q2, Q3 and Q4 be at the same temperature. Dual transistors should be used and arranged as shown in the figure so that thermal mismatches between cans appear as inaccuracies in scale factor (0.3-percent/°C) rather than a balance error (8-percent/°C). R12 is a balance potentiometer which nulls out the offset voltages of all the logging transistors. It is adjusted by setting all input voltages equal to 2V and adjusting for a 2V output voltage.

The logging transistors provide a gain which is dependent on their operating level, which complicates frequency compensation. Resistors (R3, R6 and R7) are put in the amplifier output to limit the maximum loop gain, and the compensation capacitor is chosen to correspond with this gain. As a result, the amplifiers are not especially designed for speed, but techniques for optimizing this parameter are given in reference 6.

Finally, clamp diodes D1 through D3, prevent exceeding the maximum reverse emitter-base voltage of the logging transistors with negative inputs.

ROOT EXTRACTOR*

Taking the root of a number using log converters is a fairly simple matter. All that is needed is to take the log of a voltage, divide it by, say 1/2 for the square root, and then take the antilog. A circuit which accomplishes this is shown in Figure 11. A1 and Q1 form the log converter for the input signal. This feeds Q2 which produces a level shift to give zero voltage into the R4, R5 divider for a 1V input. This divider reduces the log voltage by the ratio for the root desired and drives the buffer amplifier, A2. A2 has a second level shifting diode, Q3, its feedback network which gives the output voltage needed to get a 1V output from the antilog generator, consisting of A3 and Q4, with a unity

*The "extraction" used here doubtless has origin in the dental operation most of us would fear less than having to find even a square root without tables or other aids.

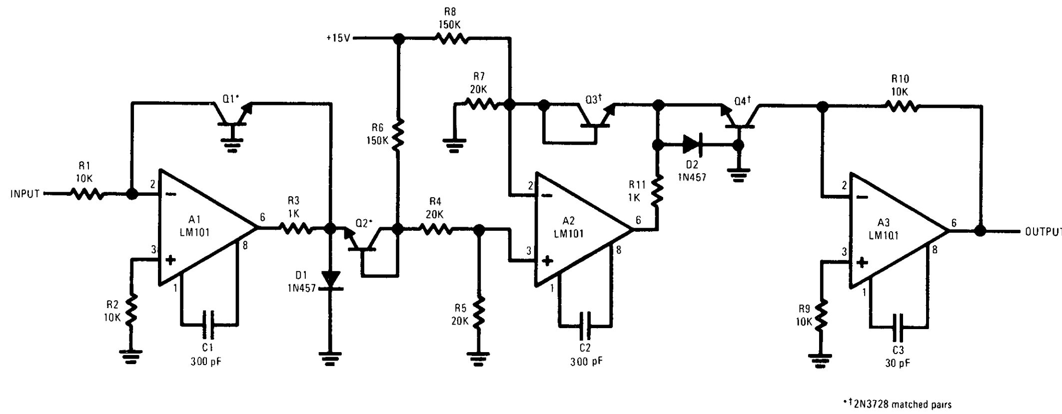


FIGURE 11. Root Extractor

input. The offset voltages of the transistors are nulled out by imbalancing R6 and R8 to give 1V output for 1V input, since any root of one is one.

Q2 and Q3 are connected as diodes in order to simplify the circuitry. This doesn't introduce problems because both operate over a very limited current range, and it is really only required that they match. R7 is a gain-compensating resistor which keeps the currents in Q2 and Q3 equal with changes in signal level.

As with the multiplier/divider, the circuit is insensitive to temperature as long as all the transistors are at the same temperature. Using transistor pairs and matching them as shown minimizes the effects of gradients.

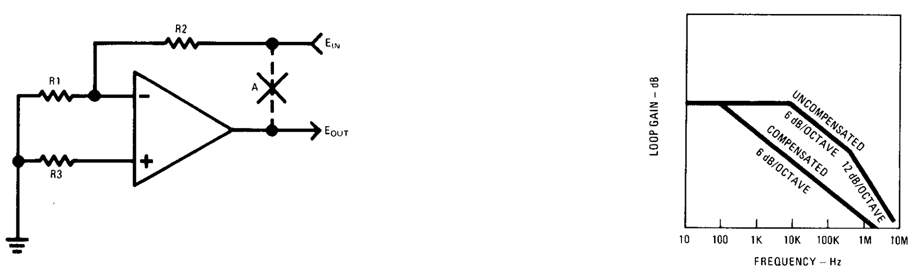
The circuit has 1-percent accuracy for input voltages between 0.5 and 50V. For lower input voltages, A1 and A3 must have their offsets balanced out individually.

FREQUENCY COMPENSATION HINTS

The ease of designing with operational amplifiers sometimes obscures some of the rules which must be followed with any feedback amplifier to keep it from oscillating. In general, these problems stem from stray capacitance, excessive capacitive loading, inadequate supply bypassing or improper frequency compensation.

In frequency compensating an operational amplifier, it is best to follow the manufacturer's recommendations. However, if operating speed and frequency response is not a consideration, a greater stability margin can ususally be obtained by increasing the size of the compensation capacitors. For example, replacing the 30 pF compensation capacitor on the LM101 with a 300 pF capacitor will make it ten times less susceptible to oscillation problems in the unity-gain connection. Similarly, on the LM709, using 0.05 μF, 1.5 kΩ, 2000 pF and 51Ω components instead of 5000 pF, 1.5 kΩ, 200 pF and 51Ω will give 20 dB more stability margin. Capacitor values less than those specified by the manufacturer for a particular gain connection should not be used since they will make the amplifier more sensitive to strays and capacitive loading, or the circuit can even oscillate with worst-case units.

The basic requirement for frequency compensating a feedback amplifier is to keep the frequency roll-off of the loop gain from exceeding 12 dB/octave when it goes through unity gain. Figure 12a shows what is meant by loop gain. The feedback loop is broken at the output, and the input sources are replaced by their equivalent impedance. Then the response is measured such that the feedback network is included.



a. Measuring Loop Gain

b. Typical Response

FIGURE 12. Illustrating Loop Gain

Figure 12b gives typical responses for both uncompensated and compensated amplifiers. An uncompensated amplifier generally rolls off at 6 dB/octave, then 12 dB/octave and even 18 dB/octave as various frequency-limiting effects within the amplifier come into play. If a loop with this kind of response were closed, it would oscillate. Frequency compensation causes the gain to roll off at a uniform 6 dB/octave right down through unity gain. This allows some margin for excess rolloff in the external circuitry.

Some of the external influences which can affect the stability of an operational amplifier is shown in Figure 13. One is the load capacitance which can come from wiring, cables or an actual capacitor on the output. This capacitance works against the output impedance of the amplifier to attenuate high frequencies. If this added rolloff occurs before the loop gain goes through zero, it can cause instability. It should be remembered that this single rolloff point can give more than 6 dB/octave rolloff since the output impedance of the amplifier can be increasing with frequency.

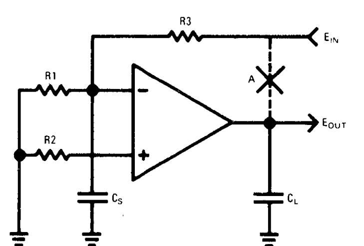


FIGURE 13. External Capacitances That Affect Stability

A second source of excess rolloff is stray capacitance on the inverting input. This becomes extremely important with large feedback resistors as might be used with an FET-input amplifier. A relatively simple method of compensating for this stray capacitance is shown in Figure 14: a lead capacitor, C1, put across the feedback resistor. Ideally, the ratio of the stray capacitance to the lead capacitor should be equal to the closed-loop gain of the amplifier. However, the lead capacitor can be made larger as long as the amplifier is compensated for unity gain. The only disadvantage of doing this is that it will reduce the bandwidth of the amplifier. Oscillations can also result if there is a large resistance on the non-inverting input of the amplifier. The differential input impedance of the amplifier falls off at high frequencies (especially with bipolar input transistors) so this resistor can produce troublesome rolloff if it is much greater than 10K, with most amplifiers. This is easily corrected by bypassing the resistor to ground.

When the capacitive load on an integrated amplifier is much greater than 100 pF, some consideration must be given to its effect on stability. Even though the amplifier does not oscillate readily, there may be a worst-case set of conditions under which it will. However, the amplifier can be stabilized for any value of capacitive loading using the circuit

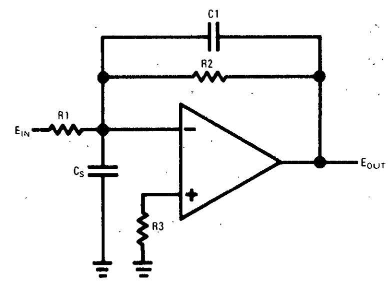


FIGURE 14. Compensating Stray Input Capacitance

shown in Figure 15. The capacitive load is isolated from the output of the amplifier with R4 which has a value of 50Ω to 100Ω for both the LM101 and the LM709. At high frequencies, the feedback path is through the lead capacitor, C1, so that the lag produced by the load capacitance does not cause instability. To use this circuit, the amplifier must be compensated for unity gain, regardless of the closed loop dc gain. The value of C1 is not too important, but at a minimum its capacitive reactance should be one-tenth the resistance of R2 at the unity-gain crossover frequency of the amplifier.

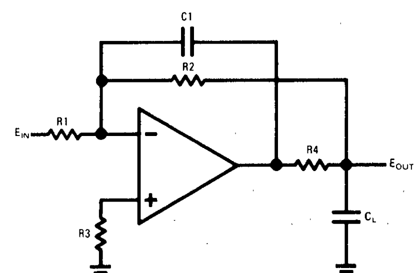


FIGURE 15. Compensating for Very Large Capacitive Loads

When an operational amplifier is operated open loop, it might appear at first glance that it needs no frequency compensation. However, this is not always the case because the external compensation is sometimes required to stabilize internal feedback loops.

The LM101 will not oscillate when operated open loop, although there may be problems if the capacitance between the balance terminal on pin 5 and the output is not held to an absolute minimum. Feedback between these two points is regenerative if it is not balanced out with a larger feedback capacitance across the compensation terminals. Usually a 3 pF compensation capacitor will completely eliminate the problem. The LM709 will oscillate when operated open loop unless a 10 pF capacitor is connected across the input compensation terminals and a 3 pF capacitor is connected on the output compensation terminals.

Problems encountered with supply bypassing are insidious in that they will hardly ever show up in a Nyquist plot. This problem has not really been thoroughly investigated, probably because one sure cure is known: bypass the positive and negative supply terminals of each amplifier to ground with at least a 0.01 μF capacitor.

For example, a LM101 can take over 1 mH inductance in either supply lead without oscillation. This should not suggest that they should be run without bypass capacitors. It has been established that 100 LM101's on a single printed circuit board with common supply busses will oscillate if the supplies are not bypassed about every fifth device. This happens even though the inputs and outputs are completely isolated.

The LM709, on the other hand, will oscillate under many load conditions with as little as 18 inches of wire between the negative supply lead and a bypass capacitor. Therefore, it is almost essential to have a set of bypass capacitors for every device.

Operational amplifiers are specified for power supply rejection at frequencies less than the first break frequency of the open loop gain. At higher frequencies, the rejection can be reduced depending on how the amplifier is frequency compensated. For both the LM101 and LM709, the rejection of high frequency signals on the positive supply is excellent. However, the situation is different for the negative supplies. These two amplifiers have compensation capacitors from the output down to a signal point which is referred to the negative supply, causing the high frequency rejection for the negative supply to be much reduced. It is therefore important to have sufficient bypassing on the negative supply to remove transients if they can cause trouble appearing on the output. One fairly large (22 μF) tantalum capacitor on the negative power lead for each printed-circuit card is usually enough to solve potential problems.

When high-current buffers are used in conjunction with operational amplifiers, supply bypassing and decoupling are even more important since they can feed a considerable amount of signal back into the supply lines. For reference, bypass capacitors of at least 0.1 μF are required for a 50 mA buffer.

When emitter followers are used to drive long cables, additional precautions are required. An emitter follower by itself – which is not contained in a feedback loop – will frequently oscillate when connected to a long length of cable. When an emitter follower is connected to the output of an operational amplifier, it can produce oscillations that will persist no matter how the loop gain is compensated. An analysis of why this happens is not very enlightening, so suffice it to say that these oscillations can usually be eliminated by putting a ferrite bead[8] between the emitter follower and the cable.

Considering the loop gain of an amplifier is a valuable tool in understanding the influence of various factors on the stability of feedback amplifiers. But it is not too helpful in determining if the amplifier is indeed stable. The reason is that most problems in a well-designed system are caused by secondary effects – which occur only under certain conditions of output voltage, load current, capacitive loading, temperature, etc. Making frequency-phase plots under all these conditions would require unreasonable amounts of time, so it is invariably not done.

A better check on stability is the small-signal transient response. It can be shown mathematically that the transient response of a network has a one-for-one correspondence with the frequency domain response.† The advantage of transient response tests is that they are displayed instantaneously on an oscilloscope, so it is reasonable to test a circuit under a wide range of conditions.

Exact methods of analysis using transient response will not be presented here. This is not because these methods are difficult, although they are. Instead, it is because it is very easy to determine which conditions are unfavorable from the overshoot and ringing on the step response. The stability margin can be determined much more easily by how much greater the aggravating conditions can be made before the circuit oscillates than by analysis of the response under given conditions. A little practice with this technique can quickly yield much better results than classical methods even for the inexperienced engineer.

SUMMARY

A number of circuits using operational amplifiers have been proposed to show their versatility in circuit design. These have ranged from low frequency oscillators through circuits for complex analog computation. Because of the low cost of monolithic amplifiers, it is almost foolish to design dc amplifiers without integrated circuits. Moreover, the price makes it practical to take advantage of operational-amplifier performance in a variety of circuits where they are not normally used.

Many of the potential oscillation problems that can be encountered in both discrete and integrated operational amplifiers were described, and some conservative solutions to these problems were presented. The areas discussed included stray capacitance, capacitive loading and supply bypassing. Finally, a simplified method of quickly testing the stability of amplifier circuits over a wide range of operating conditions was suggested.

†The frequency-domain characteristics can be determined from the impulse response of a network and this is directly relatable to the step response through the convolution integral.

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May 1968

A FAST INTEGRATED VOLTAGE FOLLOWER WITH LOW INPUT CURRENT

INTRODUCTION

Most integrated operational amplifiers on the market today have serious limitations in many voltage follower applications. They are often too slow because a voltage follower requires maximum frequency compensation, reducing slew rate to somewhere between 0.1 V/µs and 1 V/µs.[1,2] Secondly, voltage followers are most frequently used as buffer amplifiers from high impedance sources; but the input current of popular amplifiers gives excessive dc offset when operated with source resistances much above 10 KΩ.

The design of a monolithic voltage follower which combines low offset voltage with an input current of 2 nA and a 10 V/µs slew rate is described here. This performance is realized using improved bipolar transistors along with an operational amplifier circuit design which is optimized for the voltage follower configuration. The device, which is designed to operate from supply voltages between ±12V and ±15V, features a 10 MHz bandwidth along with a 3 pF input capacitance and a minimum input resistance of 10,000 MΩ. In addition, it requires no external components for frequency compensation and incorporates continuous short circuit protection.

CIRCUIT DESCRIPTION

There are fewer problems encountered in designing a high performance voltage follower than a similar general purpose amplifier. For one, no level shifting is required so complementary transistors are unnecessary as gain stages. Hence, it is possible to get better high frequency performance since this has been limited in the past by the performance of the PNP[3] transistors that can be made in monolithic circuits. Secondly, because 100-percent feedback is used, the open loop gain does not have to be as high as a general purpose amplifier; so a simpler circuit, which is easier to frequency compensate, can be used. Finally, with a fixed configuration such as a voltage follower, the input stage can be included within the compensation network. This makes it easier to get fast slewing without having to provide unreasonably large small-signal bandwidths which would make the amplifier more prone to instabilities.

Figure 1 demonstrates how simple a voltage follower circuit can be. This circuit uses a single-stage differential amplifier with an emitter-follower output. Since current sources are used on the emitter of the differential pair and as a collector load, it is practical to get an open loop voltage gain of 3000 from a single stage. The collector of the input transistor, Q1, is bootstrapped to the output to increase gain and raise the input resistance. It also eliminates leakage currents by operating the input at zero collector-base voltage. A class-A output stage is used since it behaves better at high frequencies with capacitive loads. Although frequency compensation is not always required with this configuration, R1 and C1 have been included to improve stability with capacitive loading. The compensation network is placed such that the circuit has good transient rejection on both the positive and the negative supplies.

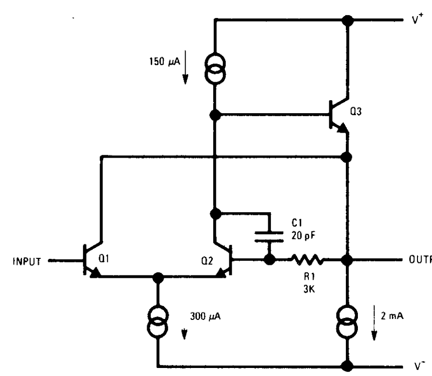


FIGURE 1. Basic Configuration of the Voltage Follower

INPUT STAGE

In order to get fast slewing, it is necessary to operate the differential amplifier at a fairly high current for an input stage. Therefore, a Darlington connection is used on the input transistors to get low input current. However, as can be seen from Figure 2, bleed resistors, R1 and R2, operate the input transistors at a current which is large by comparison to the base current of Q3 and Q4. This keeps Q1 and Q2 from seeing mismatches in the base currents of Q3 and Q4, which is the largest source of offset voltage in an ordinary Darlington differential stage. This bleed current also doubles the gain of the stage and improves the high frequency performance.

Using a Darlington stage is not the entire secret to getting low input currents.[4] With the integrated circuit transistors that have been available in the past, reducing the collector current by a factor of 10 would only reduce the base current by a factor of 3, since the current gain falls off rapidly at low collector currents. In order to get any real improvement from operating at low currents, it was necessary to make better transistors. The devices used here have a typical current gain of 1000 at 2 μA collector current.

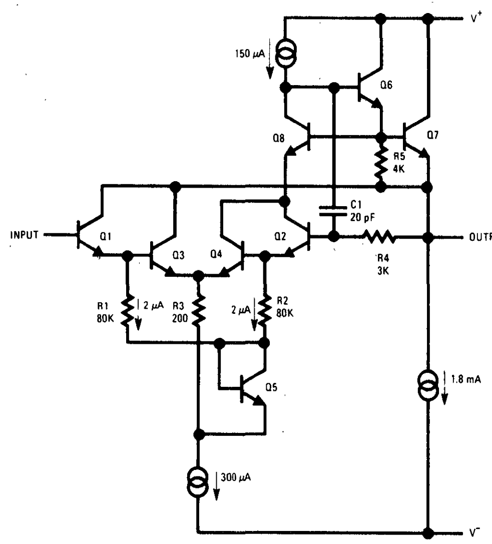


FIGURE 2. Partial Schematic of the LM102 Voltage Follower

Operating at 2 μA currents requires large resistance values which are not easily fabricated in integrated circuits. Therefore, the bleed circuit on the input stage had to be designed to minimize this resistance. R1 and R2 are operated with a 160 mV drop across them, which is determined by the drop across R3 plus the emitter-base voltage difference between Q5 and the differential transistors, Q3 and Q4. This difference is 100 mV since the differential transistors are operated at roughly 35 times the current through Q5.[5]

Pinch resistors had to be used for R1 and R2 to get 80 KΩ within a reasonable surface area. They were also necessary to keep the parasitic capacitance of the resistors small, as it could severely degrade the large signal pulse response. However, pinch resistors have a large positive temperature coefficient which causes the operating current of Q1 and Q2 to increase to 3.5 μA at -55°C and decrease to 1.4 μA at 125°C.

Figure 2 shows that an extra transistor, Q8, has been added on the collectors of Q2 and Q4. This forms a cascode stage which operates Q2 at near zero collector base voltage, as is Q1. An additional emitter follower is included on the output to further reduce output resistance.

BIASING CIRCUITRY

Figure 3 is a simplified schematic of the biasing circuitry which is represented by current sources in Figures 1 and 2. In order to realize low offset voltage, the current source on the collector of Q2 must supply a current which is exactly one-half of the input pair emitter current.

To do this, diode-connected transistors, Q14 and Q15, provide a bias voltage which is regulated against supply voltage variations for the current source transistors, Q10, Q12 and Q13. Q12 is the current source for the input pair, while Q13 generates a current which is one-half the output current of Q12. This is accomplished by making R9 twice as large as R8 and Q13 one-half the size of Q12. The output current of Q13 is fed to Q18, which biases Q19. If it is assumed that Q18 and Q19 are well matched and have large current gains, the output current of Q19 will be equal to the collector current of Q13 – or one-half the emitter current of the input pair, as required.

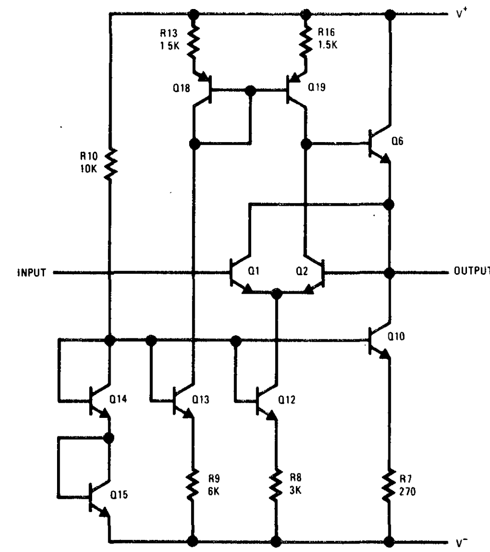


FIGURE 3. Simplified Schematic of Biasing Circuitry

ADDITIONAL DETAILS

In practice, it cannot be assumed that the current gain of the PNP transistors, Q18 and Q19, is large.[6] In fact, the current gain could be as low as unity. As a result, additional circuitry is required to get proper operation. Figure 4 shows how this is done.

Instead of connecting the base directly back to the collector, emitter follower buffers, Q16 and Q17, are used to isolate the base current from the collector of Q18. Level shifting diodes, D1 and D2, are included so that Q18 is operated at approximately the same collector base voltage as Q19, when the output of the amplifier is at zero, further improving the match.

The RC network, R11 and C2, is included to suppress oscillations in this feedback loop. The voltage drop across C2 is less than a couple of volts so a junction capacitor can be fabricated from the emitter and base diffusions of the NPN transistors. With this, the required capacitance can be obtained in a reasonable area of the chip with no additional process steps, as would be required if an MOS capacitor were used. The same is true, incidentally, for C1.

A class-A output stage is used primarily for simplicity, although the higher quiescent current in the output stage improves stability with capacitive loads. The emitter of the current sink, Q10, is brought out so that an external resistor can be connected between it and the negative supply for increased output current in applications where the

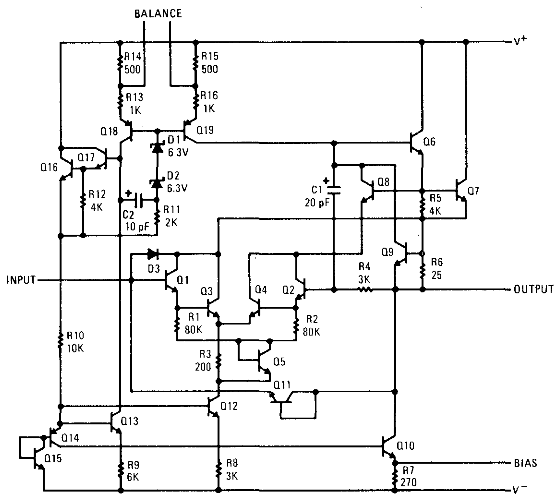


FIGURE 4. Complete Schematic Diagram

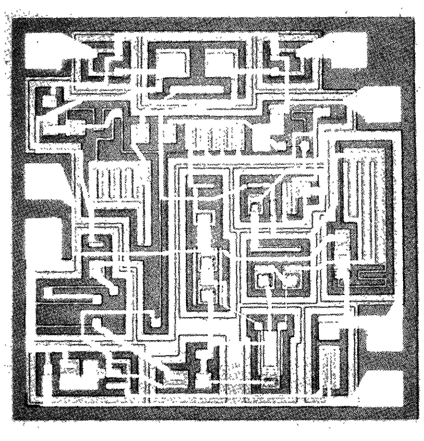


FIGURE 5. Photomicrograph of the LM102

higher dissipation can be tolerated. The current source is biased from the collector of a low gain lateral PNP transistor, Q14, so that the bias voltage for the input stage current sources will not be greatly affected when Q10 saturates on negative signals.

Resistors are included in series with the emitters of the PNP current source transistors, Q18 and Q19, to reduce their output conductance, thereby increasing gain. Taps on these resistors are brought out to provide for offset balancing. The tap point is selected to give a smooth ±20 mV adjustment range when a 1K potentiometer is connected between the balance terminals and the positive supply.

The output is inherently short-circuit proof in the negative direction. Current limiting for positive outputs is provided by Q9 and R6. However, when operating from low source resistances, a 2 KΩ to 10 KΩ resistor must be added in series with the input, since the input is clamped directly to the output through D3 and Q11 which protect the input transistors from overvoltage. This resistor was not included on the chip because it is difficult to locate a diffused resistor in an isolation region where it would be effective yet not contribute to input leakage current at high temperatures.

A photomicrograph of the LM102 is shown in Figure 5. Although the schematic diagram of the circuit appears complicated, it fits neatly on a 49 x 49 mil-square die.

PERFORMANCE

The electrical characteristics of the LM102 are summarized in Table I. It is evident from this that the primary design objectives, high speed and low input current, have indeed been achieved.

Offset Voltage	2.5 mV
Input Current	3 nA
Input Resistance	$10^{12}\Omega$
Voltage Gain	0.9995
Output Resistance	1.0Ω
Output Voltage Swing	±13V
Slew Rate	10 V/µs
Bandwidth	10 MHz
Input Capacitance	3 pF
Supply Current	3.5 mA

TABLE I. Typical Electrical Characteristics of the LM102

The low input bias current of the voltage follower is illustrated in Figure 6. It can be seen that the input current reaches a minimum at 85°C but remains low up to 125°C. This suggests operating the LM102 in a temperature stabilized component oven for wide temperature range applications. If this is done, the LM102 will give input currents which are considerably better than can be realized with FET amplifiers over a -55°C to 125°C temperature range. In addition, the temperature stabilization will greatly reduce the offset voltage drift.

Figure 7 is a plot of the frequency response of the LM102. The low frequency gain figure corresponds to an open loop gain of about 2000. Although this sounds low for an operational amplifier, it should be remembered that a voltage follower has 100-percent feedback so the gain error is only 0.05-percent. Further, because of its

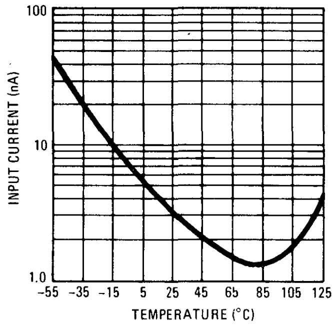


FIGURE 6. Input Bias Current

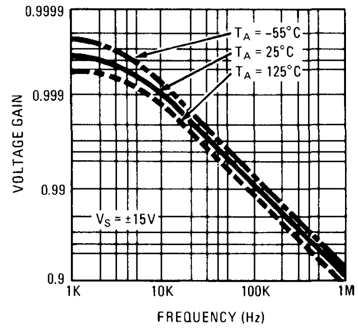


FIGURE 7. Voltage Gain at Moderate Frequencies

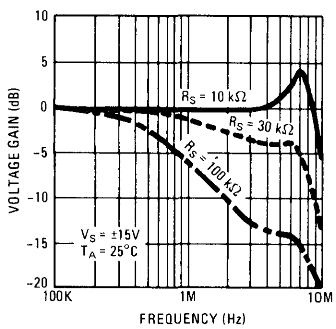


FIGURE 8. High Frequency Response

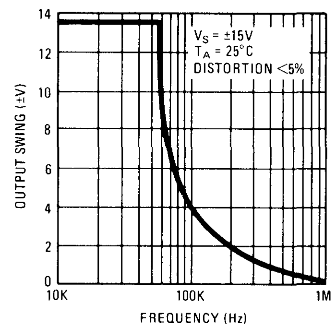


FIGURE 9. Frequency Limited Output Swing

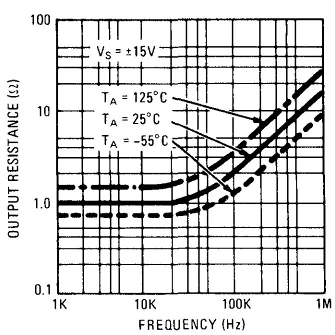


FIGURE 10. Output Resistance

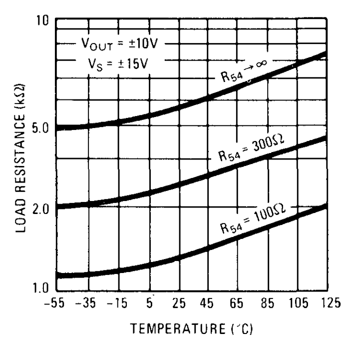


FIGURE 11. Minimum Load Resistance for Rated Output Swing

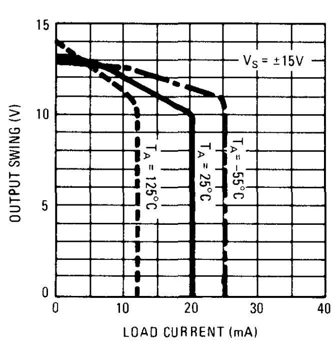


FIGURE 12. Positive Current Limiting

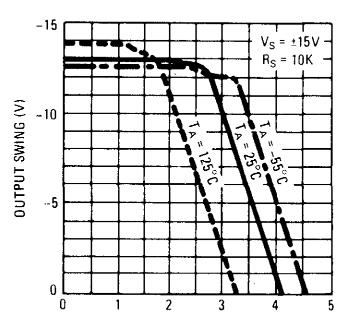


FIGURE 13. Negative Current Limiting

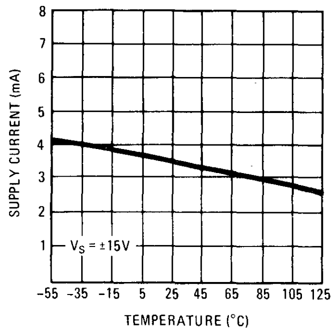


FIGURE 14. Supply Current

better high frequency response, the LM102 actually has 10 times more gain than either the LM101 or the LM709 at frequencies greater than 10 kHz. The gain of all these amplifiers is equal at 500 Hz.

It is difficult to measure the low frequency gain of a voltage follower directly because the gain error is so small. However, it can be accomplished by grounding the input of the amplifier and driving both power supplies simultaneously with the desired input signal. The amplifier error can then be observed directly on the output.

Figure 8 gives the response of the amplifier at frequencies up to 10 MHz. With a 10K source resistance, the bandwidth is nearly 10 MHz. Some peaking is evident, although it is not serious. At higher source resistances, the bandwidth is reduced by the 3 pF input capacitance as shown in the figure.

Feedback amplifiers generally have a full-signal bandwidth which is considerably less than the small signal bandwidth. The LM102 is no exception. It can only deliver its rated output swing at frequencies less than 60 kHz, as shown in Figure 9.

There is no standard way of measuring the frequency limited output swing,[7] but the criterion used here was that the total harmonic distortion be less than 5-percent.

The output resistance of the follower is about 1Ω as shown in Figure 10. This gives a gain error less than 0.01-percent with load resistances above 10K. At high frequencies as well as high temperatures, the output resistance increases because the open loop gain of the amplifier falls off.

INCREASED OUTPUT SWING

Figure 11 illustrates the function of the booster terminal on the output stage current sink. By itself, the amplifier can only deliver its rated ±10V output swing into load resistances greater than 5.7 KΩ at 25°C. With heavier loads, it will clip in the negative direction. A 300Ω resistor between pins 5 and 4 extends the drive capability to 2.5K while a 100Ω resistor will enable the amplifier to give a ±10V swing with 1.4K loads. The figure also shows the effect of temperature on the drive capability.

It should be remembered that increasing the drive current will increase dissipation in the microcircuit. For example, when the amplifier is set up to drive ±10V into a 2K load at 125°C, the worst case dissipation increase will be 150 mW (for a steady +10V output with load).

Figures 12 and 13 show the current limiting characteristics of the LM102. Figure 12, which gives the positive output level as a function of load current demonstrates the sharpness of the current limiting. The short circuit current also drops as the chip heats up, reducing power dissipation.

Figure 13 gives the limiting characteristics in the negative direction. The circuit begins to limit at lower currents since the available current is determined by a fixed-current source. It should be noted that after the output swing first starts to fall off, further increases in load current are supplied by the input through the protective clamp diodes, D3 and Q11.

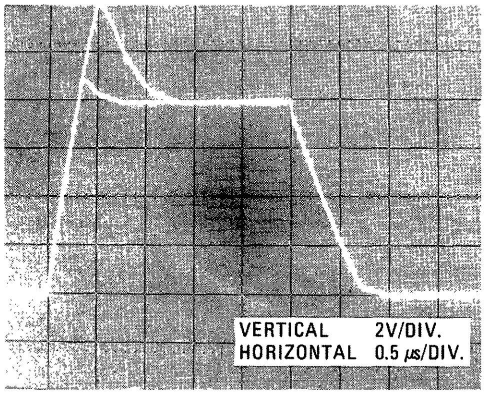
Figure 14 is a plot of the current drain over a -55°C to 125°C temperature range. The supply current does not increase appreciably over the entire output voltage range, including saturation. It is evident here that fast operation is obtained in the follower without excessive power dissipation.

SLEWING

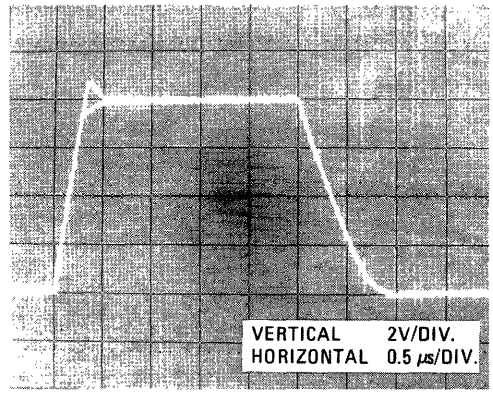
The fast slewing of the follower is demonstrated in Figure 15. A fairly large overshoot is evident for positive-going input signals above about 4V. As shown in the figure, this can be eliminated by using a high speed clamp diode between the input and the output (with the anode on the input). Although there is an internal clamp diode in this position (D3 in Figure 4), it is of necessity a collector base diode which stores excess charge when it turns on with input signals which rise faster than the output can follow. This stored charge causes the overshoot.

If the LM102 is driven from source resistances higher than 30K, the leading edge of the input pulse will always be slowed down enough by the input capacitance that the output can follow the input and the clamp diode is not needed. This is shown in Figure 15a.

Figure 15b demonstrates that the slew rate is about 10 V/µs in the slowest direction even including the effects of overshoot. But because of its restricted output current swing in the negative direction, the device will not give this slew rate with capacitive loads greater than 100 pF unless the output sink

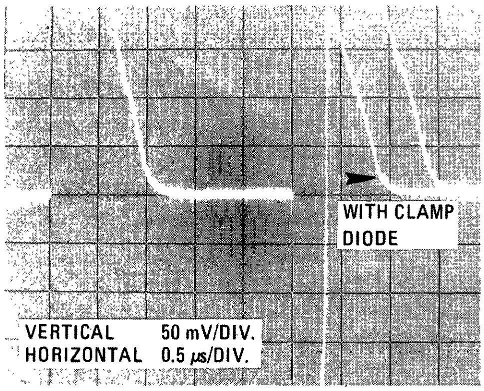


a. 3K Source Resistance

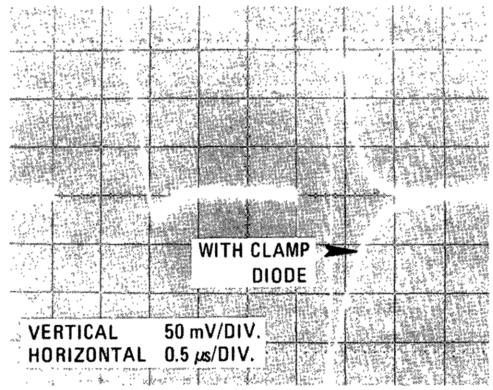


b. 30K Source Resistance

FIGURE 15. Large Signal Pulse Response With and Without a Clamp Diode



a. 3K Source Resistance



b. 30K Source Resistance

FIGURE 16. Error Signal for 8V Input Pulse — With and Without a Clamp Diode

current is increased with an external resistor on the booster terminal.

Figure 16 illustrates the fact that the settling time of the LM102 to within 5 mV of its final value is less than 1.5 μs for an 8V input pulse. These photographs show the error signal, which is the difference between the input and the output, with a ±4V rectangular pulse applied.

STABILITY

Figures 17 through 19 are indicative of the stability of the amplifier under varying conditions of capacitive loading, temperature and supply bypassing.[8] Figure 17 gives the small signal transient response with capacitive loading. These pictures were taken with both supplies bypassed to ground with 0.01 μF ceramic capacitors. With loads approaching 200 pF, the circuit tends toward instability. With capacitive loads much above this it will oscillate, although it will be stable again with more than 0.01 μF on the output. With the larger capacitances, however, both the small signal risetime and the slew rate will be reduced.

Figure 18 shows how the stability is affected over a -55°C to +125°C temperature range. Again, the conditions here are 200 pF capacitive load with bypassed supplies.

The effect of unbypassed supplies is demonstrated in Figure 19. The response was measured under the same conditions as Figure 17, except that there is 16″ of wire between the device and the bypass capacitors on the power supply. It is evident that the circuit is on the verge of becoming unstable with capacitive loading. This clearly proves the advisability of properly bypassing the supplies on any high frequency amplifier.

OPERATING HINTS

A number of precautions concerning the proper use of the LM102 have already been given along with hints on optimizing the performance in certain applications. These are worth repeating here.

- The output is short circuit protected; however, the input is clamped to the output to prevent excessive voltage from being developed across the input transistors. If the amplifier is driven from low source impedances, excessive current can flow through these clamp diodes when the output is shorted. This can be prevented by inserting a resistor larger than 3 KΩ in series with the input.

- The circuit cannot deliver its full slew rate into capacitive loads greater than 100 pF unless more sink current is provided on the output with a resistor between pins 4 and 5.

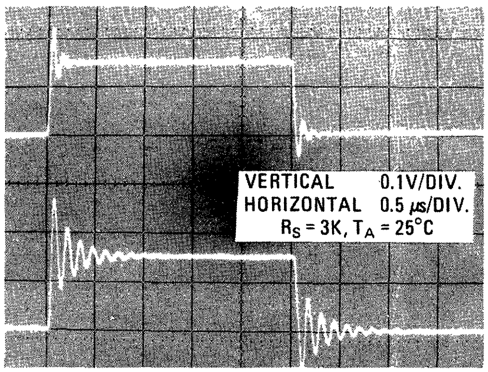


FIGURE 17. Small Signal Transient Response for C_L = 10 pF (Top) and C_L = 200 pF (Bottom)

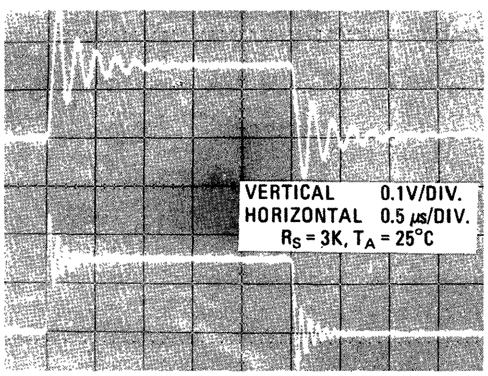


FIGURE 18. Transient Response for C_L = 200 pF at 125°C (Top) and –55°C (Bottom)

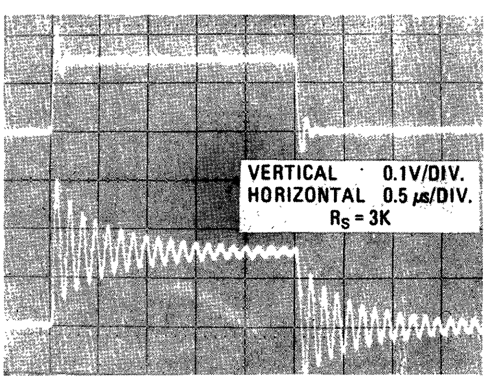


FIGURE 19. Transient Response With Unbypassed Supplies, C_L = 10 pF (Top) and C_L = 200 pF (Bottom)

- The amplifier may oscillate when operated with capacitive loads between 200 pF and 0.01 μF.

- As is the case with any high frequency amplifier, the power supply leads of the LM102 should be bypassed with capacitors greater than 0.01 μF located as close as possible to the device. This is particularly true if it is driving capacitive loads.

Figure 20a gives the connection for getting full output swing into loads less than 8K. The external resistor, R1, should not be made less than 100Ω as this could cause limiting on positive peaks. Figure 20b shows how to connect a potentiometer to balance out the offset voltage. Figure 20c gives the placement of a clamp diode which can be used to reduce the overshoot that occurs when the follower is driven with large input pulses with a leading-edge slope greater than 10 V/μs. The diode is only needed, however, when the source resistance is less than 30K since the slope seen by the amplifier will be reduced by the input capacitance with the higher source resistances.

APPLICATIONS*

The use of the LM102 in a switch circuit for driving the ladder network in an analog to digital converter is shown in Figure 21. Simple transistor switches, connected in the reverse mode for low saturation voltage, generate the 0V and 5V levels for the ladder network. The switch output is buffered by A2 and A3 to give a low driving impedance in both the high and low states.

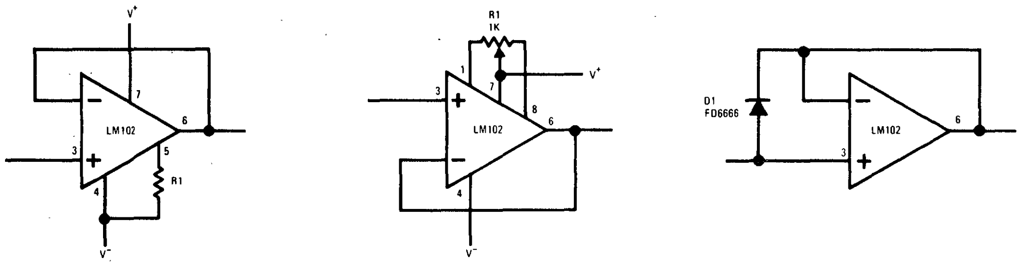
The switch transistors can be driven directly from integrated logic circuits. Resistors R7 and R8 limit the base drive; the values indicated are for operation with standard TTL or DTL circuits. If necessary, the switching speed can be increased somewhat by bypassing the resistors with 100 pF capacitors.

Even with operation at maximum speed, clamp diodes are not needed on the voltage followers to reduce overshoot. The pullup resistors on the switches, R5 and R6, can be made large enough so that the LM102 does not see a positive-going input pulse that is much faster than the output slew rate.

The main advantage of this circuit is that it gives much lower output resistance than push-pull switches. Furthermore, the drive circuitry for these switches is considerably simpler.

The LM102 can also be used as a buffer for the temperature compensated voltage reference, as shown in Figure 21. The output of the reference diode is divided down with a resistive divider, and it can be set to the desired value with R3.

*Other applications are given in reference 8.



a. For Increased Swing   b. For Offset Balancing   c. For Eliminating Overshoot

FIGURE 20. Auxiliary Circuits for the LM102

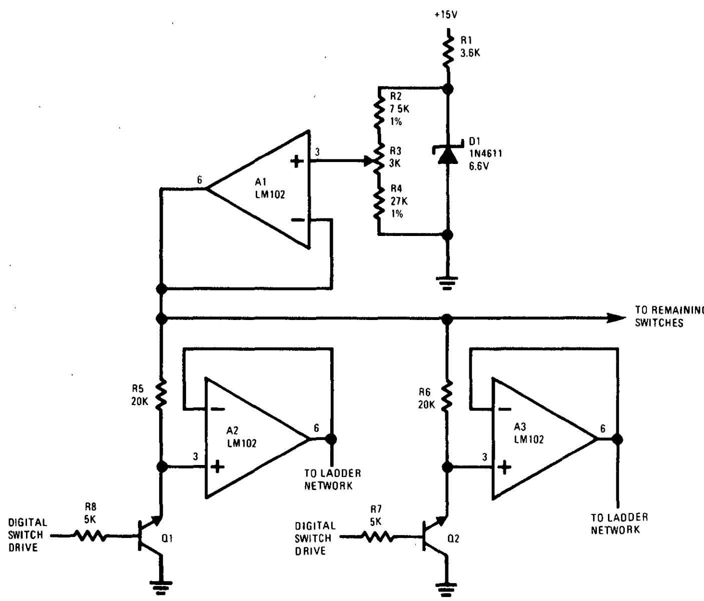


FIGURE 21. Using the LM102 to Drive the Ladder Network in an A/D Converter

ANALOG COMMUTATOR

The low input current and fast slewing of the LM102 make it well suited as a buffer amplifier in high speed analog commutators. The low input current permits operation with switch resistances even higher than 10 KΩ without affecting the dc stability.

Figure 22 shows an expandable four-channel analog commutator. Two DM7501 dual flip flops form a four-bit static shift register. The parallel outputs drive DM7800 level translators which convert the TTL logic levels to voltages suitable for driving MOS devices, and this is coupled into an MM451 four-channel analog switch. An extra gate on the input of the translator can be used, as shown, to shut off all the analog switches.

In operation, a bit enters the register and cycles through at the clock frequency, turning on each analog switch in sequence. The "clear" input is used to reset the register such that all analog switches are off. The channel capacity can be expanded by connecting registers in series and hooking the output of additional analog switches to the input of the buffer amplifiers.

When the output of a large number of MOS switches are connected together, the capacitance on the output node can become high enough to reduce accuracy at a given operating speed. This problem can be avoided, however, by breaking up the total number of channels, buffering these segments with voltage followers and then subcommutate them into the A/D converter.

SAMPLE AND HOLD

Although there are many ways to make a sample and hold device, the circuit shown in Figure 23 is

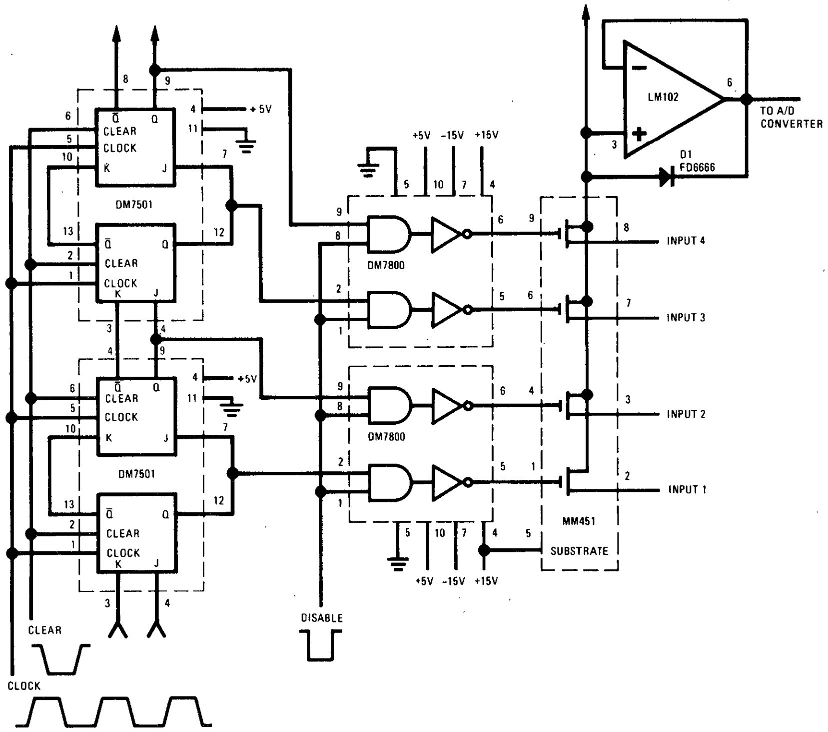


FIGURE 22. Analog Commutator With Buffered Output

undoubtedly one of the simplest. When a negative going sample pulse is applied to the MOS switch, it will turn on hard and charge the holding capacitor to the instantaneous value of the input voltage. After the switch is turned off, the capacitor is isolated from any loading by the LM102; and it will hold the voltage impressed upon it.

The maximum input current of the LM102 is 10 nA, so with a 10 μF holding capacitor the drift rate in hold will be less than 1 mV/sec. If accuracies of about 1-percent or better are required, it is necessary to use a capacitor with polycarbonate, polyethylene or teflon dielectric. Most other capacitors exhibit a polarization phenomenon[9] which causes the stored voltage to fall off after the sample interval with a time constant of several seconds. For example, if the capacitor is charged from 0 to 5V during the sample interval, the magnitude of the falloff is about 50 to 100 mV.

AC AMPLIFIER

The LM102 has a minimum input resistance of 10,000 MΩ, so for dc amplifier applications this can be completely neglected. However, with an ac coupled amplifier a biasing resistor must be used to supply the input current. This drastically reduces the input resistance.

Figure 24 illustrates a method of bootstrapping the bias resistor to get higher input resistance. Even though a 200 KΩ bias resistor is used for good dc stability, the input resistance is about 12 MΩ at 100 Hz, increasing to 100 MΩ at 1 kHz.

ACTIVE FILTERS

Active RC filters have been replacing passive LC filters at an ever-increasing rate because of the declining price and smaller size of active components. Figure 25 is a low-pass filter which is one of the simplest forms of active filters. The circuit has the filter characteristics of two isolated RC filter sections and also has a buffered, low-impedance output.

The attenuation is roughly 12 dB at twice the cutoff frequency and the ultimate attenuation is 40 dB/decade. A third low-pass RC section can be added on the output of the amplifier for an ultimate attenuation of 60 dB/decade,[10] although this means that the output is no longer buffered.

There are two basic designs for this type of filter. One is the Butterworth filter with maximally flat frequency response. For this characteristic, the component values are determined from[11]

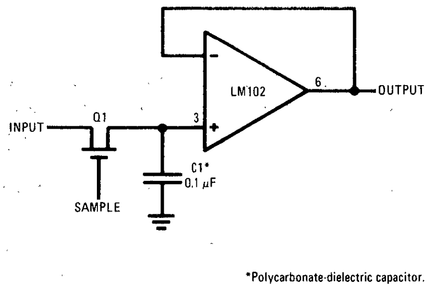


FIGURE 23. Sample and Hold Circuit

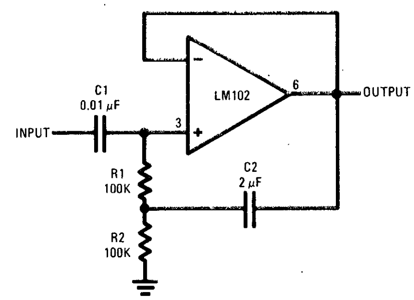


FIGURE 24. High Input Impedance ac Amplifier

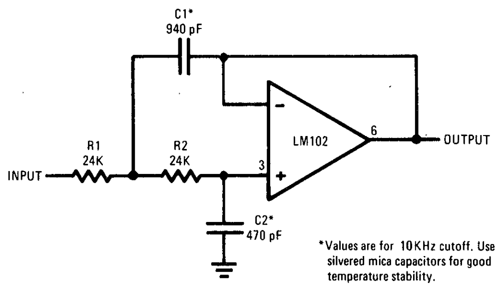


FIGURE 25. Low Pass Active Filter

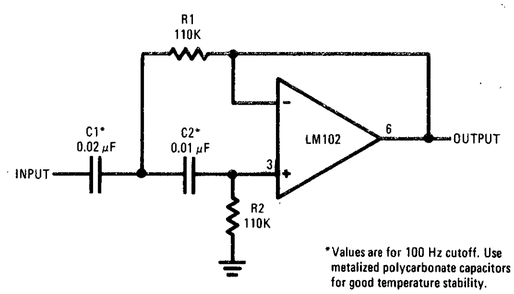


FIGURE 26. High Pass Active Filter

$$C1 = \frac{R1 + R2}{\sqrt{2}\, R1R2\omega_C}$$

and

$$C2 = \frac{\sqrt{2}}{(R1 + R2)\, \omega_C}.$$

The second kind is the linear phase filter with minimum settling time for a pulse input. The design equations for this are

$$C1 = \frac{R1 + R2}{\sqrt{3}\, R1R2\omega_C}$$

and

$$C2 = \frac{\sqrt{3}}{(R1 + R2)\, \omega_C}$$

Substituting capacitors for resistors and resistors for capacitors in the circuit of Figure 25, a similar high-pass filter is obtained. This is shown in Figure 26.

CONCLUSIONS

The LM102 represents a significant advance in the state of the art of linear circuits manufacturing. The device incorporates transistors which have higher current gain than is available with discrete components. Further, a factor of three to five improvement over this can be expected in the near future.

The performance realized challenges that of field effect transistors, if operation over the military temperature range is considered. This is especially true if the components are included in a temperature-stabilized oven.

Although the circuit introduced here is restricted to voltage follower applications, many of the techniques used here can be applied to general purpose amplifiers. This is indicative of the performance that can ultimately be realized with monolithic amplifiers.

Even though it's only a voltage follower, the LM102 can be used in a wide variety of applications ranging from low drift sample and hold circuits to a buffer amplifier for high-speed analog commutators. Its usefulness is enhanced by the fact that it is a plug-in replacement for both the LM101 and the LM709 in voltage follower applications. The circuit will work in the same socket, unaffected if the compensation components for the other amplifiers are installed or not.

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March 1968

TUNED CIRCUIT DESIGN USING MONOLITHIC RF/IF AMPLIFIERS

INTRODUCTION

In replacing conventional tuned high frequency stages, monolithic RF/IF amplifiers can provide performance, as well as economic advantages. Large available gain per stage, inherent stability, self-contained biasing, and excellent limiting or AGC capabilities allow such amplifiers to improve conventional designs, while their very small chip size makes them competitive with single transistor stages.

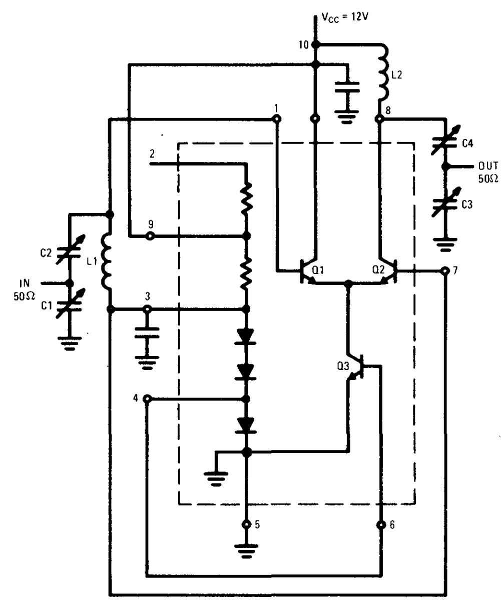

FIGURE 1. Emitter Coupled RF Amplifier

Two especially useful RF/IF amplifiers are the "emitter coupled" differential amplifier, Figure 1, and the modified "cascode", Figure 2. Emitter coupled operation is advantageous because of its symmetrical, non-saturated limiting action, and corresponding fast recovery from large signal overdrive, making a nearly ideal FM IF stage. The "cascode" combines the large available stable gain and low noise figure, for which the configuration is well known, with a highly effective remote gain control capability, via a second common-base stage, which overcomes many of the interstage detuning and bandwidth variation problems found in conventional transistor AGC stages.

The "emitter coupled" and "cascode" configurations contain essentially the same components; they are available as either type 703 (Figure 3), which

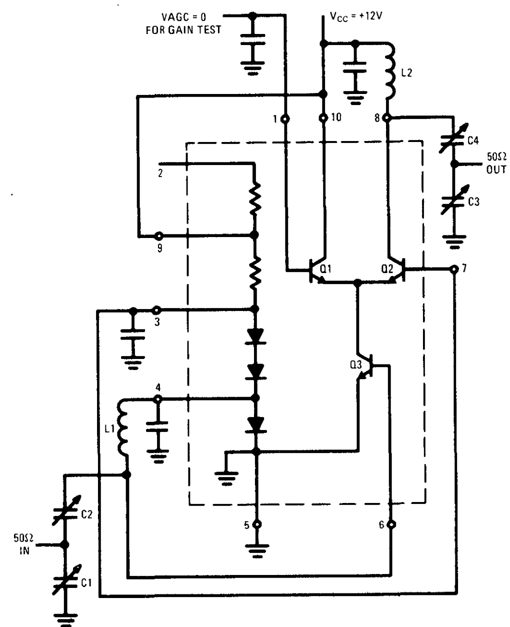

FIGURE 2. Cascode RF Amplifier

is permanently connected as an emitter coupled amplifier, in an economical six pin package, or as the more versatile type LM171 (Figure 4), in which a ten pin package allows the user to select either emitter coupled or cascode configurations. Since the 171, when externally connected as an emitter coupled amplifier, is essentially identical in performance to the 703, references will be made only to "cascode" or "emitter coupled" configurations.

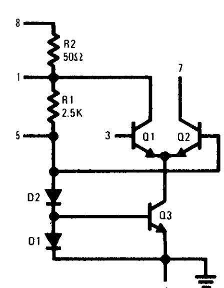

FIGURE 3. LM703 Configuration

DC Biasing

Both the 703 and 171 are biased by using the inherent match between adjacent monolithic components. They are designed for use with conventional tuned interstages, in which DC bias currents flow through the input and output tuning inductances.

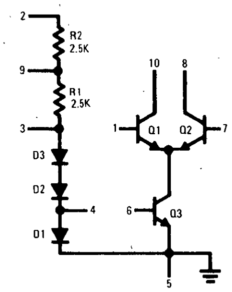

FIGURE 4. 171 Configuration

In either case, a resistor forces DC current from the positive supply into a chain of diodes (two for the 703, three for the 171), proportional to the difference between supply and forward diode-chain voltages, and inversely to the value of the resistor. The forced current, I_{bias} establishes a voltage drop across the bottom diode (in reality, an NPN transistor with collector-base short), which is identical to the base-emitter voltage required to force a collector current of I_{bias} in a matched common-emitter stage. Since the transistor is monolithically matched to the bottom diode, and of fairly high DC "beta", an efficient, reliably biased current source is created.

Total current through an NPN differential pair is determined by the current source, while current "split" depends on the differential base voltage. Common-mode base voltage is readily available by using the tap at the top of the diode chain. In the 703, the differential emitters operate at a forced voltage of one forward diode drop, V_{be}, the current source still being effective with zero volts, collector to base. Because the 171, as a cascode, requires high frequency performance of the current source, three biasing diodes are used, fixing the differential emitters at 2 V_{be}.

Both 703 and 171 function as ordinary differential amplifiers, splitting available current source drive equally, when base voltages are equal, and being capable of either complete cutoff, or full conduction of available current into one of the pair, depending on differential input. In emitter coupled service, the input signal is injected in series with the differential pair's DC bias, while, in the cascode, it is in series with the current source's base bias.

Emitter Coupled Operation

To assure symmetrical limiting, and maximum small-signal linearity, it is necessary that the differential pair be closely balanced, so that quiescent operation occurs in the center of the amplifier's transfer characteristic (Figure 5). Typical V_{be} matches better than ±0.3 mV, for both 703 and 171 assure this, provided that DC resistance of the input inductor is so low that input bias currents in the 50 μA region do not induce appreciable input offset voltages.

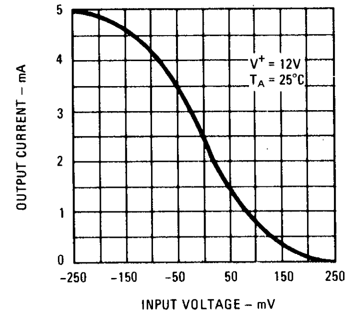

FIGURE 5. Emitter Coupled Transfer Characteristic

The transfer characteristic of Figure 5 is represented by the equation:

$$\frac{I_{(current\ source)}}{I_{(output)}} = 1 + e^{\left(\frac{qV_{IN}}{kT}\right)} \qquad (1)$$

Calculating the difference in V_{IN} required to change this ratio from 10% to 90%, it may be seen that:

$$V_{IN}\ (10\%) - V_{IN}\ (90\%) = 2\,\frac{kT}{q}\ (\ln_e 9) = 0.384T\ (mV) \qquad (2)$$

This quantity, the transition width of an emitter coupled amplifier, is independent of supply voltage and current, and proportional to absolute temperature, varying from 84 mV at −55°C to 153 mV at +125°C, and is approximately 114 mV at 25°C. Forward transconductance, however, is directly proportional to total supply current, taking the approximate form:

$$|y_{21}| = 3.6\ (I_{supply}, mA)\ \text{mmhos} \qquad (3)$$

at 25°C, 10.7 MHz, for either 703 or emitter-coupled 171. Thus, emitter coupled amplifier gain may be controlled by externally varying "bias chain" current, changing the current source by the same amount, but without affecting transition width.

Because an emitter coupled amplifier's input impedance is a function of drive level (Figure 6), interstages designed with small-signal y-parameters may exhibit center frequency shifts and bandwidth decreases as signal level increases. This is less of a problem in FM IF strips, where input signal amplitude is essentially constant, dictated by the limiting characteristics of the previous stage (Figure 7).

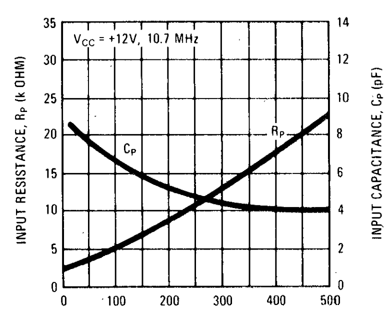

FIGURE 6. Effect of Drive Level on Emitter Coupled Input Impedance

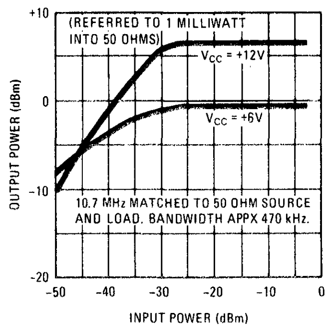

FIGURE 7. Emitter Coupled Limiting Characteristics

Cascode Operation

The cascode configuration exhibits the same input characteristics as a common-emitter stage, and nearly the same output characteristics, but has superior available gain and stability; thus, it may directly replace many existing AM-IF designs. The modified cascode possible with the 171 allows the effective forward transconductance to be controlled by a small DC voltage, applied differentially between Pins 1 and 7, as in Figure 2. With the AGC input near ground, and the base of the output common-base transistor at 3 V_{be} (from the bias chain), the output transistor acts as it would in an ordinary cascode circuit. As the AGC transistor's base voltage is increased, it begins to conduct part of the available DC current and a proportional amount of signal, from the input stage. As emitter current increases in the AGC transistor, its emitter resistance decreases, while the emitter resistance of the output transistor increases proportionally; when the differential pair is balanced, output is reduced by half, and increased AGC voltage causes all DC current, as well as nearly all signal, to be shunted to the AGC transistor (Figure 8). Infinite gain reduction is not possible, because of capacitive leakages in the cut-off output transistor; nevertheless, large AGC range per stage is possible (Figure 9).

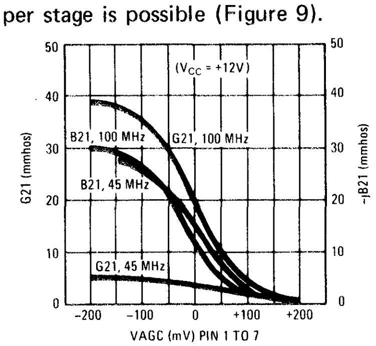

FIGURE 8. Cascode Y_{21} vs AGC

The magnitude of forward transadmittance is approximately proportional to the fraction of available DC current shunted into the output stage; it can be related to the AGC voltage by the expression:

$$|y_{21}| = \frac{(Y_o)}{\left(1 + e^{\left[\frac{q(V_{agc} - 3\,V_{be})}{kT}\right]}\right)} \text{ mmhos} \qquad (4)$$

where Y_O is the maximum (no-AGC) magnitude of y_{21} for given conditions. At 25°C, V_{CC} = 12 volts,

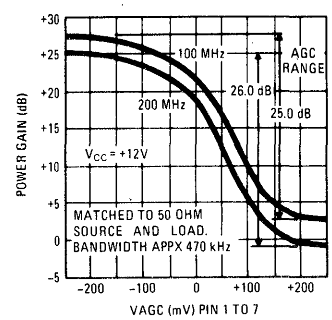

FIGURE 9. Tuned Cascode Power Gain vs AGC

and 100 MHz, for example, 171 Y_o is about 50 mmhos. From Equation (4), it may be seen that balanced conditions (V_{agc} = 3 V_{be}) result in the exponential term equaling unity, so that forward transconductance is half of its maximum value.

The combined second-stage input admittance seen by the collector of the input transistor remains essentially constant, as balance of the differential pair is varied; thus, input admittance of the cascode remains constant over a wide AGC range, allowing interstages to be sharply tuned without fear of center frequency or bandwidth shift when AGC is applied (Figure 10). Moreover, the exceptionally low reverse transconductance (.001 mmhos or less at 200 MHz) allows high-Q interstages to be aligned in an IF strip with minimal interaction between succeeding tuning operations.

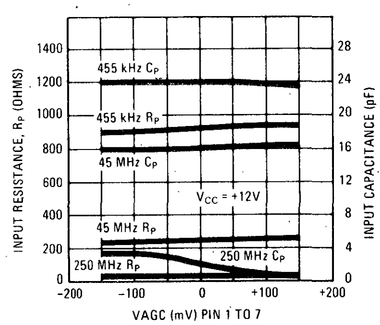

FIGURE 10. Effect of AGC on Cascode Input Impedance

Gain reduction may be accomplished with either positive-going or negative-going AGC, simply by choosing the appropriate input base of the differential pair. Approximately 200 mV peak-to-peak is sufficient to operate the AGC from full conduction to cutoff at 25°C; adjacent AGC stages may be connected with the AGC inputs in parallel, if the DC "reference" is obtained for each differential pair from a common point, such as the bias chain of one of the amplifiers. Alternatively, sensitivity to differences in individual bias chain references may be reduced, as well as AGC voltage sensitivity, by using an external voltage divider for each AGC input.

Data Sheet Parameters as Design Aids

While production measurement to guarantee "black box" parameters for all possible operating conditions and frequencies is impractical, both the 703 and 171 data sheets supply a wealth of parameter information. The most convenient characterization for practical RF circuit design appears to be the four complex "y-parameters", which define input, output, and transfer admittances. In some cases, capacitance and resistance values are presented, as they are easier than pure y-parameters to verify in the laboratory, but they may easily be converted to equivalent y-parameters. A number of systematized design approaches are available, in the literature, and will not be treated here in detail.

Interstage Configurations

Tuned interstages for emitter coupled and cascode amplifiers can take a wide variety of forms, provided that they meet the DC biasing requirements previously outlined. The "tapped capacitor" parallel resonant circuit of Figures 1 and 2 is especially useful when transformers are to be avoided, or when adjustment capability is required to match different source and load admittances. A second common approach is the single or double tuned interstage transformer, currently used in the majority of commerical designs. While the transformer requires more careful initial design, to obtain desired matching, gain and bandwidth, it is better suited to mass-produced systems. Capacitively coupled interstages, such as three terminal ceramic filters, or crystal lattice filters, require RF chokes or external resistors to supply the required DC bias levels.

Practical Circuits

Two interstage designs will be briefly presented; one, a 10.7 MHz emitter-coupled stage, is useful in an FM IF strip, while the other, a 100 MHz cascode, might find application in a VHF receiver front end, or a radar IF strip. No attempt will be made to give optimized designs; however, considerations involved in such optimization are pointed out.

100 MHz Cascode

The objective is to build a high gain, narrow-band stage, with input and output matched to 50 ohms. To obtain high Q, and ease of matching, a capacitive divider is used for input and output, rather than a transformer (Figure 2). At 100 MHz, the following parameters may be read from typical curves on the 171 data sheet:

R_{IN} = 150 ohms, C_{IN} = 11 pF
(V_{CC} = 12V, connected to Pin 9)
or $y_{11} = 6.6 + j\,6.6$ mmhos
R_{OUT} = 9000 ohms, C_{OUT} = 3 pF
or $y_{22} = 0.11 + j\,1.8$ mmhos
and $y_{21} = 38 + j\,30$ mmhos (no AGC applied)
$y_{12} \approx .001 + j0$ mmhos (negligible)

Maximum available power gain may be calculated for these parameters:

$$MAG = \frac{|y_{21}|^2}{4\,g_{11}g_{22}}$$

$$= \frac{(48.5\times 10^{-3})^2}{(4\times 6.6\times 10^{-3}\times .11\times 10^{-3})} = 805 \qquad (5)$$

$$= 29.2\text{ dB} \quad (\text{neglecting } y_{12})$$

As a check, the stability criterion, C, is calculated:

$$C = \frac{|y_{12}y_{21}|}{2\,g_{11}g_{22} - R_e(y_{12}y_{21})}$$

$$= \frac{(.001\times 10^{-3}\times 48.5\times 10^{-3})}{2(6.6\times 10^{-3}\times .11\times 10^{-3}) - (.001\times 10^{-3}\times 38\times 10^{-3})}$$

$$= .0325 \qquad (6)$$

Since the criterion $0 < C < 1$ is satisfied, the cascode is unconditionally stable at 100 MHz, for any source and load. In a practical circuit, power gain nearly equal to MAG may be attained with conjugate input and output matching, provided that physical coupling (external feedback) between interstages is minimized by shielding or careful layout.

While circuit optimization must unavoidably be done in the laboratory, the procedure shown below will provide initial component values. To conjugate match a 50 ohm resistive source to 150 ohms, and 11 pF at the cascode input, consider Figure 11. An overall bandwidth of about 5 MHz is desired; however a preliminary calculation reveals that the required Q, for equal effect from input and output tuned circuits, requires impractical component values at the input, because of the low input resistance. The input coupling circuit is therefore designed with practical values, leaving the frequency shaping function primarily to the output network, in this example.

Choosing a total input capacitance of 15 pF, the value of L_1 is:

$$L_1 = \frac{1}{4\pi^2 f_o^2 C_{tIN}} = \frac{1}{4\pi^2(10^{16})\,15(10^{-12})} \qquad (7)$$

$$= 0.17\,\mu\text{H}$$

The series combination of C_1 and C_2 must equal the difference between C_{tin} and 11 pF, or 4 pF. For the circuit of Figure 2, the real part of input impedance, R_{in}, seen by the cascode input, may be calculated:

$$R_{IN} = R_S\left[\left(\frac{1}{2\pi f_o R_S C_2}\right)^2 + \left(1 + \frac{C_1}{C_2}\right)^2\right] \qquad (8)$$

after some rearranging,

$$\frac{C_1}{C_2} = \sqrt{\frac{R_{IN}}{R_S} - \left(\frac{1}{2\pi f_o R_S C_2}\right)^2} - 1 \qquad (9)$$

it may be shown that

$$\frac{R_{IN}}{R_S} \gg \left(\frac{1}{2\pi f_o R_S C_2}\right)^2 \qquad (10)$$

thus,

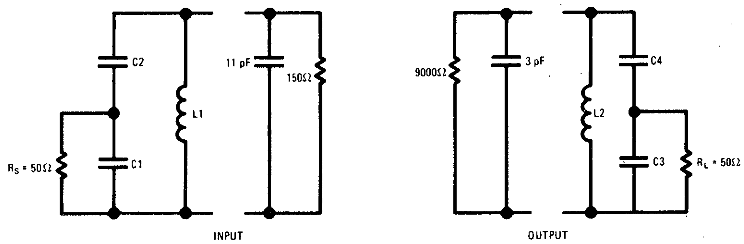

FIGURE 11. Equivalent 100 mHz Cascode Networks

$$\frac{C_1}{C_2} \approx \sqrt{\frac{R_{IN}}{R_S}} - 1 \qquad (11)$$

and

$$\frac{C_2C_1}{C_2+C_1} + C_{IN} = C_T \qquad (12)$$

substituting,

$$\frac{C_1}{C_2} = \sqrt{3} - 1 = .73 \qquad \frac{C_2C_1}{C_2+C_1} + 11\,\text{pF} = 15\,\text{pF}$$

solving,

$C_1 = 6.8$ pF, $C_2 = 9.4$ pF

The same procedure and equivalent circuit may be used to determine values for the output network; in this case, however, the choice of total output capacitance is not arbitrary, since a known bandwidth is desired. For a 5 MHz bandwidth, conjugate matched to 9000 ohms,

$$Q = \frac{f_o}{BW} = \frac{100}{5} = 20$$

$$C_{t(OUT)} = \frac{Q}{2\pi f_o R_{t(OUT)}} = \frac{20}{2\pi(10^8)(4500)} = 7.1\text{ pF}$$

$$L_2 = \frac{1}{4\pi^2(10^{16})\,7.1\,(10^{-12})} = 0.36\,\mu\text{H}$$

$$\frac{C_1}{C_2} \approx \sqrt{\frac{9000}{50}} - 1 = 13.4 - 1 = 12.4$$

$$\frac{C_2C_1}{C_2+C_1} = 7.1 - 3 = 4.1$$

solving,

$C_1 = 4.4$ pF, $C_2 = 55$ pF

Laboratory measurements, in which circuit values given above were used as design centers for adjustment, give typical cascode power gain of 27.5 dB, with the desired 5 MHz bandwidth, using carefully constructed, low loss inductors.

10.7 MHz FM IF Using Emitter Coupled Amplifiers

Complete design of a high quality FM IF strip is a painstaking process, in which a number of parameters must be weighed against each other. Since design techniques are well covered in the literature[4,5,6,7], only a brief discussion of design considerations will be included in this report.

Maximum available power gain may be calculated for either 171 or 703 as emitter coupled amplifier, using the formula of the preceding example. At 10.7 MHz, 25°C, and $V_{CC} = 12$V, using 703 values,

$y_{11} = 0.35 + j\,0.61$ mmho ($R_{IN} = 2.9$k, $C_{IN} = 9$pF)

$y_{21} = -33.4 + j\,5.88$ mmho (note negative real part)

$y_{12} \approx 0.002 + j\,0$ mmho

$y_{22} = 0.03 + j\,0.18$ mmho ($R_{OUT} = 33$k, $C_{OUT} = 2.6$ pF)

$$MAG = \frac{|y_{21}|^2}{4g_{11}g_{22}} = \frac{(34\times 10^{-3})^2}{4(.35\times 10^{-3}\times .03\times 10^{-3})} = 2.75\times 10^3$$

$$= 34.4\text{ dB}$$

(Due to somewhat different typical y-parameters, MAG for an Emitter Coupled 171 = 39 dB.)

Calculating the stability criterion:

$$C = \frac{|y_{12}y_{21}|}{2g_{11}g_{22} - R_e(y_{12}y_{21})}$$

$$= \frac{(.002\times 10^{-3}\times 34\times 10^{-3})}{2(.35\times 10^{-3}\times .03\times 10^{-3}) - (.002\times 10^{-3}\times[-33.4]\times 10^{-3})}$$

$$= \frac{6.8\times 10^{-8}}{2.1\times 10^{-8} + 6.7\times 10^{-8}}$$

$$= 0.775$$

For the conditions given, $0 < C < 1$, making the device unconditionally stable for all sources and loads. In a practical 10.7 MHz IF strip, however, external coupling, especially from the strip's output to its input, can cause instability without careful physical design.

A modern FM tuner IF strip capable of low-distortion multiplex reception, requires:

A. Bandwidth at least 300 kHz. In a four stage design, with five interstage networks, bandwidth per stage may be calculated from overall bandwidth by use of the "shrinkage" formula:

$$BW(\text{per stage}) = \frac{BW_{(overall)}}{\sqrt{2^{1/n} - 1}} \quad (n = \text{number of interstages})$$

$$= \frac{300}{\sqrt{2^{1/5}-1}} = \frac{300}{.388} \qquad (13)$$

$$= 773\,\text{kHz}$$

B. Sharp skirt selectivity without phase/frequency nonlinearity within the passband. This usually implies double-tuned interstage transformers. Stover, et. al.(5), show that a transformer coupling factor between 0.6 and 0.8 gives minimum phase nonlinearity, the higher value being preferred for higher gain per stage.

C. Overall power gain of at least 100 dB, or 25 dB per stage in a four stage strip, to obtain adequate sensitivity and AM rejection.

D. A maximum value of load resistance across the output of each stage, given by:

$$R_L \leqslant \frac{2(V_{CC}-NV_{be})}{I_{OUT(MAX)}} \qquad (14)$$

where N = number of bias chain diodes

N = 2 for the 703, or 3 for the 171

$I_{OUT(MAX)}$ is approximately 5 mA, for both types.

This relationship assures that maximum output current limiting is reached before the output transistor can saturate, guaranteeing non-saturated limiting action.

E. The input admittance used in making interstage calculations should be the value resulting from a given value of input swing, (see Figure 6), rather than the small-signal value. The input swing, however, depends upon the transformer ratio, so that transformer optimization is a multi-approximation procedure.

F. The interstages should be designed to minimize the effects of varying drive levels upon center frequency and bandwidth, since very weak signals may operate the first one or two stages linearly, rather than as limiters.

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June 1968

NEW USES FOR THE LM100 REGULATOR

INTRODUCTION

One might think that an integrated circuit like a voltage regulator would be limited to one specialized application. Such is not the case, as was proven by the results of an applications contest that was conducted recently for our LM100 voltage regulator.

The LM100 is a monolithic integrated circuit that was designed as a series regulator to operate in either a linear or a switching mode. Its output voltage can be set anywhere between 2 and 30V with a pair of external resistors. By itself it can deliver output currents of 10 to 20 mA, but discrete transistors can be added to boost the output current to any desired level. The integrated circuit design is described along with its applications as a series regulator in references 1 and 2.

The contest brought out a number of novel ways to use the LM100 in other voltage-regulator applications such as a shunt regulator. Included were temperature regulators and light-level regulators. It was also shown that the LM100 could effectively be used as an operational amplifier, especially if the application required a reference voltage or if it was necessary to add transistors for increased output power.

It is appropriate to point out that all the circuits described here for the LM100 will work equally well with the LM200 or LM300, within their respective temperature and operating-voltage ranges.

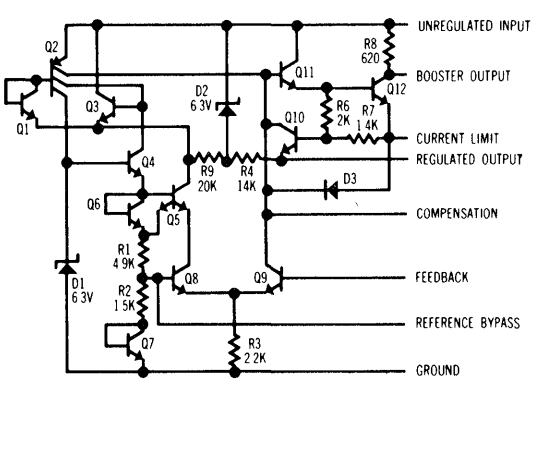


FIGURE 1. LM100 Schematic

THE LM100

Before going into the various circuits, it is in order to describe briefly the operation of the LM100. A schematic diagram of the integrated circuit is given in Figure 1. Generation of the reference voltage starts with zener diode, D1, which is supplied with a fixed current from one of the collectors of Q2. This regulated voltage, which has a positive temperature coefficient, is buffered by Q4, divided down by R1 and R2 and connected in series with a diode-connected transistor, Q7. The negative temperature coefficient of Q7 cancels out the positive coefficient of the voltage across R2, producing a temperature-compensated 1.8V on the base of Q8. This point is also brought outside the circuit so that an external capacitor can be added to bypass any noise from the zener diode.

Transistors Q8 and Q9 make up the error amplifier of the circuit. A gain of 2000 is obtained from this single stage by using a current source, another collector on Q2, as a collector load. The output of the amplifier is buffered by Q11 and used to drive the series-pass transistor, Q12. The collector of Q12 is brought out so that an external PNP transistor, or PNP-NPN combination, can be added for increased output current.

Current limiting is provided by Q10. When the voltage across an external resistor connected between Pins 1 and 8 becomes high enough to turn on Q10, it removes the base drive from Q11 so the regulator exhibits a constant-current characteristic. As for the remaining details, the collector of the amplifier, Q9, is brought out so that external collector-base capacitance can be added to frequency-stabilize the circuit when it is used as a linear regulator. R9 and R4 are used to start up the regulator, while the rest of the circuitry establishes the proper operating levels for the current source transistor, Q2.

Now that some understanding of the internal workings of the LM100 has been established, we can discuss the applications for the circuit.

SHUNT REGULATOR

Shunt regulators are sometimes substituted for series regulators even though they are less efficient. The reason is that they are not as sensitive to input voltage transients, they do not feed load current transients back into the unregulated supply, they are inherently short-circuit proof and they are less prone to failures where the output voltage becomes excessive.

Although the LM100 was designed primarily as a series regulator, it can also be used in shunt-regulator applications. Figure 2 shows a 3A shunt regulator. The output of the LM100 drives a compound emitter follower which conducts the excess input current. A zener diode, D1, provides a level shift so that the output transistors within the LM100 are properly biased. R5 supplies base drive for Q2 and also the minimum load current for the LM100. R4 is included to minimize dissipation in the power transistors when the regulator is lightly loaded. The output voltage is determined in the normal fashion by R1 and R2. Although no output capacitor is used, it may be advisable to include one to reduce the output impedance at high frequencies.

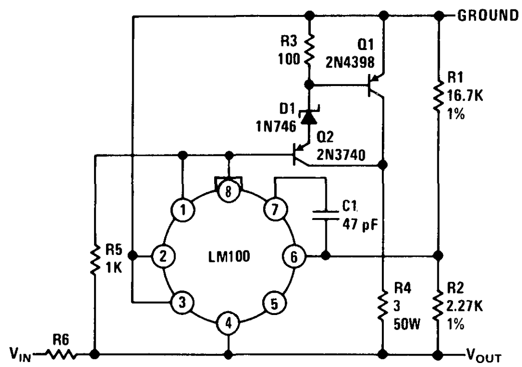


FIGURE 2. Negative Shunt Regulator

Because a shunt regulator is a two terminal device, one design, using an LM100, can be used as either a positive or a negative regulator.

This circuit was submitted by Bob Dobkin of Philbrick/Nexus Research, Dedham, Massachusetts and R. F. Downs of LTV Research Center, Anaheim, California.

SWITCHING REGULATOR WITH OVERLOAD SHUTOFF

It is difficult to current limit a switching regulator because the circuit must continue to operate in a high efficiency switching mode even when the output is short circuited. Otherwise, the power dissipation in the switch transistor will be excessive, more than ten times the full load dissipation, even though the current is limited.

A unique solution to this problem is the overload shutoff scheme shown in Figure 3. When the output current becomes excessive, the voltage drop across a current sense resistor fires an SCR which shuts off the regulator. The regulator remains off, dissipating practically no power, until it is reset by removing the input voltage.

In the actual circuit, complementary transistors, Q1 and Q2, replace the SCR since it is difficult to find devices with a low enough holding current (about 50 μA). When the voltage drop across R4 rises to about 0.7V, Q2 turns on, removing the base drive to the output transistors on the LM100 through Pin 7. Then Q1 latches Q2, holding the regulator off until the input voltage is removed. It will then start when power is applied if the overload has been removed.

This circuit was designed by Dan Lubarsky of Moore Associates, San Carlos, California.

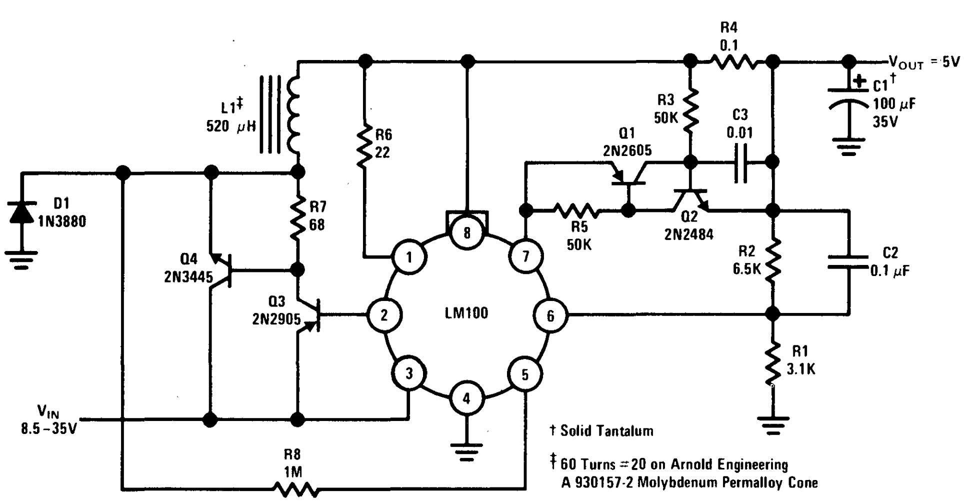


FIGURE 3. 3A Switching Regulator With Overload Shutoff

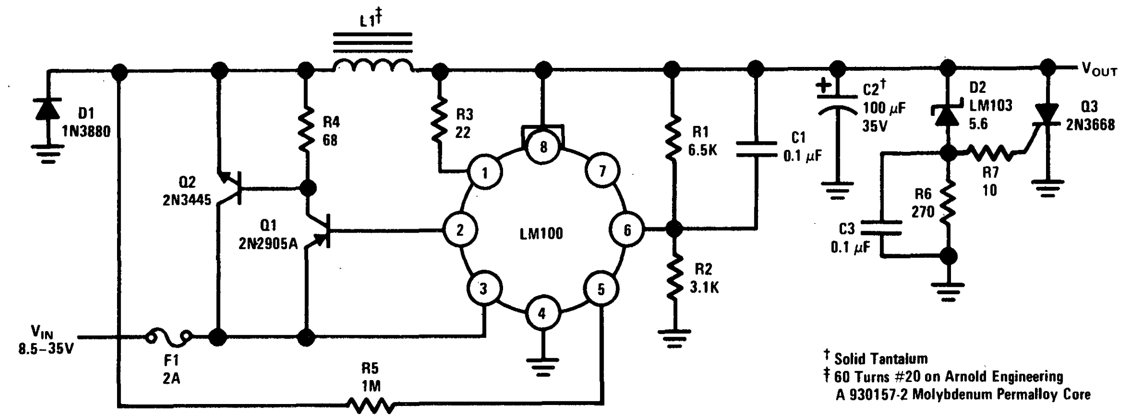


FIGURE 4. Switching Regulator with Crowbar Overvoltage Protection

OVERVOLTAGE PROTECTION

A switching regulator can be used in place of a power converter to reduce high input voltages down to a considerably lower output voltage with good efficiency. In addition, it simultaneously regulates the output voltage. As a result, a switching regulator is simpler and more efficient than a power converter/regulator combination. One objection brought up against switching regulators is that they can fail with the output voltage going up to the unregulated input voltage which is frequently several times the regulated output voltage. This can destroy the equipment that the regulator is supplying. A power converter has the advantage that it will usually fail with the output voltage going to zero.

A circuit which protects the load from overvoltages is shown in Figure 4. If the output voltage should rise significantly above 6V, the zener diode, D2, breaks down and fires the SCR, Q13, shorting the output and blowing the fuse on the input line. C3 keeps the SCR from firing on the voltage transients which can be present around a switching regulator, and R7 is included to make sure that excessive gate current does not flow when it fires. Since the SCR is located on the output of the regulator, it is not prone to dV/dt firing on fast transients which might be present on the unregulated input.

It is important to design the regulator so that the overshoot in the output voltage[2] caused by suddenly removing full load current does not fire the SCR. If this is done, about the only thing that can cause an overvoltage output is failure of the regulator switching transistors.

This circuit comes from E. S. Madson of ESM, Copenhagen, Denmark and Don Learned, Heath Company, Benton Harbor, Michigan.

FOCUS CONTROL CURRENT SOURCE

Although the LM100 is most frequently used as a voltage regulator, it is also useful as a current regulator. A current regulator can be made by regulating the voltage across a known resistor, producing a fixed current.

The focus control current source shown in Figure 5 is an example of such a current regulator.

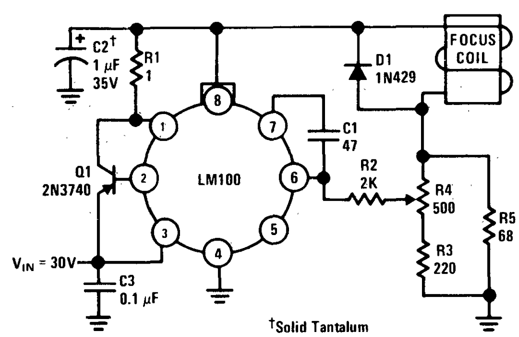


FIGURE 5. Focus Control Current Source

The output current from the pass transistor, Q1, is set by selecting an appropriate value for R5 and then adjusting the voltage drop across it with R4. With the arrangement used, most of the power is dissipated in R5 rather than the control potentiometer. R2 is included in the adjustment circuit so that the LM100 feedback terminal operates from approximately 2.2 kΩ source resistance. This is the optimum design value for minimum thermal drift and proper frequency compensation.

The regulator is protected against shorts to ground, from the focus coil or its leads, by R1. D1 prevents voltage reversals on the integrated circuit or the pass element, caused by the inductive kickback of the focus coil, when the input voltage is switched off. C2 and C3 are required to keep the circuit from oscillating.

A particular advantage of the LM100 in this application is that its low reference voltage enables it to regulate a current with a minimum of voltage dropped across the sense resistor. This is important both to increase the efficiency and to minimize dissipation in the sense resistor which usually must be a precision resistor.

This design was submitted by H. J. Weber of EG&G, Boston, Massachusetts. Similar circuits were sent in by C. M. Katkic of Michigan Bell Telephone Company, Southfield, Michigan and C. H. Ristad.

1A CURRENT SOURCE

Another current source circuit is shown in Figure 6. Here the LM100 regulates the emitter current of a Darlington-connected transistor, and the output current is taken from the collectors. The use of a Darlington connection for Q1 and Q2 improves the accuracy of the circuit by minimizing the base-current error between the emitter and collector current.

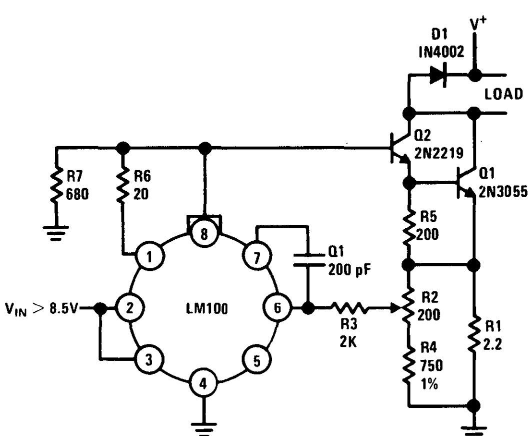


FIGURE 6. 1A Current Source

The output of the LM100, which drives the control transistors, must be short-circuit protected with R6 to limit the current when Q2 saturates. R7 is required to provide the minimum load current for the integrated circuit. D1 is included to absorb the kickback of inductive loads when power is shut off. The output current of the circuit is adjusted with R2.

The maximum supply voltage (V^+) that can be used with this circuit is limited only by the breakdown voltage of the control transistors. If this voltage is less than 40V, this supply can also be used to power the LM100.

The regulator can be switched off electrically by clamping Pin 7 of the LM100 with a 1 kΩ resistor, a diode, and a transistor to ground. If it is desirable to operate the circuit as a fast switch, however, Q1 should be replaced with a faster transistor like the 2N3445 and C1 should be reduced to 47 pF. It would also be advisable to use a 1N3880, which is a faster device, for D1.

This circuit was contributed by Bob Dobkin of Philbrick/Nexus Research, Dedham, Massachusetts; Tom Hall of Bausch and Lomb, Bellaire, Texas and Steve Menasian of the University of Washington, Seattle, Washington.

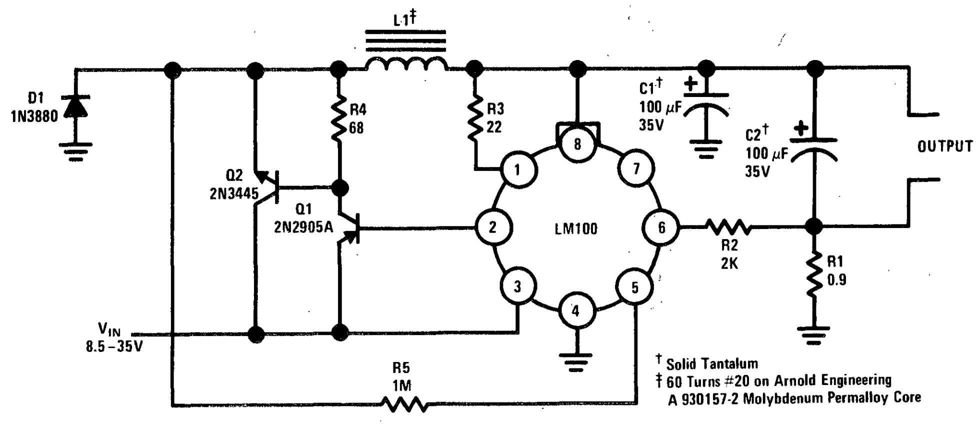
SWITCHING CURRENT REGULATOR

Current regulators generally operate with a large voltage drop across the control transistors since they must accommodate large variations in the voltage across the load. Consequently, the power dissipation in the transistors can be quite high.

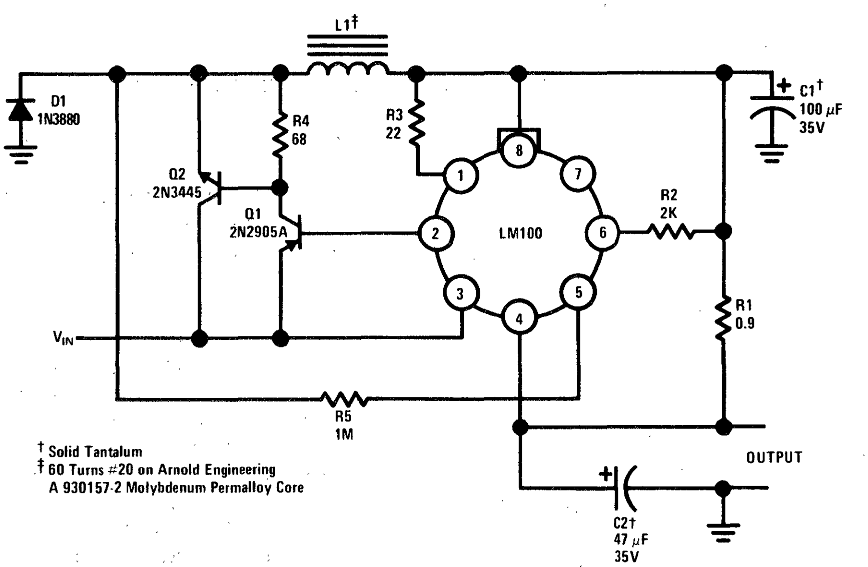
The switching regulator principle can be applied to a current regulator to greatly increase efficiency and reduce the power dissipation in the control transistors. Figure 7a gives the schematic of a switching current regulator wherein the input power,[1] for a fixed load current, is roughly proportional to the voltage across the load. A standard switching regulator is used, except that the load is connected from the output to the feedback terminal of the LM100. A current sense resistor, R1, is connected from the feedback terminal to ground to set the output current. If desired, an adjustment potentiometer can be connected across the current sense resistor as shown in Figure 6.

An additional filter capacitor, C2, is put across the load terminals to reduce output ripple. If it is not needed, it can be removed if an 0.1 μF capacitor is connected from the top of C1 to Pin 6 of the LM100 to make sure all the output ripple of the regulator appears at the feedback terminal.

An alternate scheme which has the current output referenced to ground is given in Figure 7b. This circuit is identical to that in Figure 7a except that the load is inserted in the ground line. The quiescent current of the regulator, flowing out of Pin 4, introduces an error term. However, since this current is only about 2 mA and is reasonably independent of changes in the input or load voltages, the error is usually not significant.



a. Current Source With Floating Load



b. Current Source With Grounded Load

FIGURE 7. Switching Current Regulators

With this circuit, the difference between the input voltage and the load voltage cannot drop below 8.5V, or the circuit will drop out of regulation because the voltage across the LM100 is insufficient to bias the reference circuitry.

This circuit was sent in by T. H. Lynch of Bunker-Ramo Corporation, Canoga Park, California.

TEMPERATURE CONTROLLER

A circuit for an oven-temperature controller using the LM100 is given in Figure 8. Temperature changes in the oven are sensed by a thermistor. This signal is fed to the LM100 which controls power to the heater by switching the series pass transistor, Q2, on and off. Since the pass transistor will be nearly saturated in the on condition, its power dissipation is minimized.

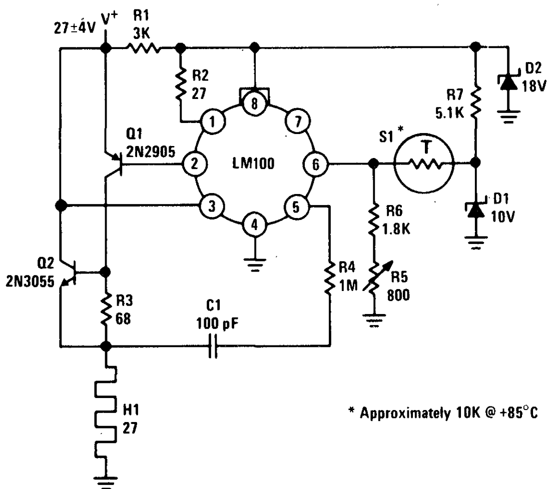


FIGURE 8. Switching Temperature Controller

In operation, if the oven temperature should try to increase, the thermistor resistance will drop, increasing the voltage on the feedback terminal of the regulator. This action shuts off power to the heater. The opposite would be true if the temperature dropped.

Variable-duty-cycle. switching action is obtained by applying positive feedback around the regulator from the output to the reference bypass terminal (which is also the non-inverting input to the error amplifier) through C1 and R4. When the circuit switches on or off, it will remain in that state for a time determined by this RC time constant.

Additional details of the circuit are that base drive to Q1 is limited, to a value determined by R2, by the internal current-limiting circuitry of the LM100. D2 provides a roughly regulated supply for D1 in addition to fixing the output level of the LM100 at a level which properly biases the internal transistors. The reference diode for the thermistor sensor, D1, need not be a temperature-compensated device as long as it is put in the oven with the thermistor. Finally, the temperature is adjusted with R5.

Using a thermistor with a temperature coefficient higher than 1%/°C, control accuracy should be better than ±1°C for a wide range of ambient conditions, even if the LM100 is not put inside the oven.

This circuit was contributed by C. W. Andreasen of Stromberg-Carlson, San Diego, California and A. B. Williams of Stelma Incorporated, Stamford, Connecticut.

POWER AMPLIFIER

The versatility of the LM100 is demonstrated by the power amplifier circuit in Figure 9. The LM100 is used as a high-gain amplifier and connected to a quasi-complementary power output stage. Feedback around the entire circuit stabilizes the gain and reduces distortion. In addition, the regulation characteristics of the LM100 are used to stabilize the quiescent output voltage and minimize ripple feedthrough from the power supply.

The LM100 drives the output transistors, Q5 and Q6, for positive-going output signals while Q1, operating as a current source from the 1.8V on the reference terminal of the LM100, supplies base drive to Q3 and Q4 for negative-going signals. Q2 eliminates the dead zone of the class-B output stage, and it is bypassed by C5 to present a lower driving impedance to Q3 at high frequencies. The voltage drop across Q2 will be a multiple of its emitter-base voltage, determined by R9 and R10. These resistors can therefore be selected to give the desired quiescent current in Q4 and Q6. It is important that Q2 be mounted on the heat sink with the output and driver transistors to prevent thermal runaway.

Output current limiting is obtained with D2 and D3. D2 clamps the base drive of Q3 when the voltage drop across R6 exceeds one diode drop, and D3 clamps the base of Q5 when the voltage across R7 becomes greater than two diode drops. R11 is needed to limit the output current of the LM100 when D3 becomes forward biased.

The power supply ripple is peak detected by D1 and C1 to get increased positive output swing by operating the LM100 at a higher voltage than Q5 and Q6 during the troughs of the ripple. This also reduces the ripple seen by the LM100. C5 bypasses any zener noise on the reference terminal of the LM100 that would otherwise be seen on the output.

The quiescent output voltage is set with R2 and R3 in the same way as with a voltage regulator. The ac voltage gain is determined by the ratio of R1 and R3, since the circuit is connected as a summing amplifier.

This circuit was designed by Bob Dobkin of Philbrick/Nexus Research, Dedham, Massachusetts and H. D. Carlstrom, Sanders Associates, Nashua, New Hampshire.

HIGH EFFICIENCY SINGLE-SIDEBAND TRANSMITTER

A circuit which can be used to improve the efficiency of a single-sideband transmitter is shown in Figure 10. A switching regulator operates the linear output amplifiers of a conventional single-sideband transmitter at a voltage just higher than that required to accommodate the envelope of the

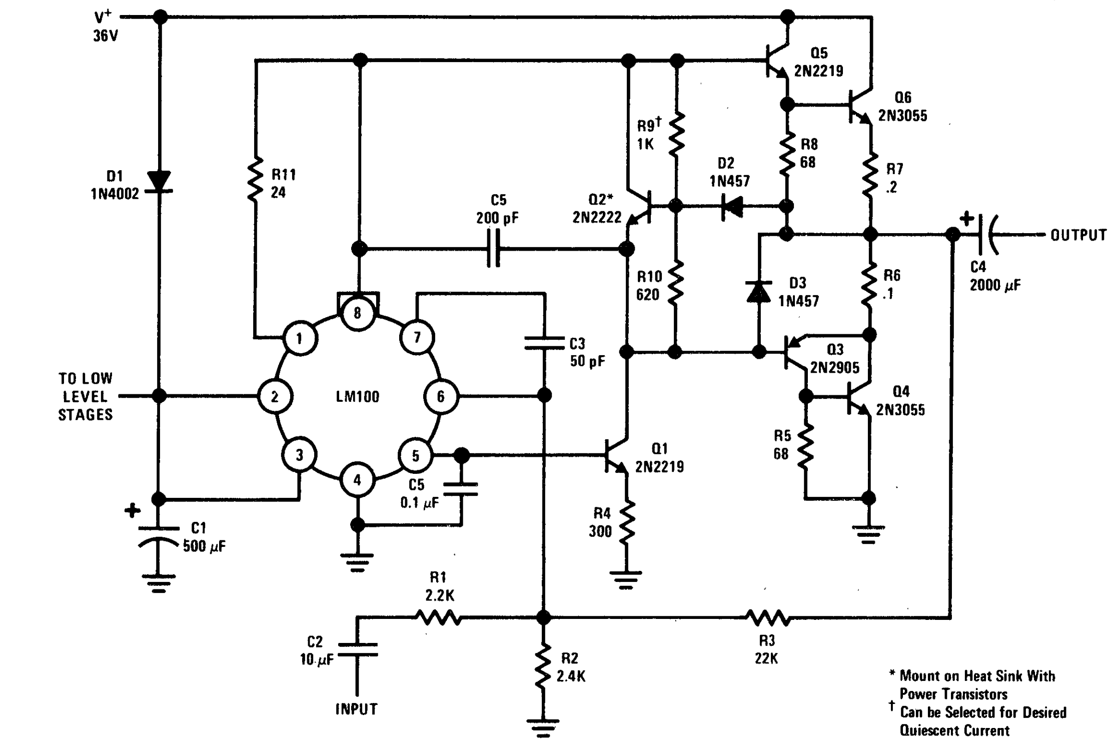


FIGURE 9. Power Amplifier With Current Limiting

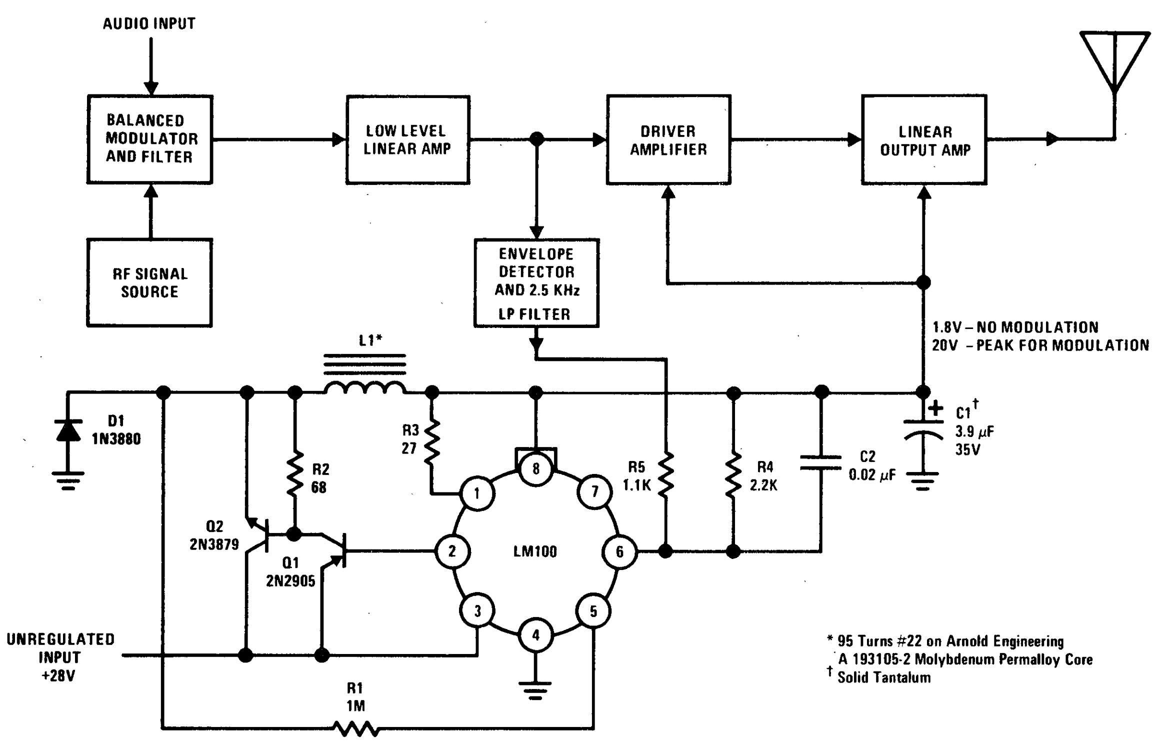


FIGURE 10. High Efficiency Modulation Scheme for Single Sideband Transmitter

rf output signal. With no modulating signal, the driver and output amplifiers are operated at 1.8V, which is the reference voltage of the LM100. When modulation is present, the envelope of the rf waveform is detected and used to drive the regulator so that its output voltage follows the shape of the envelope. Hence, the amplifiers are always supplied just enough voltage to keep them from saturating. Since the switching regulator converts the dc input voltage down to the lower voltage driving the amplifiers with high efficiency, the overall transmitter efficiency is increased.

The amplitude of the envelope on the output of the switching regulator is determined by R5, as the detected envelope will be multiplied by the ratio R4/R5. The output signal of the envelope detector must be negative-going so that the drive voltage will be positive-going. In addition, it is necessary to dc couple or clamp the detected envelope so that the supply voltage to the amplifiers does not drop below their minimum operating level on the troughs of the signal. It is also important that the output amplifiers be designed so that their gain does not vary with the voltage supplied to them or distortion will be introduced.

This technique can be used to increase efficiency with AM transmission. Here, the switching regulator is driven with a negative-going modulation signal, which has been clamped to 1.8V, instead of the detected envelope. The regulator output drives a class-C rf power stage. The output waveform of the regulator must accurately follow the modulating signal, and the ripple on the output of the switching regulator must be eliminated because the drive signal to the output amplifier appears directly on the envelope of the rf output. These conditions can be satisfied by operating the switching regulator at 100 kHz and using additional filtering between the regulator and the output stage.

With either modulation scheme, the output voltage of the regulator/amplifier can be limited by putting a zener diode across R4. This protects the rf output amplifier from excessive voltage caused by overmodulation or high dc input voltage.

This design comes from Ben Stopka of Collins Radio, Cedar Rapids, Iowa.

LIGHT-INTENSITY REGULATOR

Figure 11 gives the circuit for a light-intensity regulator using the LM100. A phototransistor senses the light level and drives the feedback terminal of the LM100 to control current flow into an incandescent bulb. R1 serves to limit the inrush current to the bulb when the circuit is first turned on.

The current gain of the phototransistor, Q2, is fixed at 10, to make it less temperature sensitive, by R3 and the temperature compensating diode, D1. A photodiode, such as the 1N2175, could be substituted for the phototransistor if it had sufficient light sensitivity; and R3 and D1 could be eliminated. The input voltage does not have to be regulated as the sensitivity of a phototransistor or photodiode is not greatly affected by the voltage drop across it. A photoconductor can also be used in place of the phototransistor, except that input voltage would have to be regulated.

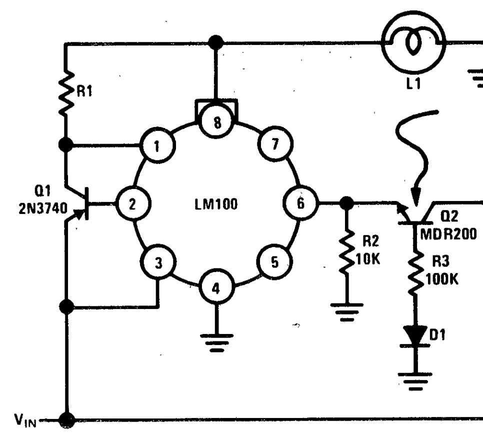


FIGURE 11. Light Intensity Regulator

This circuit is adapted from one submitted by Geoffrey Hedrick of Lear Siegler/Astek Division, Armonk, New York.

HIGH VOLTAGE REGULATOR

Although the LM100 was designed primarily for applications with output voltages below 30V, it can be used as a high voltage regulator under certain circumstances. An example of this, a circuit regulating the output of a 2 KV supply, is given in Figure 12.

The LM100 senses the output of the high voltage supply through a resistive divider and varies the input to a dc/dc converter, which generates the high voltage. Hence, the circuit regulates without having any high voltages impressed across it.

Under ordinary circumstances, the feedback terminal of the LM100 wants to operate from a 2K divider impedance. Satisfying this condition on a 2 KV regulator would require that about 2W be dissipated in the divider. This, however, is reduced to 40 mW by the addition of Q1 which acts as a buffer for a high impedance divider, operating the LM100 from the proper source resistance. The other half of the transistor, Q2, is required to compensate for the temperature drift in the emitter-base voltage of Q1, so that it is not multiplied by the divider ratio. The circuit does have an uncompensated drift of 2 mV/°C; but this is added directly to the output, not multiplied by the divider ratio, so it will be insignificant with a 2 KV regulator.

This circuit was contributed by Don Sobel of Federal Scientific Corporation, New York, New York and A. A. Frank of the University of Southern California, Los Angeles, California.

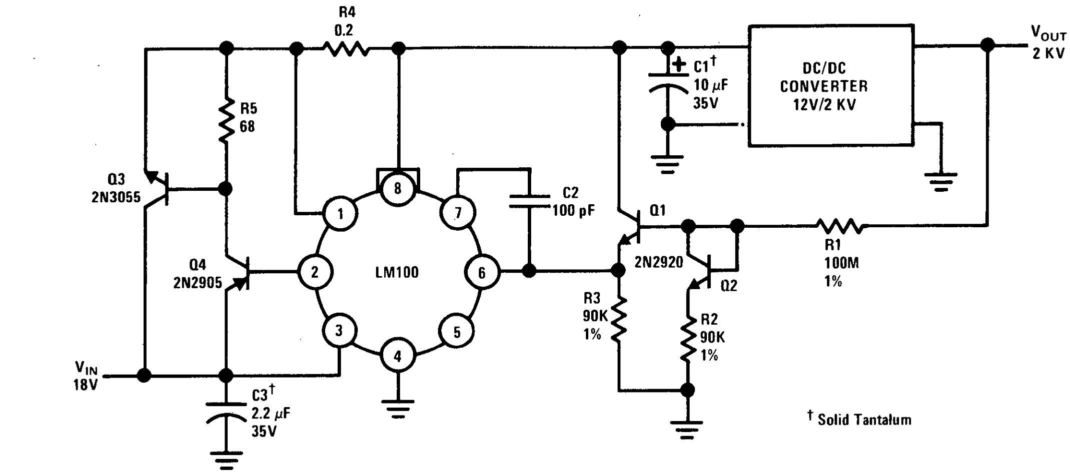


FIGURE 12. High Voltage Regulator

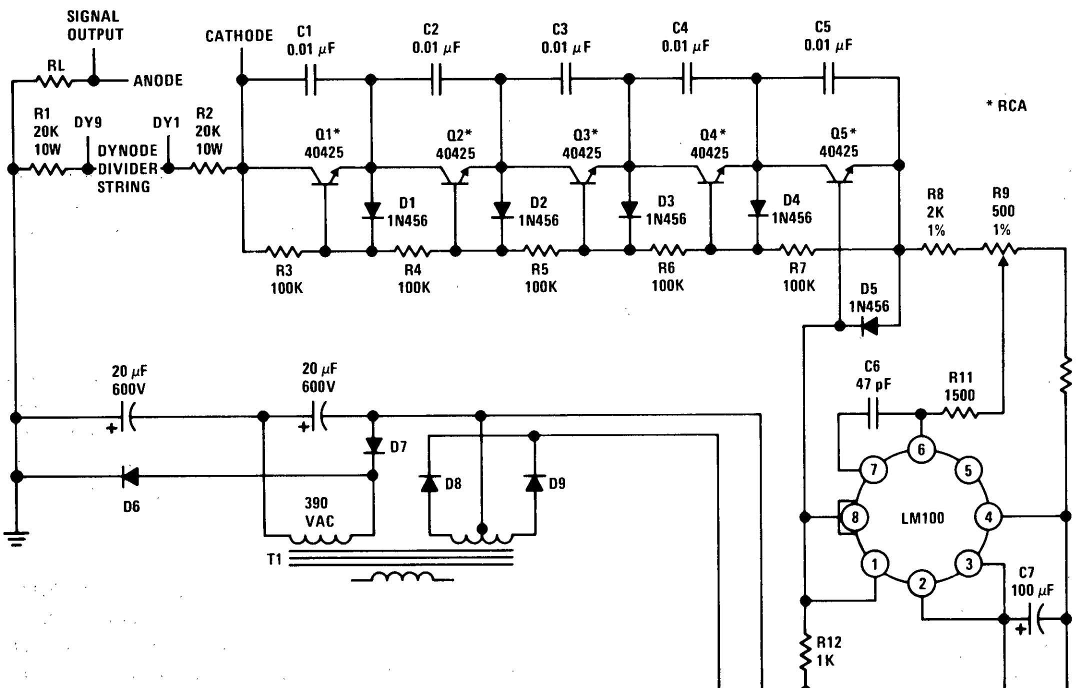


FIGURE 13. Photomultiplier Tube Supply

PHOTOMULTIPLIER TUBE SUPPLY

A second high voltage supply is diagrammed in Figure 13. This is a high voltage supply for a 9-dynode photomultiplier tube. In this circuit, a full wave rectifier operating off one winding of a power transformer provides a 15V bias voltage for the LM100. The high voltage is produced from a voltage doubler which operates from a second winding. The circuit actually functions as a current regulator similar to that shown in Figure 6. The output current is passed through a resistive divider which develops the operating voltages for the cathode and dynodes of the photomultiplier tube.

Five cascode-connected transistors, Q1 through Q5, are used as the pass transistors. This is presently the lowest-cost solution to the problem of handling the required voltage and power levels. Base drive is provided for the cascode string, by R3 through R7, in a manner which does not affect regulation. Capacitors, C1 through C5, suppress and equalize transients across the pass transistors; and clamp diodes across the sensitive emitter-base junctions of the transistors prevent damage from voltage transients.

This circuit was designed by J. P. Ekstrand of Spectra Physics, Mountain View, California.

LINE RESISTANCE COMPENSATOR

Remote sensing of the load voltage to eliminate the effects of line resistance can be done with the LM100 by connecting the feedback resistors directly across the load, rather than at the regulator output. However, it may be necessary to increase the size of the frequency compensation capacitor ordinarily used with the regulator. In certain applications, remote sensing is undesirable or the actual load is not directly accessible. An example of this is a dc motor application where it is desirable to reduce the effects of the armature resistance.

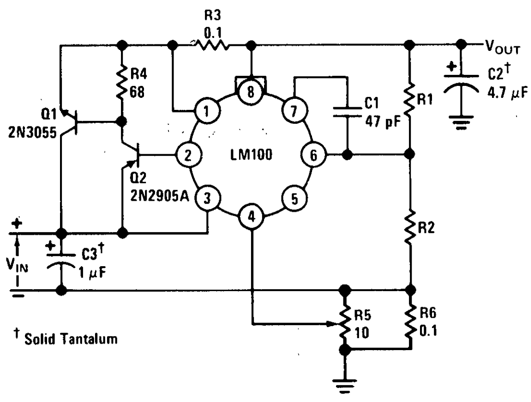


FIGURE 14. Line Resistance Compensator for High Current Regulators

A circuit which permits compensation of line resistance is shown in Figure 14. A negative-going voltage which is proportional to the load current is produced across R6. Divider resistor, R2, is returned to this voltage so that the output voltage will increase with increasing load current. The ground terminal of the regulator is returned to the arm of the potentiometer connected across R6 so that the compensation can be set to exactly cancel out the line resistance. With the arm of the potentiometer on ground, the output resistance will be reduced by R6 multiplied by the ratio of R1 to R2. With the potentiometer set to the opposite extreme, the output resistance will be increased by the value of R6.

There is a reason why R5 is included, and R6 is not just made a potentiometer. It is practically impossible to find a potentiometer with a low enough resistance value and high enough power rating. In fact, with higher currents, it is even hard to find a suitable resistor for R6. A 0.1Ω, 10W resistor is not easy to find. One way of getting it is to take a 1Ω, 10W, adjustable, wire-wound resistor and put two taps at the 1/3 resistance points. The three resistor segments are then connected in parallel to make a 0.11Ω, 10W resistor.

This circuit was suggested by W. J. Godsey of Hayes International Corporation, Birmingham, Alabama.

USING ALL NPN PASS TRANSISTORS

The LM100 was designed to use a PNP or PNP/NPN combination for the series pass element. With this configuration, the minimum output-input voltage differential is not increased by the addition of booster transistors. However, the device can also be used with all NPN pass transistors as shown in Figure 15.

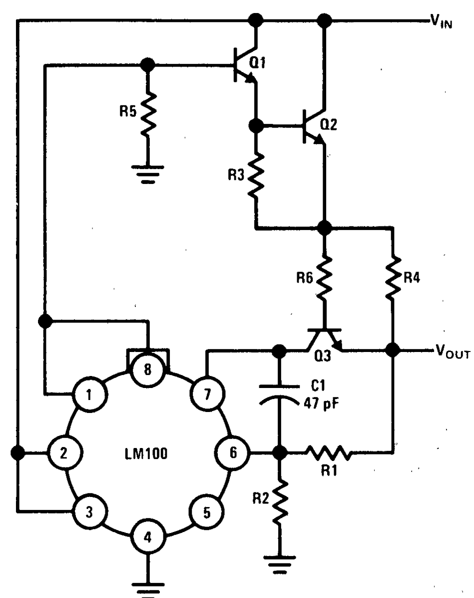


FIGURE 15. Circuit for Using the LM100 With all NPN Pass Elements

With this configuration, it is not possible to use the internal current limiting of the LM100, so an external transistor, Q3, must be added to provide this function. Limiting occurs when the voltage drop across R4 is equal to the emitter-base voltage of Q3. R5 is also required to make sure that the LM100 is operated above its minimum load current.

The main advantage of using all NPN pass transistors is that the circuit can be operated with less capacitance on the output of the regulator. When NPN and PNP transistors are used, relatively large (1-10 µF) bypass capacitors must be connected on both the input and output of the regulator. Without these, the circuit is susceptible to oscillations.

This design was based on a circuit submitted by E. F. Donner of Lockheed, San Jose, California.

HIGH STABILITY REGULATOR

The performance of regulators with output voltages above 10V can be improved considerably by the addition of an external temperature-compensated reference diode. Normally, the voltage change at the feedback terminal of the LM100 due to changes in temperature, load or input voltage are multiplied by the divider ratio of the feedback resistors which determine the output voltage. This effect can be reduced by putting a reference diode in the feedback divider as shown in Figure 16. The diode permits a lower divider ratio to be used and, therefore, improves regulation and drift characteristics.

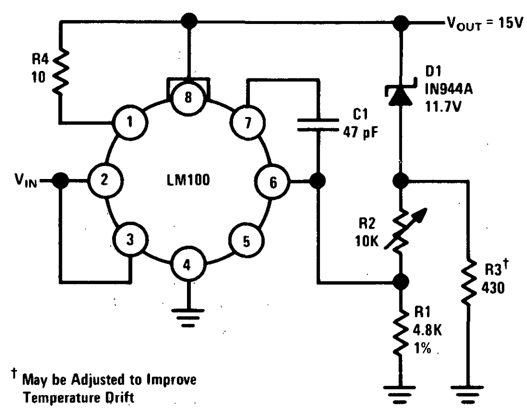


FIGURE 16. High Stability Regulator

The regulation of the circuit in Figure 16 is given by

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \left(\frac{V_{OUT} - V_Z}{V_{OUT}}\right) \frac{\Delta V_{FB}}{V_{FB}},$$

where V_Z is the breakdown voltage of D1 and V_{FB} is the voltage on the feedback terminal of the regulator. Hence, the improvement in regulation and temperature drift (assuming no drift in the external diode) will be $\frac{V_{OUT}}{V_{OUT} - V_Z}$, which is equal to 4.5 in the example given.

The temperature drift can be improved still further by adjusting R3 to compensate for the combined drift of D1 and the LM100. Changing the diode current changes its drift, as shown in Figure 17. Larger values of R3 make the output voltage temperature coefficient more negative, while decreasing the resistor makes the temperature coefficient more positive.

Although the circuit shown is a low current regulator, this idea is equally useful for high-power linear regulators and even switching regulators.

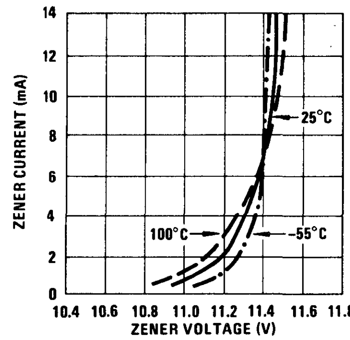


FIGURE 17. Drift Characteristics of an 1N944A as a Function of Operating Current

This contribution was made by Ahti Aintila, Helsinki, Finland.

PULSE REGULATOR

Because of the relatively fast operation possible with the LM100, it can be used as a pulse squarer or pulse regulator. A circuit which accomplishes this is shown in Figure 18.

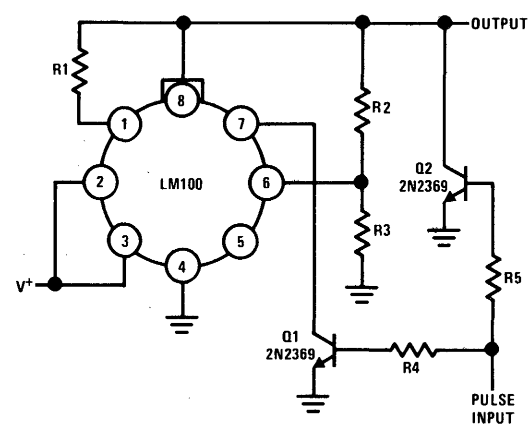


FIGURE 18. Pulse Regulator

In this circuit, R2 and R3 are set up to give the desired pulse height (dc) from the LM100. A positive-pulse input turns on Q1, which disables the LM100 by grounding the base of the NPN emitter followers on the output of the integrated circuit. At the same time, Q2 grounds the regulator output, providing current-sinking capability.

If additional output-current drive is needed, an NPN buffer, similar to that shown in Figure 15, should be used on the LM100 in place of a PNP because of the difficulties encountered in stabilizing the PNP circuit without capacitance on the output.

This method of pulsing the circuit on and off, that is pulling Pin 7 down within one diode drop of ground, can be used as an electrical shutoff for any of the voltage or current regulators.

Credit for this circuit is given to Don Maurer of Medtronic Incorporated, Minneapolis, Minnesota and E. E. Cunningham of Ectron Corporation, San Diego, California.

CONCLUSION

These examples show that certain integrated circuits can be treated like a component, rather than a specialized circuit function. This seems to be particularly true for linear integrated circuits. It is possible to use almost any standard circuit in a wide variety of applications by designing imaginatively. If this is done, it is possible to reap the rewards of standard circuits – low cost and immediate availability – in practically any equipment design.

REFERENCES

1. R. J. Widlar, "A Versatile, Monolithic Voltage Regulator," National Semiconductor Corporation AN-1, February, 1967.
2. R. J. Widlar, "Designing Switching Regulators," National Semiconductor Corporation AN-2, April, 1967.

December 1968

LOW POWER OPERATIONAL NH0001 AMPLIFIER

INTRODUCTION

Although many Integrated Circuit Operational Amplifiers are available with excellent characteristics, two areas leave considerable room for improvement; namely, offset voltage and power requirements. The NH0001 operational amplifier has been designed to provide extremely low offset voltages (typically 0.2 millivolts at 25°C) and quiescent supply currents in the 100 μA range, while still providing reasonable loaded output swings and a compensated gain bandwidth in the 0.5 to 1.0 MHz range. The circuit diagram (Figure 1A and 1B) shows the simplicity of the NH0001; the only unusual characteristic being the use of PNP transistors in the input stages for improved beta vs. temperature linearity and lower noise.

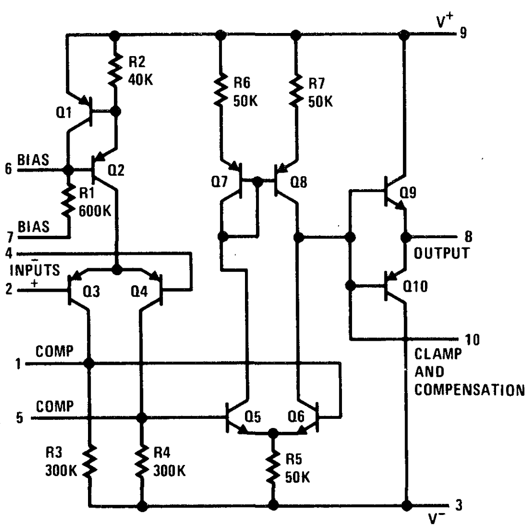


Figure 1A. NH0001 Schematic.

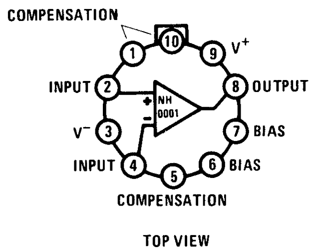


Figure 1B. NH0001 Pin Configuration.

CIRCUIT OPERATION

Q1, Q2, R1 and R2 form a simple constant current supply of ≈16 μA at 25°C, 8 μA at +125°C and 22 μA at -55°C. This current is supplied to the common emitters of the input pair Q3 and Q4 which, along with their load resistors R3 and R4, form a simple differential amplifier. The low frequency gain of this stage is approximately 30, minimizing the effect on the input of changes in offset voltage in the second stage pair, Q5 and Q6.

The second stage differential pair with high impedance load, Q8, form the main voltage gain of the amplifier. Typical values of collector currents in Q5 and Q6 are 20 μA each and the voltage gain of this stage is approximately 2000.

The output section is simply a compound NPN – PNP pair providing isolation between the high impedance junction of the collectors of Q6 and Q8, and the load.

Operation from Single Power Supply

When operating from ±V supplies, pin 7 is normally returned to ground. When operating from a single supply, or when no ground is available, pin 7 may be directly connected to pin 3, for voltages equal to or less than 20 volts between pins 3 and 9. This will increase the quiescent current since the effect of connecting pin 7 to pin 3 is to connect the 600K resistor, R1, across the full power supplies. Since the minimum current required from pin 7 is 10 μA, an external resistor (Rx) may be inserted in series with R1 from pin 7 to pin 3.

Recommended range for value of Rx is shown in Figure 2.

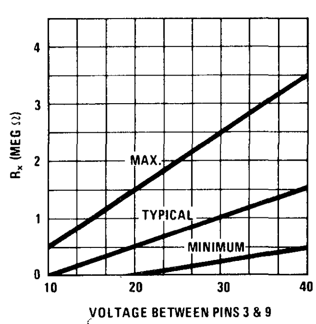


Figure 2. Range of Resistor Values Inserted from Pin 7 to Pin 3 when Pin 7 is not grounded.

Clamped Output Swing

The output voltage can be quite effectively held between specified limits by means of diode clamps on pin 10. From Figure 3 which is the output section of the NH0001, clamping pin 10 will maintain the output within one V_{BE} of pin 10. Since $I_{B(+)}$ and $I_{B(-)}$ are limited to approximately 75 μA at 25°C, the extra quiescent current is quite nominal.

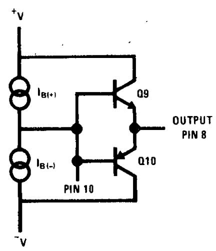


Figure 3. Output of NH0001

A specified output range may be obtained by appropriate connection of diodes from pin 10 to the reference limits. Figure 4 shows the connections for various reference levels.

A typical use of a clamp on pin 10 is to provide compatible drive for either DTL or T^2L logic circuits. This is usually accomplished with a 5 volt Zener diode or the emitter-base junction of a switching transistor such as the 2N2369. Figure 5 shows the NH0001 used as a comparator with a diode clamp on pin 10.

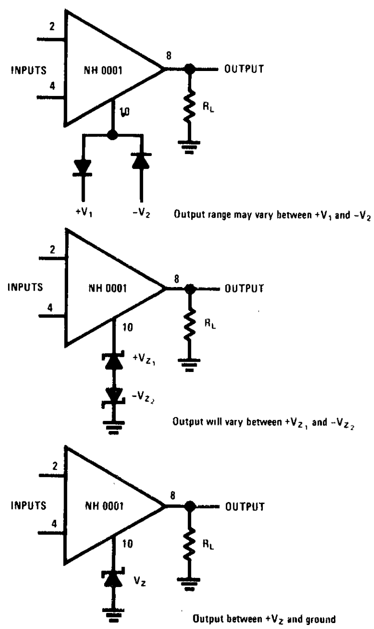


Figure 4. Methods of Restricting Output Voltage Swing.

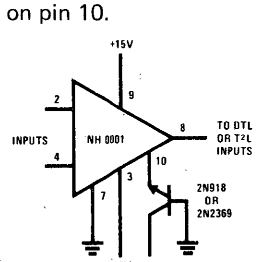


Figure 5A. NH 0001 As Comparator For Driving DTL or T^2L.

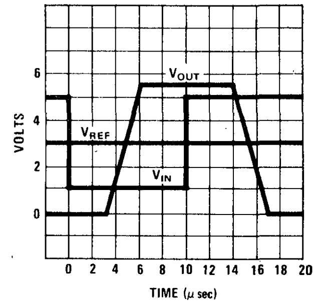


Figure 5B. Output Waveform When Used in Circuit of Fig. 5A.

For driving MOS inputs or clocks, the NH0001 is connected as follows:

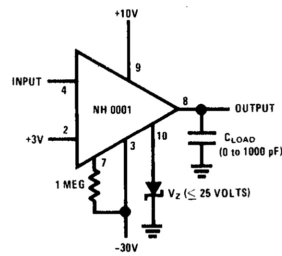


Figure 6A. NH 0001 As Comparator For Driving MOS.

Delay and storage times of 3 to 5 μsec will be observed with rise and fall voltage rates of 2 to 4 volts/μsec. Capacitance loads of up to 1000 pF will not noticeably increase the switching times.

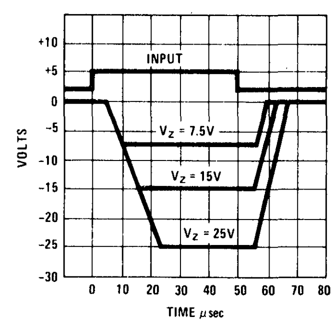


Figure 6B. Output Waveform For Circuit of Fig. 6A.

Input Offset Voltage Balancing

Although the offset voltage of the NH0001 is quite low, it is possible that even lower values are required. Figure 7 shows the recommended balancing technique.

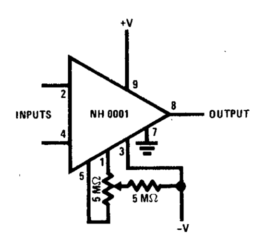


Figure 7. Method of Balancing Input Offset Voltage.

Input Bias Current Compensation

Methods of compensation recommended in NS Application Note AN-3 can all be successfully used with the NH0001 with the exception that all polarities are reversed and NPN bias transistors substituted for the PNP units. Transistor type 2N2484 units are recommended, For optimum compensation over a wide temperature range, the method of generating the emitter current of the compensating transistor shown in Figure 4 and 6 of AN-3 should be modified to be similar to the current source used in the NH0001. Figure 8 shows the recommended circuit.

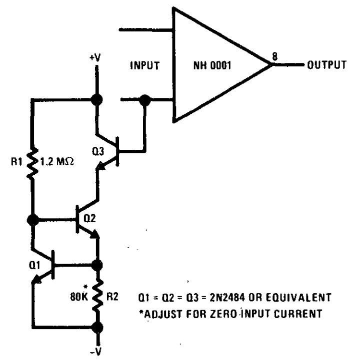


Figure 8. Method of Compensating for Input Bias Current.

Increased Output Swing

For lightly loaded outputs (RL $\geq$ 10K), the maximum negative output swing will exceed the positive swing by approximately a volt. If the maximum positive swing is required, it may be obtained by connecting a low capacitance (C $\leq$ 2 pF at zero volts) diode between pins 1 and 5, with the cathode on pin 1. Table 1 shows the typical positive and negative swing with RL = 100 KΩ both with and without the diode clamp.

TABLE 1 Maximum Output Swings vs Supply Voltage

Supply Voltage	±5V	±10V	±15V	±20V
Typical Negative Output	3.8	8.8	13.5	18.4
Typical Positive Output without Diode Clamp	2.7	7.6	12.2	17.0
Typical Positive Output with Diode Clamp	3.6	8.4	13.0	18.0

$T_A = 25°C$

As explained in the following section, the inclusion of a diode from pin 1 to 5, in addition to increasing the available positive output voltage, will also reduce the maximum positive short circuit current.

Reducing the Short-Circuit Current

As mentioned above, a diode connected from pin 1 to pin 5 will reduce the positive output short circuit current. If the polarity of the diode is reversed, the negative short circuit current will be similarly reduced. If 2 diodes are connected from pins 1 to 5 in opposite directions, the short circuit current will be reduced in both the positive and negative direction.

Figure 9 shows the connections and Figure 10 gives the typical short circuit currents available both with and without the diode clamps.

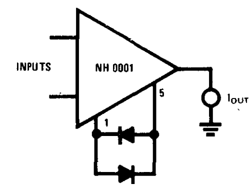


Figure 9. Method of Reducing Output Short Circuit Current.

If this control is not adequate, external limiting as shown in Figure 11 can be used to limit I_{OUT} to less than 1 mA.

Referring to Figure 2, in the limiting mode, the V_{BE} of the conducting output transistors (Q9 or Q10) will add to the drop across R_{LIM} to be equal to the sum of the two forward drops of conducting diodes between pin 10 and the output. Thus the output current will be limited to that value which causes approximately one diode forward

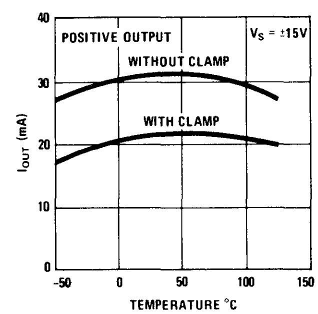


Figure 10A. Short Circuit Output Current.

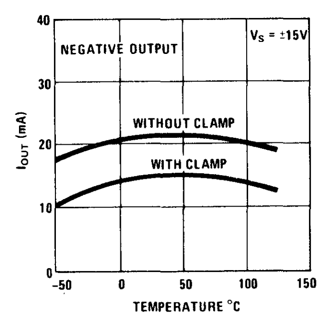


Figure 10B. Short Circuit Output Current.

drop across R_{LIM}. In addition, the diode current which may be as high as 75 μA at 25°C will be added to the output current.

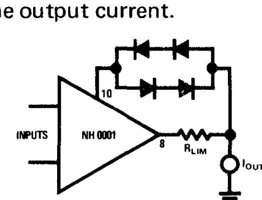


Figure 11. Alternate Method of Limiting Output Short Circuit Current.

Typical Performance of the NH0001 Operational Amplifier ($V_S = \pm 15V$, $T = 25°C$)

PARAMETER	CONDITION	VALUE
Input Offset Voltage	$R_S \leq 5K$	0.2 mV
Input Offset Current		3 nA
Input Bias Current		30 nA
Positive Supply Current		80 μA
Negative Supply Current		55 μA
Voltage Gain	$R_L = 100K$	60,000
Output Voltage	$R_L = 100K$	±12V
CMRR	$R_S \leq 5K$	90 dB
PSRR	$R_S \leq 5K$	96 dB
Temperature Range		−55°C to 125°C
Temperature Drift		4 μV/°C
Supply Voltage Range		±5V to ±20V

REFERENCE:

R. J. Widlar, "Drift Compensation Techniques for Integrated DC Amplifiers" AN-3, National Semiconductor, April, 1968.

September 1968

APPLICATION OF THE NH0002 CURRENT AMPLIFIER

INTRODUCTION

The NH0002 Current Amplifier integrated building block provides a wide band unity gain amplifier capable of providing peak currents of up to ±200 mA into a 50 ohm load.

The circuit uses thick film technology to integrate 2 NPN and 2 PNP complementary matched silicon transistors with 4 cermet resistors on a single alumina ceramic substrate. A circuit schematic is shown in Figure 1. The negative thermal feedback provided by the close proximity of the components on a single substrate eliminates any thermal runaway problem that could occur if this circuit were constructed using discrete components.

A typical circuit features a dynamic input impedance of 200 Kohms, an output impedance of 6 ohms, DC to 50 MHz bandwidth, and an output voltage swing that approaches supply voltage. A complete list of the guaranteed and typical values for the electrical characteristics under the stated conditions is given in Table 1. These features make the NH0002 ideal for integration with an operational amplifier inside a closed loop configuration

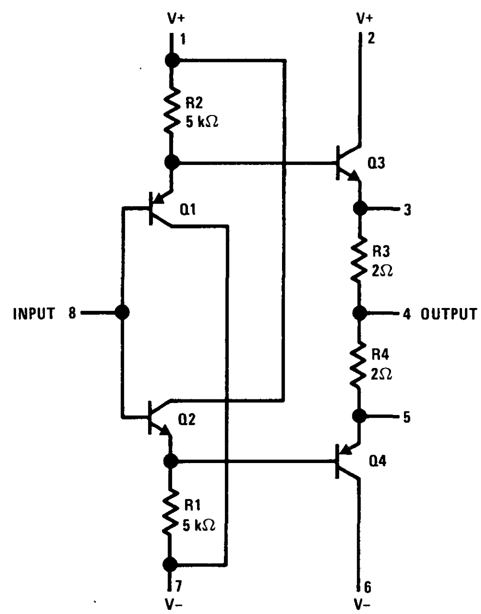


FIGURE 1. Circuit Schematic

TABLE 1. Electrical characteristics, specification applies for T_A = 25°C with +12.0V on pins 1 and 2; −12.0V on pins 6 and 7.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain	R_S = 10 kΩ, R_L = 1.0 kΩ V_{IN} = 3.0 V_{PP}, f = 1.0 kHz T_A = −55°C to 125°C	.95	.97		
Input Impedance	R_S = 200 kΩ, V_{IN} = 1.0 V_{rms}, f = 1.0 kHz, R_L = 1.0 kΩ	180	200	–	kΩ
Output Impedance	V_{IN} = 1.0 V_{rms}, f = 1.0 kHz R_L = 50Ω, R_S = 10 kΩ	–	6	10	Ω
Output Voltage Swing	R_L = 1.0 kΩ, f = 1.0 kHz	±10	±11	–	V
DC Input Offset Voltage	R_S = 10 kΩ, R_L = 1.0 kΩ T_A = −55°C to 125°C	–	±40	±100	mV
DC Input Offset Current	R_S = 10 kΩ, R_L = 1.0 kΩ T_A = −55°C to 125°C	–	±6.0	±10	μA
Harmonic Distortion	V_{IN} = 5.0 V_{rms}, f = 1.0 kHz	–	0.1	–	%
Bandwidth	V_{IN} = 1.0 V_{rms}, R_L = 50Ω, f = 1 MHz	30	50	–	MHz
Positive Supply Current	R_S = 10 kΩ, R_L = 1 kΩ	–	+6.0	+10.0	mA
Negative Supply Current	R_S = 10 kΩ, R_L = 1 kΩ	–	−6.0	−10.0	mA

to increase its current output. The symmetrical class B output portion of the circuit also provides a constant low output impedance for both the positive and negative slopes of output pulses.

CIRCUIT OPERATION

The majority of circuit applications will use symmetrical power supplies, with equal positive voltage being applied to pins 1 and 2, and equal negative voltage applied to pins 6 and 7. The reason that pin 2 and pin 6 are not connected internally to pin 1 and pin 7, respectively, is to increase the versatility of circuit operation by allowing a decreased voltage to be applied to pins 2 and 6 to minimize the power dissipation in Q3 and Q4. The larger voltage applied to the input stage also provides increased current drive as required to the output stage.

The operation of the circuit can be understood by considering that the input pin 8 is at V_{IN}. The emitter of Q1 will be approximately 0.6 volt more positive than V_{IN} at 25°C, and the converse is true for Q2. This 0.6 volt will provide a forward bias on Q3 to cancel out the Q1 base to emitter drop which in turn would provide V_{IN} at the output if all junctions, resistors, power supplies, etc., were electrically identical. The greatest error is introduced because the forward drops in the base-emitter junctions for the NPN and PNP devices are slightly different. For example, the V_{BE} of the NPN will be typically 0.6V and the V_{BE} of the PNP will be typically 0.64V under the same conditions of $I_C = 2.4$ mA at $V_{CE} = 12.0$V at 25°C. These are the approximate input stage circuit conditions for Q1 and Q2 for plus and minus 12V supplies. Fortunately, this error in both input and output offset voltage is almost always negligible when it is used inside the closed loop of a high gain operational amplifier.

A plot of input impedance vs frequency is shown in Figure 2. Inspection of this plot shows that the input impedance can be closely approximated to that of a simple first order linear network with a 45° phase lag at 0.6 MHz and a 90° phase lag at approximately one decade higher in frequency. This information is very useful for designers who have to integrate circuits which have large source

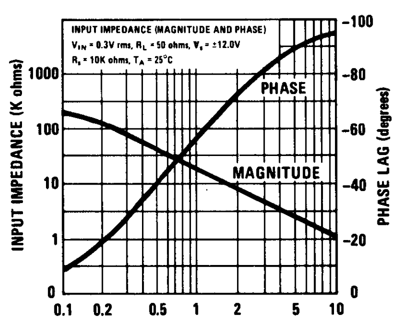


FIGURE 2. Input Impedance vs Frequency

impedances over a wide frequency range. The output impedance of the amplifier is very low, 6 ohms typically, and in conjunction with a voltage bandwidth of approximately 50 MHz can be considered to be insignificant for most applications for this type of device.

A plot of the voltage bandwidth is shown in Figure 3. Inspection of this plot shows that phase information as well as gain information was included to assist users of this device. For example, at 10 MHz, less than an 8° phase lag would be subtracted from the phase margin of an operational amplifier when it is integrated with this device. The open loop gain of the operational amplifier would be decreased by less than 10% at 10 MHz and therefore can be considered to be insignificant for most applications.

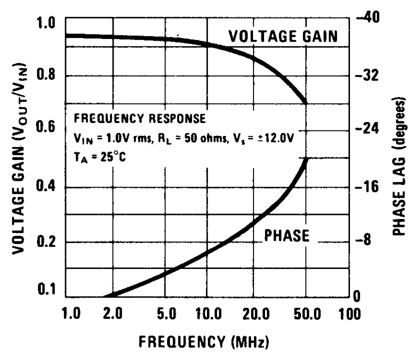


FIGURE 3. Frequency Response

APPLICATIONS

Figure 4 shows the NH0002 integrated with the NH0005 to provide differential inputs and outputs. In order for this circuit to funtion properly, a load must be floated between the outputs of the two devices to provide a complete loop of feedback. A differential head on a scope across the load presents a true waveform of the actual signal being applied to it. If only one end of the load is displayed, it will appear distorted because this information is being fed back negatively to the input in order to cancel out the loop distortion of the overall amplifier. With the compensation shown, a 20V peak to peak signal can be applied to a 100 ohm load to 80 KHz. The overall circuit is approximately 33% efficient under these conditions. A derating factor and/or heat sink must be used at higher temperatures, as shown by the NH0002 and NH0005 data sheets.

Additional output power could also be obtained by connecting another NH0002 to pin 9 of the operational amplifier. The overall load distortion under high circuit voltage gain configurations would also be reduced using two NH0002's because the NH0002 is more linear than the simple output circuits of these particular operational amplifiers.

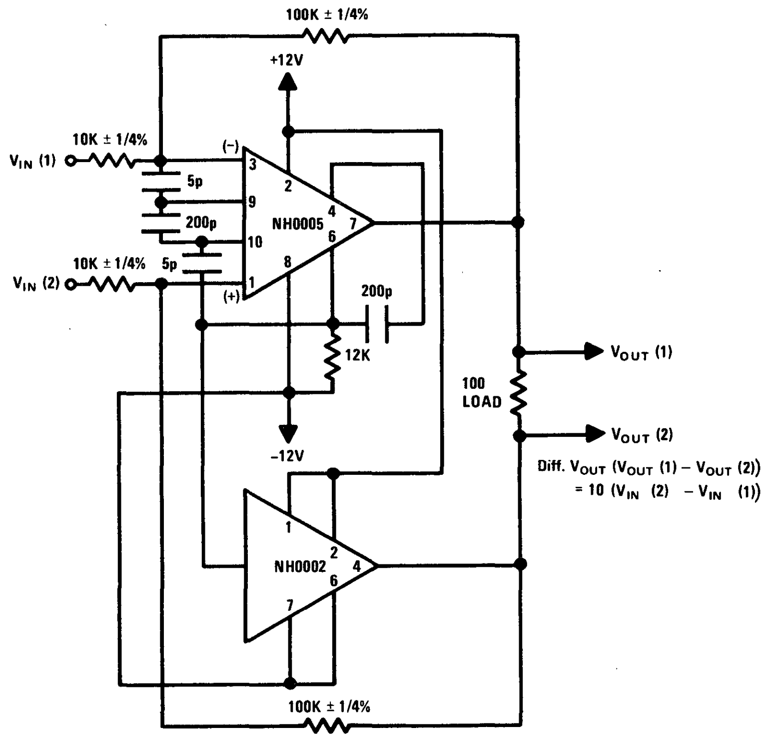


FIGURE 4. Differential Input-Output Operational Amplifier Integration

Figure 5 shows the NH0002 integrated with the LH101 in a booster follower configuration. The configuration is stable without the requirement for any external compensation; however, it would behoove the designer to be conservative and bypass both the negative and positive power supplies with at least a 0.01 μf capacitor to cancel out any power supply lead inductance. A 100 ohm damping resistor, located right at the input of the NH0002, might also be required between the operational amplifier and the booster amplifier. The physical layout will determine the requirement for this type of oscillation suppression. Current limiting can be added by incorporating series resistors from pins 2 and 6 to their respective power supplies. The exact value would be a function of power supply voltage and required operating temperature.

A breadboard of this configuration was assembled to empirically check the increase in offset voltage due to the addition of the NH0002. The offset voltage was measured with and without an NH0002 inside the loop with a voltage gain of 100, at –55°C, 25°C and 125°C. The additional offset voltage was less than 0.3% for all three temperature conditions even though the offset voltage of the NH0002 is much higher than that of the LH101. The high open loop gain of the LH101 divides out this source of circuit error. The integration of this device also allows higher closed loop circuit gain without excessive cross-over distortion than would be obtainable with the simple booster amplifier shown in Figure 6.

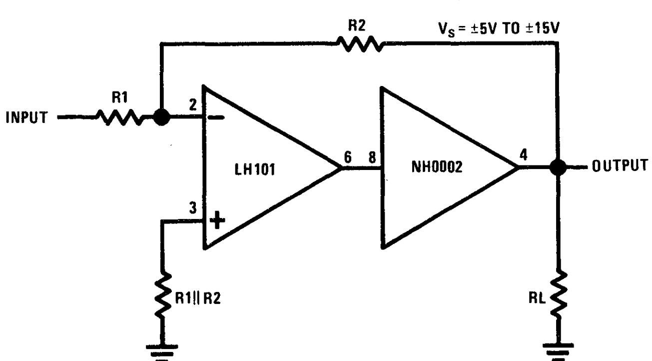


FIGURE 5. LH101-NH0002 Booster Amplifier Integration

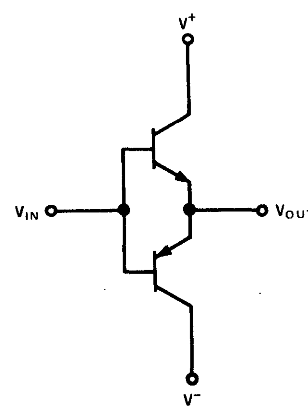


FIGURE 6. Simple Booster Amplifier

Figure 7 shows the NH0002 being used as a level shifter with a high pass filter on the input in order to reference the output to zero quiescent volts. The purpose of the 10 Kohm resistor is to provide current bias to the circuit's input transistors to reduce the output offset voltage. Figure 3, Input Impedance vs Frequency, provides a useful design aid in order to determine the value of the capacitor for the particular application. The 10 Kohm resistor, of course, has to be considered as being in parallel with the circuit's input impedance.

For a pulse input signal, the output impedance of the circuit remains low for both the positive and negative portions of the output pulse. This circuit provides both fast rise and fall times for pulse signals, even with capacitive loading. The NH0002 data sheet shows typical rise and fall times for both positive and negative pulses into a 50 ohm load.

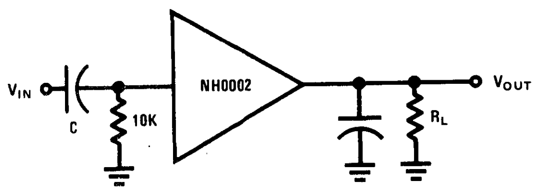


FIGURE 7. Level Shifter

Figure 8 shows the NH0002 being used to drive a pulse-transformer. The low output offset voltage allows the pulse transformer to be directly coupled to the amplifier without using a coupling capacitor to prevent saturation. The pulse transformer can be used to change the amplitude and impedance level of the pulse, the polarity of the pulses, or, with the aid of a center-tapped winding, positive and negative pulses simultaneously.

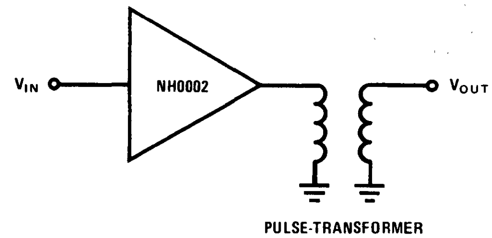


FIGURE 8. Driver for a Pulse-Transformer

The NH0002 can also be used to drive long transmission lines. Figure 9 shows a circuit configuration to match the output impedance of the amplifier to the load and coaxial cable for proper line termination to minimize reflections. A capacitor can be added to empirically adjust the time response of the waveform.

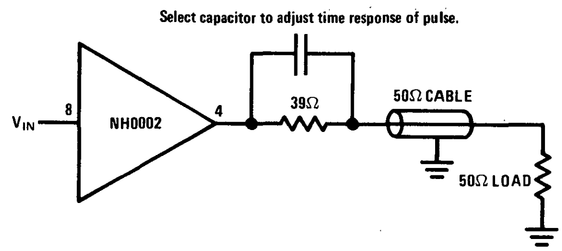


FIGURE 9. Transmission Line Driver

SUMMARY

The multitude of different applications suggested in this article shows the versatility of the NH0002. The applications specially covered were for a differential input-output operational amplifier, booster amplifier, level shifter, driver for a pulse-transformer, and transmission line driver.

August 1968

A COMPLETE MONOLITHIC IF STRIP FOR AM/AGC APPLICATIONS

INTRODUCTION

Intermediate-frequency amplifiers in superheterodyne receivers and signal-frequency amplifiers in T.R.F. receivers have traditionally been partitioned into a number of discrete power-gain stages, with interstage networks performing both DC decoupling and bandpass shaping functions. As long as the active components (vacuum tubes or transistors) comprised a substantial part of the "strip's" total cost, it made sense to design on a "cost-per-stage" basis.

A number of currently available microcircuits, such as types LM703 and LM171, provided a transitional opportunity for RF system designers to use proven interstage network designs, substituting the self-contained, inherently stable, high gain-bandwidth product microcircuit directly for a conventional common-emitter IF stage. While the excellent FM limiting and AGC characteristics of such monolithic stages have already proven themselves in commercial and entertainment equipment, they have usually constituted performance, rather than cost, advantages to the system manufacturer.

Monolithic technology has already emerged, in the digital area, from an initial period of novelty and a subsequent period of superior performance, into the current realization that, against MSI or LSI, discrete transistor computing systems cannot be competitive. The linear circuit to be described, a multifunction IF strip, is a step in the same direction, in which a number of discrete circuit functions have been combined, replacing not only the active elements and DC biasing components, but eliminating many of the peripheral IF elements as well.

A SYSTEM APPROACH

Monolithic techniques allow a rethinking of traditional IF strip partitioning. Previously, the most efficient utilization of available power gain was obtained by matched, tuned, interstage networks. Because of the limited AGC range obtainable by varying DC emitter current in a conventional common-emitter IF stage, several stages received AGC voltage from the detector at once. This dictated combersome DC biasing to obtain the desired AGC characteristic, and made an input and an output transformer mandatory for each stage, to decouple DC-operating point shifts due to AGC operation.

Economics dictated the simplest detector schemes, usually a single diode, biased from a tuned transformer secondary. AGC voltage was usually obtained directly from the diode detector. Generally, because of large tuned gain and, often, marginal stability in the conventional common-emitter stage, power-supply decoupling was required for each stage.

Suppose, however, that the above requirements are largely eliminated by availability of almost unlimited monolithic complexity and inherent internal biasing. It would be much more efficient to put all power gain in a single, lumped stage, preceded by a single (perhaps multisection, for selectivity) bandpass filter. This would considerably reduce the assembly and alignment labor in an AM receiver. Rather than deal with the sizeable problems of AGC in direct-coupled, high-gain amplifiers, a simpler approach is to achieve full gain-control range through a high-performance variable attenuator stage, between the input bandpass filter and the input to the lumped gain stage, leaving the lumped gain stage at its maximum gain at all times. Finally, an AM detector is desirable which can be directly coupled to the gain stage output, which is insensitive to DC biasing, and which reliably provides a DC AGC voltage compatible with the input variable attenuator. A block diagram of the new subsystem appears in Figure 1.

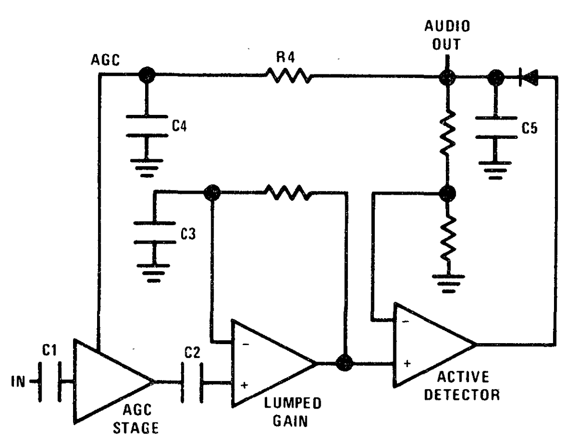
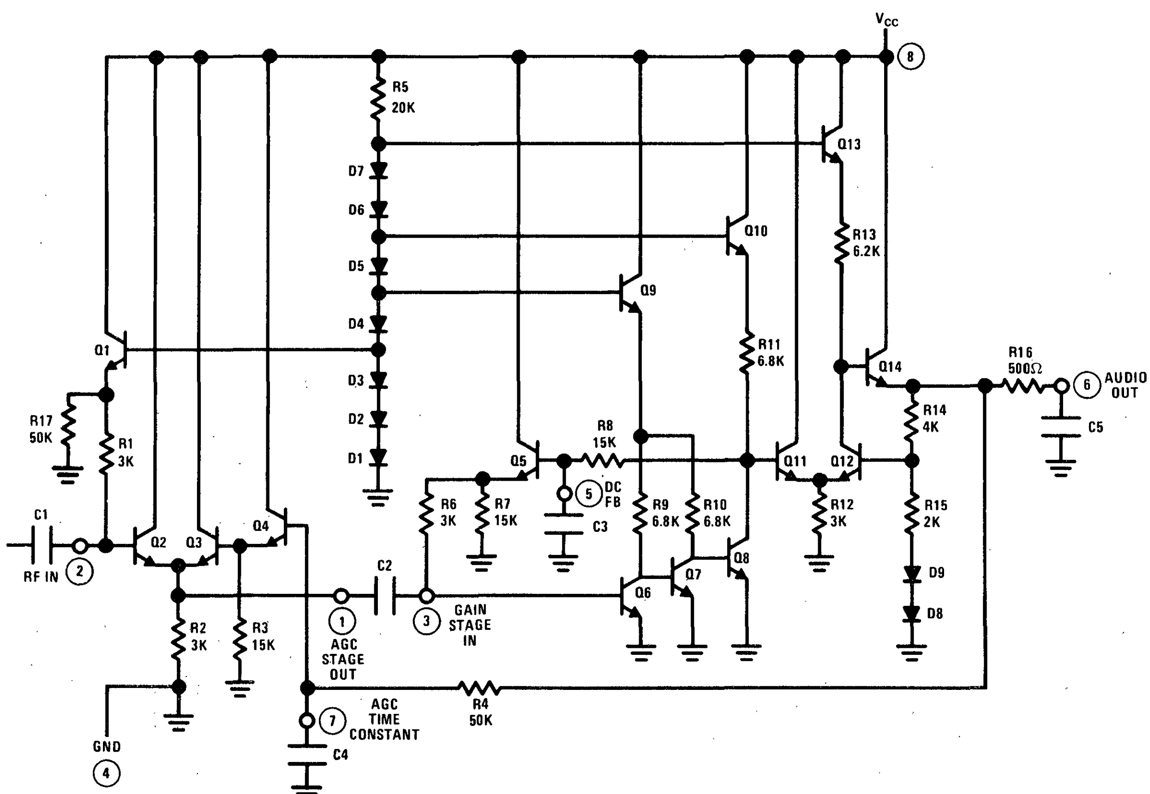


FIGURE 1. LM172 Block Diagram

A PRACTICAL MONOLITH

A complete schematic for National Semiconductor's AM IF Strip, the LM172/272, appears in Figure 2. All capacitors shown are external to the 8 pin, TO5 package; these capacitors establish the minimal amount of decoupling and time constants required to operate such a complex, high gain-bandwidth product microcircuit.

Examining first the AGC section, Figure 3, it may be seen that an emitter-coupled pair is used as a series-shunt variable attenuator. The base of Q2 is held at a DC voltage of two forward diode drops, 2 V_{be}, by emitter follower Q1 and R1, with only AC signals coupled through an input capacitor. If V_{AGC} is held below 3 V_{be}, Q3 will be completely off, and Q2 behaves as an ordinary emitter follower, with R2 as load. When V_{AGC} equals 3 V_{be}, Q2 and Q3 form a balanced differential pair, conducting equal emitter currents from "current source" R2, and as V_{AGC} increases, Q3 turns increasingly on, with Q2 turning off. As this occurs, the effective emitter resistance of Q2 increases, in series with the input signal, while the emitter resistance of Q3 decreases, shunting across the signal. Thus, Q2 and Q3 form a series-shunt attenuator, with minimum attenuation of 0 dB. Since the base of Q2 remains at a fixed bias, while that of Q3 increases with AGC, the DC output voltage at the common emitter point rises slightly as gain is decreased. Consequently, a decoupling capacitor is needed between the AGC stage and the lumped-gain stage, to prevent unbiasing the gain stage with AGC variations.



pin numbers appear in circles

FIGURE 2. LM172 AGC AM IF Strip

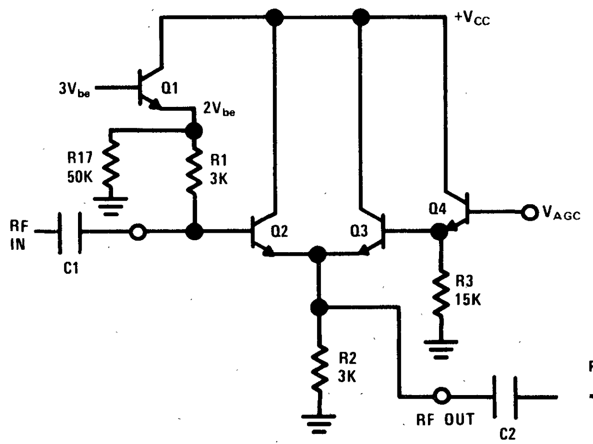


FIGURE 3. AGC Section

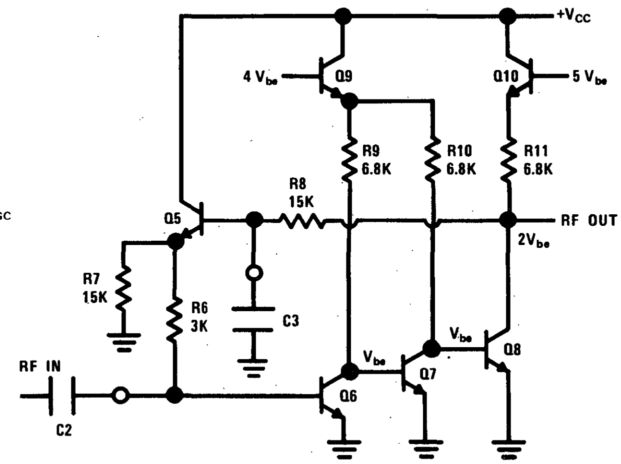


FIGURE 4. Lumped Gain Stage

The lumped-gain stage, Figure 4, is basically a cascade of three common-emitter amplifiers, direct-coupled. A conventional, discrete transistor version of this cascade would require much more complex, less-efficient DC biasing. Notice that no emitter resistors are used; this gives maximum voltage gain per stage, but still allows reliable biasing, since an overall DC feedback loop, R8, C3, Q5 and R6, automatically sets the DC output voltage of each transistor to exactly the right level to correctly bias the following transistor. The feedback loop is effective only for DC, because of the R8-C3 rolloff; thus maximum AC gain is always attained with DC stability. Notice that the collectors of Q6 and Q7 are operated at V_{be}, to satisfy biasing of following stages; thus, they operate with zero volts collector to base, and still exhibit excellent current gain and gain-bandwidth product, by virtue of their very small geometries and low-saturation voltages. The three collector-load resistances, R9, R10 and R11, are biased from their own emitter-follower voltage regulators, which eliminate supply decoupling problems, and allow the active part of the circuit to operate with constant bias conditions, regardless of power-supply voltage. Since each part of the circuit is supply-regulated in this way, supply current does not increase linearly with supply voltage, as in most designs, but remains relatively constant. Thus, the circuit remains highly efficient at low-supply voltages, without excessive drain at higher voltages.

A number of improvements may be made over the conventional AM diode detector. Unless simple diodes are slightly forward-biased by additional circuitry, they will not respond to small-input signals, because of the voltage required to overcome forward V_{be}. Moreover, diode detectors are inefficient, generally giving less audio output than is available from the modulated carrier. A more nearly ideal detector, Figure 5, is one found in most operational amplifier handbooks. If gain of the operational amplifier is sufficiently high, audio output exactly follows modulation envelope; since the diode is inside a feedback loop, the operational amplifier will automatically bias the diode to respond to small signals. When no carrier is present, DC output voltage is zero. An unmodulated carrier causes DC output voltage to rise to one-half the peak-to-peak RF level. Superimposing audio modulation on the carrier has no effect on the average, or DC output voltage, but causes the RC network to "follow" the modulation envelope on the positive side of the carrier.

A simple modification to the active detector of Figure 5 is the addition of a resistive divider, Figure 6. While basic operation remains unchanged, the active detector now has an audio and DC voltage gain equal to $(R1 + R2)/R2$. Such a detector can perform some of the audio preamplification necessary in the radio receiver.

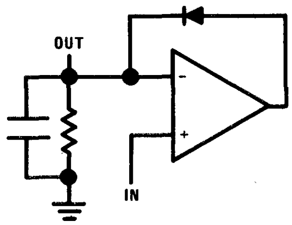


FIGURE 5. Unity Gain Active Dector

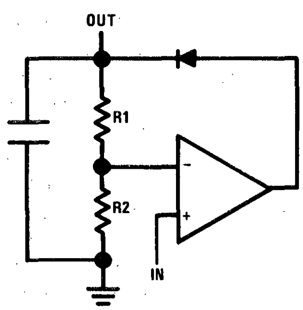


FIGURE 6. Active Detector with Voltage Gain

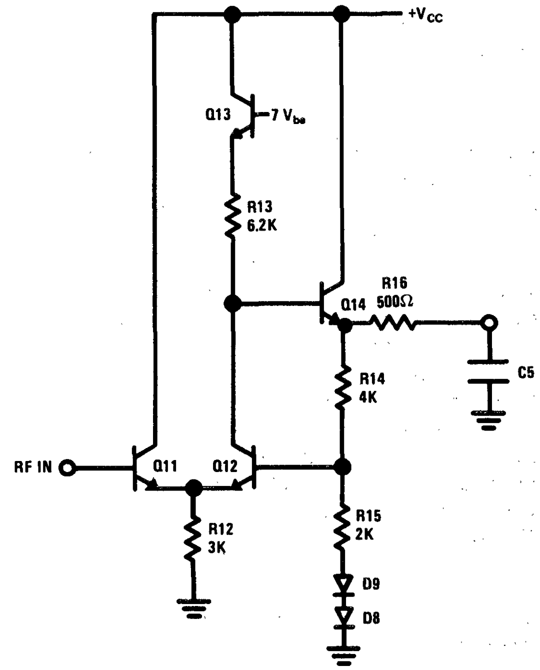


FIGURE 7. Active Detector

The actual active detector used in the LM172 is a differential amplifier, Figure 7, with an emitter follower performing the function of the feedback diode. While not an operational amplifier, the circuit's voltage gain of about 40 dB is sufficient to provide excellent detection. Because an emitter follower was substituted for the diode, output impedance is low; it would, in fact, be too low for effective carrier ripple filtering by C5, if it were not for the addition of R16. A resistive divider, R14 and R15, give the detector an audio voltage gain of 3, with D8 and D9 compensating for the DC voltage (2 V_{be}) superimposed on the RF input voltage by the preceding lumped gain stage. Q13 acts as a supply regulator for the differential amplifier.

The entire circuit fits on a small 33 x 33.5 mil monolithic chip (Figure 8), and in view of the self-contained feedback loops, which automatically compensate for component parameter variations, is an unusually reproducible microcircuit.

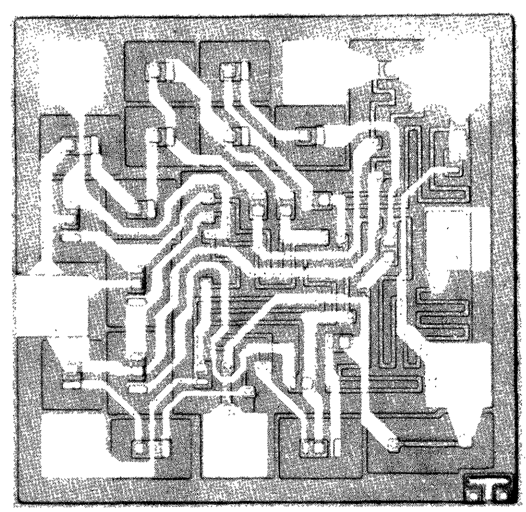


FIGURE 8. Chip Photo

LM172 APPLICATIONS

SUPERHETERODYNE RECEIVER IF STRIP

By far the most popular receiver configuration, in military, two-way-radio and entertainment use, is one in which the incoming signal is amplified, and then translated, via a mixer, to a standard intermediate frequency, where most of the receiver's voltage gain and selectivity is achieved. A typical system appears in Figure 9. Conventional circuitry may be used ahead of the LM172; although a double-section 455 kHz ceramic filter is shown, LC filtering may be used if desired. The circuit works effectively for IF frequencies between 50 kHz and 2 MHz, depending on input bandpass components. Capacitors C2, C3 and C5 should be scaled proportionately at frequencies other than 455 kHz.

The circuit of Figure 9 exhibits the following IF characteristics:

AGC Range (referred to Pin 2) from 50 μV to 50 mV: 60 dB

Audio output for 80% modulated carrier, within AGC range: 0.8V p-p

Total Supply drain into LM172, V_{CC} = +6V: 1.4 mA, or 8.4 mW.

Improved selectivity may be obtained by substituting another ceramic filter between Pins 1 and 3, instead of C2. The 3K impedances at Pins 1, 2 and 3 are especially suited to the inexpensive Murata filters. While audio distortion occurs for voltages at Pin 2 much above 100 mV rms. distortion is low for signals within the AGC range of the circuit. Gain in the RF amplifier and mixer must therefore be chosen to provide signals less than 100 mV into Pin 2 for the desired range of RF input levels. Additional AGC is possible by using the DC voltage appearing at Pin 7 to control the gain of the input RF amplifier. Since AGC action occurs at and above 3 V_{be}, the National LM171 RF/IF Amplifier, operated as a cascode, is ideally suited to such front-end control, as its gain-control voltage region coincides with that of the LM172.

Because of the built-in supply regulation, the strip operates with supply voltage varying from +6 to +15 volts with no perceptible changes in receiver performance.

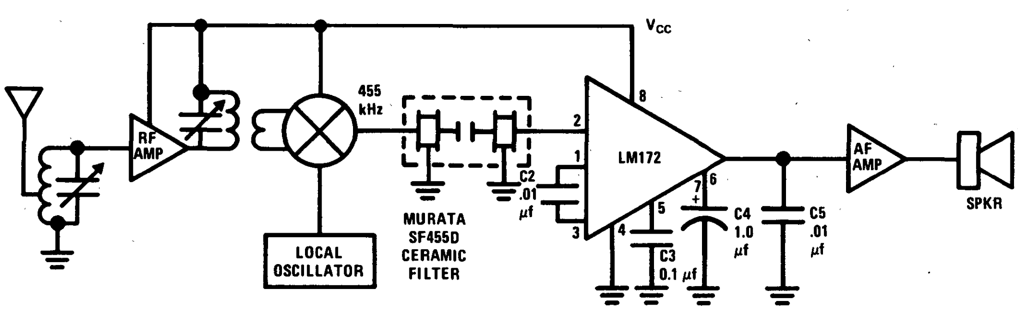


FIGURE 9. Superheterodyne Block Diagram

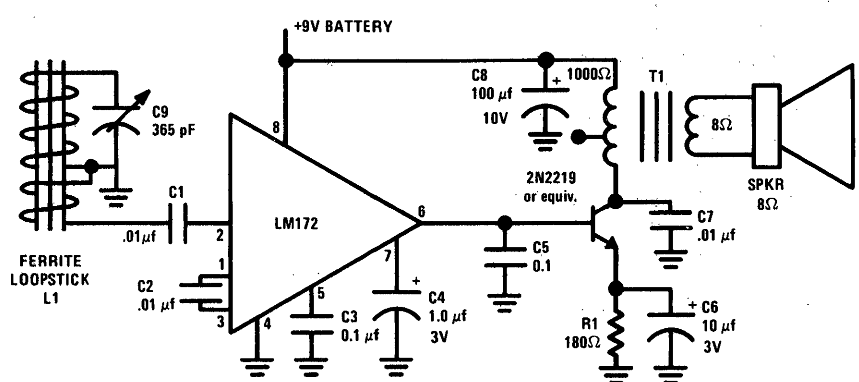
LOW FREQUENCY T.R.F. RECEIVER

Because the LM172 is a broadband functional module, it may be used to amplify and detect signals below 2 MHz directly, without the more complex frequency conversion of superheterodyne receivers. In the AM Broadcast Band (550-1650 kHz), the strip has sufficient sensitivity to operate alone in urban reception areas, since AGC action is useful down to about 50 microvolts at Pin 2. With additional gain either preceding the module, or inserted between Pins 1 and 3, it may also be useful in monitoring Loran (1.8-2.0 MHz), or the numerous directional and informational channels below 550 kHz.

While the complete T.R.F. (Tuned Radio Frequency) broadcast receiver of Figure 10 has relatively poor selectivity, because only a single, low "Q" tuned circuit is used in the entire receiver, it serves to illustrate the straightforward design possible in T.R.F. construction. More sophisticated designs might use multisection tuning, ahead of the strip. The prototype was constructed using very inexpensive imported "transistor-radio" components.

A ferrite "loopstick" antenna, L1, resonates with a small, polyethylene dielectric tuning capacitor within the broadcast band. The LM172 performs its gain function just as it would in an IF application, but in this case, directly drives a class A power amplifier. Since the DC output voltage at Pin 6 is relatively constant (from 2.1 to about 2.4 volts as a function of AGC), it is used to bias the class A stage directly, eliminating a number of components. C7 and C8 are needed to prevent regenerative audio oscillations with weak batteries. Total receiver drain from the 9-volt supply is 10 mA, of which only 1.9 mA is used in the LM172; the rest is needed for the audio amplifier.

A volume control was not provided in the prototype, as volume was excellent with the small (2" diameter) speaker used, and AGC was so effective that no perceptible difference in stations was heard. Volume control is possible by inserting a potentiometer between the emitter of the audio output transistor and R1.



L1 – Ferrite Loopstick – Philmore FF15 (packaged as set of 3 sizes)
C9 – Sub-miniature variable capacitor – Philmore 1949G – 365 pF max.
T1 – Midget Audio Transformer, 1000Ω:8Ω – Archer ⌞73-1380 (Radio Shack, Inc.)
SPKR – 2" PM Speaker, 8Ω, 0.1 watt – Philmore TS20

FIGURE 10. T.R.F. Broadcast Receiver

February 1969

AN APPLICATIONS GUIDE FOR OPERATIONAL AMPLIFIERS

INTRODUCTION

The general utility of the operational amplifier is derived from the fact that it is intended for use in a feedback loop whose feedback properties determine the feed-forward characteristics of the amplifier and loop combination. To suit it for this usage, the ideal operational amplifier would have infinite input impedance, zero output impedance, infinite gain and an open-loop 3 dB point at infinite frequency rolling off at 6 dB per octave. Unfortunately, the unit cost—in quantity—would also be infinite.

Intensive development of the operational amplifier, particularly in integrated form, has yielded circuits which are quite good engineering approximations of the ideal for finite cost. Quantity prices for the best contemporary integrated amplifiers are low compared with transistor prices of five years ago. The low cost and high quality of these amplifiers allows the implementation of equipment and systems functions impractical with discrete components. An example is the low frequency function generator which may use 15 to 20 operational amplifiers in generation, wave shaping, triggering and phase-locking.

The availability of the low-cost integrated amplifier makes it mandatory that systems and equipments engineers be familiar with operational amplifier applications. This paper will present amplifier usages ranging from the simple unity-gain buffer to relatively complex generator and wave-shaping circuits. The general theory of operational amplifiers is not within the scope of this paper and many excellent references are available in the literature.[1,2,3,4] The approach will be shaded toward the practical, amplifier parameters will be discussed as they affect circuit performance, and application restrictions will be outlined.

The applications discussed will be arranged in order of increasing complexity in five categories: simple amplifiers, operational circuits, transducer amplifiers, wave shapers and generators, and power supplies. The integrated amplifiers shown in the figures are for the most part internally compensated so frequency stabilization components are not shown; however, other amplifiers may be used to achieve greater operating speed in many circuits as will be shown in the text. Amplifier parameter definitions are contained in Appendix I.

THE INVERTING AMPLIFIER

The basic operational amplifier circuit is shown in Figure 1. This circuit gives closed-loop gain of R2/R1 when this ratio is small compared with the amplifier open-loop gain and, as the name implies, is an inverting circuit. The input impedance is equal to R1. The closed-loop bandwidth is equal to the unity-gain frequency divided by one plus the closed-loop gain.

The only cautions to be observed are that R3 should be chosen to be equal to the parallel combination of R1 and R2 to minimize the offset voltage error due to bias current and that there will be an offset voltage at the amplifier output equal to closed-loop gain times the offset voltage at the amplifier input.

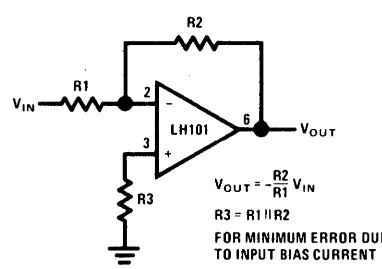


FIGURE 1. Inverting Amplifier

Offset voltage at the input of an operational amplifier is comprised of two components, these components are identified in specifying the amplifier as input offset voltage and input bias current. The input offset voltage is fixed for a particular amplifier, however the contribution due to input bias current is dependent on the circuit configuration used. For minimum offset voltage at the amplifier input without circuit adjustment the source resistance for both inputs should be equal. In this case the maximum offset voltage would be the algebraic sum of amplifier offset voltage and the voltage drop across the source resistance due to offset current. Amplifier offset voltage is the predominant error term for low source resistances and offset current causes the main error for high source resistances.

In high source resistance applications, offset voltage at the amplifier output may be adjusted by adjusting the value of R3 and using the variation in voltage drop across it as an input offset voltage trim.

Offset voltage at the amplifier output is not as important in AC coupled applications. Here the only consideration is that any offset voltage at the output reduces the peak to peak linear output swing of the amplifier.

The gain-frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is the situation of conditional stability. Obviously the most critical case occurs when the attenuation of the feedback network is zero.

Amplifiers which are not internally compensated may be used to achieve increased performance in circuits where feedback network attenuation is high. As an example, the LM101 may be operated at unity gain in the inverting amplifier circuit with a 15 pF compensating capacitor, since the feedback network has an attenuation of 6 dB, while it requires 30 pF in the non-inverting unity gain connection where the feedback network has zero attenuation. Since amplifier slew rate is dependent on compensation, the LM101 slew rate in the inverting unity gain connection will be twice that for the non-inverting connection and the inverting gain of ten connection will yield eleven times the slew rate of the non-inverting unity gain connection. The compensation trade-off for a particular connection is stability versus bandwidth, larger values of compensation capacitor yield greater stability and lower bandwidth and vice versa.

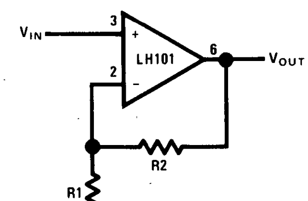
The preceding discussion of offset voltage, bias current and stability is applicable to most amplifier applications and will be referenced in later sections. A more complete treatment is contained in Reference 4.

THE NON-INVERTING AMPLIFIER

Figure 2 shows a high input impedance non-inverting circuit. This circuit gives a closed-loop gain equal to the ratio of the sum of R1 and R2 to R1 and a closed-loop 3 dB bandwidth equal to the amplifier unity-gain frequency divided by the closed-loop gain.

The primary differences between this connection and the inverting circuit are that the output is not inverted and that the input impedance is very high and is equal to the differential input impedance multiplied by loop gain. (Open loop gain/Closed loop gain.) In DC coupled applications, input impedance is not as important as input current and its voltage drop across the source resistance.

Applications cautions are the same for this amplifier as for the inverting amplifier with one exception. The amplifier output will go into saturation if the input is allowed to float. This may be important if the amplifier must be switched from source to source. The compensation trade off discussed for the inverting amplifier is also valid for this connection.



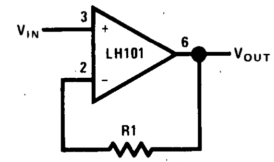
$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$

$R1 \parallel R2 = R_{SOURCE}$
FOR MINIMUM ERROR DUE TO INPUT BIAS CURRENT

FIGURE 2. Non-Inverting Amplifier

THE UNITY-GAIN BUFFER

The unity-gain buffer is shown in Figure 3. The circuit gives the highest input impedance of any operational amplifier circuit. Input impedance is equal to the differential input impedance multiplied by the open-loop gain, in parallel with common mode input impedance. The gain error of this circuit is equal to the reciprocal of the amplifier open-loop gain or to the common mode rejection, whichever is less.



$V_{OUT} = V_{IN}$
$R1 = R_{SOURCE}$
FOR MINIMUM ERROR DUE TO INPUT BIAS CURRENT

FIGURE 3. Unity Gain Buffer

Input impedance is a misleading concept in a DC coupled unity-gain buffer. Bias current for the amplifier will be supplied by the source resistance and will cause an error at the amplifier input due to its voltage drop across the source resistance. Since this is the case, a low bias current amplifier such as the LH102[6] should be chosen as a unity-gain buffer when working from high source resistances. Bias current compensation techniques are discussed in Reference 5.

The cautions to be observed in applying this circuit are three: the amplifier must be compensated for unity gain operation, the output swing of the amplifier may be limited by the amplifier common mode range, and some amplifiers exhibit a latch-up mode when the amplifier common mode range is exceeded. The LH101 may be used in this circuit with none of these problems; or, for faster operation, the LM102 may be chosen.

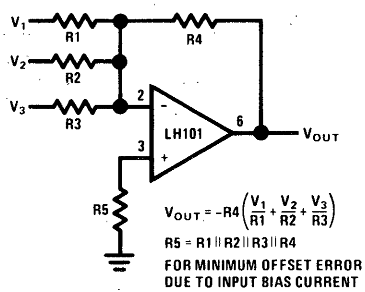


FIGURE 4. Summing Amplifier

SUMMING AMPLIFIER

The summing amplifier, a special case of the inverting amplifier, is shown in Figure 4. The circuit gives an inverted output which is equal to the weighted algebraic sum of all three inputs. The gain of any input of this circuit is equal to the ratio of the appropriate input resistor to the feedback resistor, R4. Amplifier bandwidth may be calculated as in the inverting amplifier shown in Figure 1 by assuming the input resistor to be the parallel combination of R1, R2, and R3. Application cautions are the same as for the inverting amplifier. If an uncompensated amplifier is used, compensation is calculated on the basis of this bandwidth as is discussed in the section describing the simple inverting amplifier.

The advantage of this circuit is that there is no interaction between inputs and operations such as summing and weighted averaging are implemented very easily.

THE DIFFERENCE AMPLIFIER

The difference amplifier is the complement of the summing amplifier and allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to the two inputs. This circuit is shown in Figure 5 and is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.

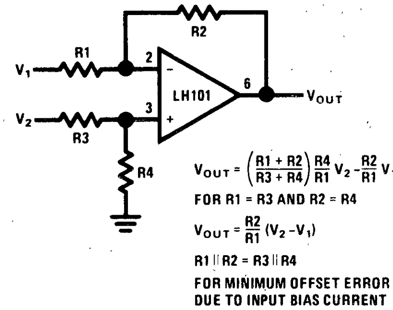


FIGURE 5. Difference Amplifier

Circuit bandwidth may be calculated in the same manner as for the inverting amplifier, but input impedance is somewhat more complicated. Input impedance for the two inputs is not necessarily equal; inverting input impedance is the same as for the inverting amplifier of Figure 1 and the non-inverting input impedance is the sum of R3 and R4. Gain for either input is the ratio of R1 to R2 for the special case of a differential input single-ended output where R1 = R3 and R2 = R4. The general expression for gain is given in the figure. Compensation should be chosen on the basis of amplifier bandwidth.

Care must be exercised in applying this circuit since input impedances are not equal for minimum bias current error.

DIFFERENTIATOR

The differentiator is shown in Figure 6 and, as the name implies, is used to perform the mathematical operation of differentiation. The form shown is not the practical form, it is a true differentiator and is extremely susceptible to high frequency noise since AC gain increases at the rate of 6 dB per octave. In addition, the feedback network of the differentiator, R2C1, is an RC low pass filter which contributes 90° phase shift to the loop and may cause stability problems even with an amplifier which is compensated for unity gain.

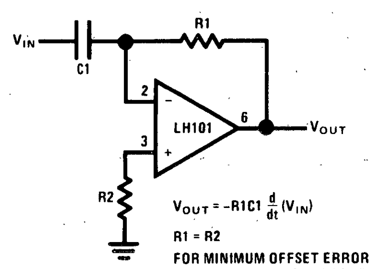


FIGURE 6. Differentiator

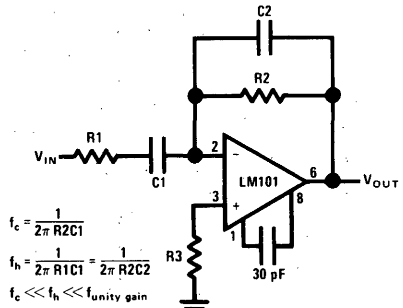


FIGURE 7. Practical Differentiator

A practical differentiator is shown in Figure 7. Here both the stability and noise problems are corrected by addition of two additional components, R1 and C2. R2 and C2 form a 6 dB per octave high frequency roll-off in the feedback network and R1C1 form a 6 dB per octave roll-off network in the input network for a total high frequency roll-off of 12 dB per octave to reduce the effect of high frequency input and amplifier noise. In addition R1C1 and R2C2 form lead networks in the feedback loop which, if placed below the amplifier unity gain frequency, provide 90° phase lead to compensate the 90° phase lag of R2C1 and prevent loop instability. A gain frequency plot is shown in Figure 8 for clarity.

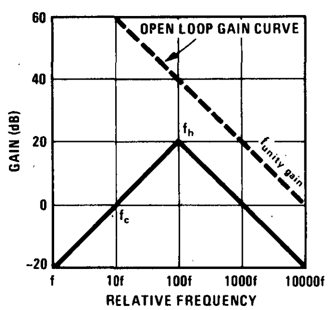


FIGURE 8. Differentiator Frequency Response

INTEGRATOR

The integrator is shown in Figure 9 and performs the mathematical operation of integration. This circuit is essentially a low-pass filter with a frequency response decreasing at 6 dB per octave. An amplitude-frequency plot is shown in Figure 10.

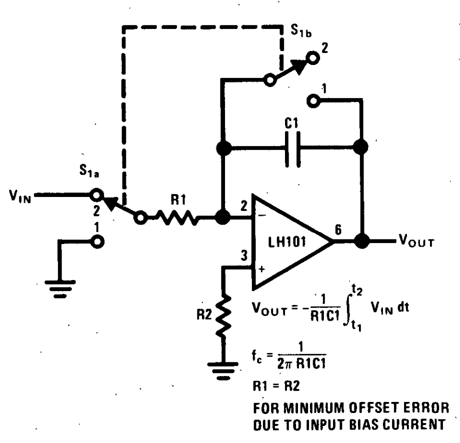


FIGURE 9. Integrator

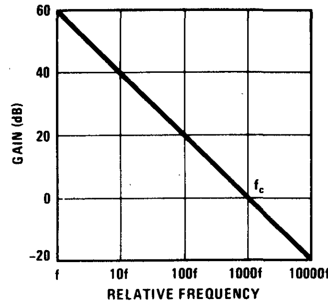


FIGURE 10. Integrator Frequency Response

The circuit must be provided with an external method of establishing initial conditions. This is shown in the figure as S_1. When S_1 is in position 1, the amplifier is connected in unity-gain and capacitor C1 is discharged, setting an initial condition of zero volts. When S_1 is in position 2, the amplifier is connected as an integrator and its output will change in accordance with a constant times the time integral of the input voltage.

The cautions to be observed with this circuit are two: the amplifier used should generally be stabilized for unity-gain operation and R2 must equal R1 for minimum error due to bias current.

SIMPLE LOW-PASS FILTER

The simple low-pass filter is shown in Figure 11. This circuit has a 6 dB per octave roll-off after a closed-loop 3 dB point defined by f_c. Gain below this corner frequency is defined by the ratio of R3 to R1. The circuit may be considered as an AC integrator at frequencies well above f_c; however, the time domain response is that of a single RC rather than an integral.

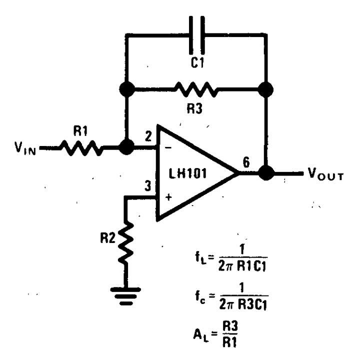


FIGURE 11. Simple Low Pass Filter

R2 should be chosen equal to the parallel combination of R1 and R3 to minimize errors due to bias current. The amplifier should be compensated for unity-gain or an internally compensated amplifier can be used.

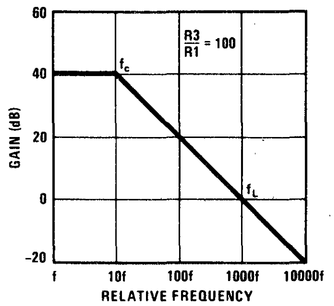


FIGURE 12. Low Pass Filter Response

A gain frequency plot of circuit response is shown in Figure 12 to illustrate the difference between this circuit and the true integrator.

THE CURRENT-TO-VOLTAGE CONVERTER

Current may be measured in two ways with an operational amplifier. The current may be converted into a voltage with a resistor and then amplified or the current may be injected directly into a summing node. Converting into voltage is undesirable for two reasons: first, an impedance is inserted into the measuring line causing an error; second, amplifier offset voltage is also amplified with a subsequent loss of accuracy. The use of a current-to-voltage transducer avoids both of these problems.

The current-to-voltage transducer is shown in Figure 13. The input current is fed directly into the summing node and the amplifier output voltage changes to extract the same current from the summing node through R1. The scale factor of this

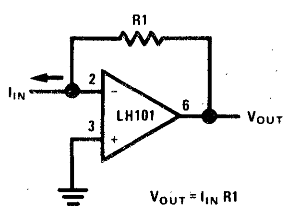


FIGURE 13. Current to Voltage Converter

circuit is R1 volts per amp. The only conversion error in this circuit is I_{bias} which is summed algebraically with I_{IN}.

This basic circuit is useful for many applications other than current measurement. It is shown as a photocell amplifier in the following section.

The only design constraints are that scale factors must be chosen to minimize errors due to bias current and since voltage gain and source impedance are often indeterminate (as with photocells) the amplifier must be compensated for unity-gain operation. Valuable techniques for bias current compensation are contained in Reference 5.

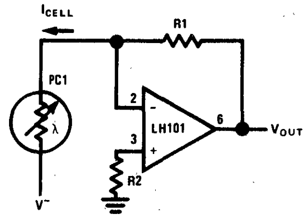


FIGURE 14. Amplifier for Photoconductive Cell

PHOTOCELL AMPLIFIERS

Amplifiers for photoconductive, photodiode and photovoltaic cells are shown in Figures 14, 15, and 16 respectively.

All photogenerators display some voltage dependence of both speed and linearity. It is obvious that the current through a photoconductive cell will not display strict proportionality to incident light if the cell terminal voltage is allowed to vary with cell conductance. Somewhat less obvious is the fact that photodiode leakage and photovoltaic cell internal losses are also functions of terminal voltage. The current-to-voltage converter neatly sidesteps gross linearity problems by fixing a constant terminal voltage, zero in the case of photovoltaic cells and a fixed bias voltage in the case of photoconductors or photodiodes.

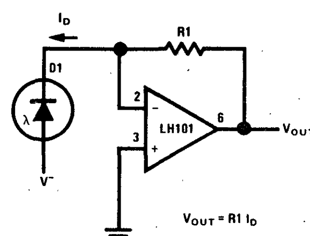


FIGURE 15. Photodiode Amplifier

Photodetector speed is optimized by operating into a fixed low load impedance. Currently available photovoltaic detectors show response times in the microsecond range at zero load impedance and photoconductors, even though slow, are materially faster at low load resistances.

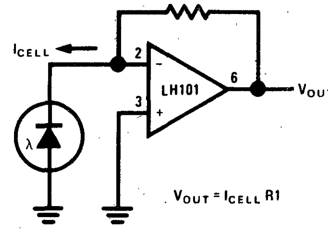


FIGURE 16. Photovoltaic Cell Amplifier

The feedback resistance, R1, is dependent on cell sensitivity and should be chosen for either maximum dynamic range or for a desired scale factor. R2 is elective: in the case of photovoltaic cells or of photodiodes, it is not required in the case of photoconductive cells, it should be chosen to minimize bias current error over the operating range.

PRECISION CURRENT SOURCE

The precision current source is shown in Figures 17 and 18. The configurations shown will sink or source conventional current respectively.

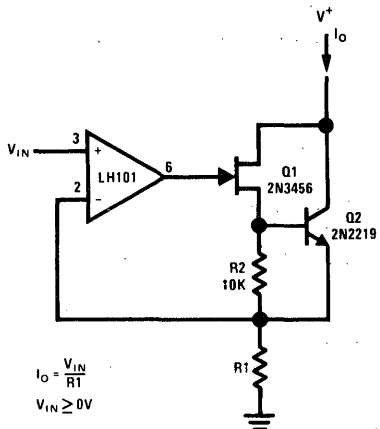


FIGURE 17. Precision Current Sink

Caution must be exercised in applying these circuits. The voltage compliance of the source extends from BV_{CER} of the external transistor to approximately 1 volt more negative than V_{IN}. The compliance of the current sink is the same in the positive direction.

The impedance of these current generators is essentially infinite for small currents and they are accurate so long as V_{IN} is much greater than V_{OS} and I_O is much greater than I_{bias}.

The source and sink illustrated in Figures 17 and 18 use an FET to drive a bipolar output transistor. It is possible to use a Darlington connection in place of the FET-bipolar combination in cases where the output current is high and the base current of the Darlington input would not cause a significant error.

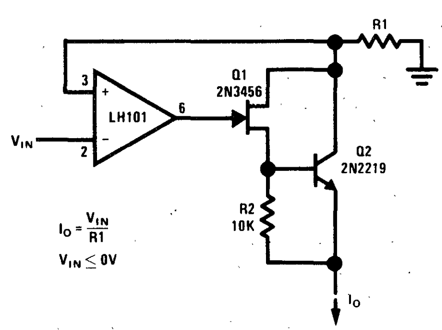


FIGURE 18. Precision Current Source

The amplifiers used must be compensated for unity-gain and additional compensation may be required depending on load reactance and external transistor parameters.

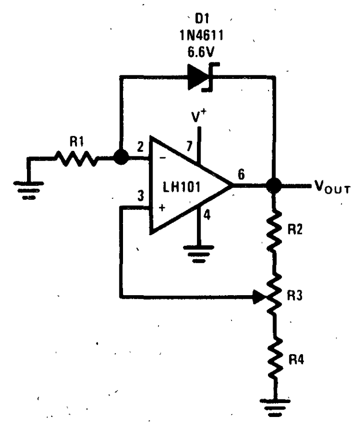


FIGURE 19a. Positive Voltage Reference

ADJUSTABLE VOLTAGE REFERENCES

Adjustable voltage reference circuits are shown in Figures 19 and 20. The two circuits shown have different areas of applicability. The basic difference between the two is that Figure 19 illustrates a voltage source which provides a voltage greater than the reference diode while Figure 20 illustrates a voltage source which provides a voltage lower than the reference diode. The figures show both positive and negative voltage sources.

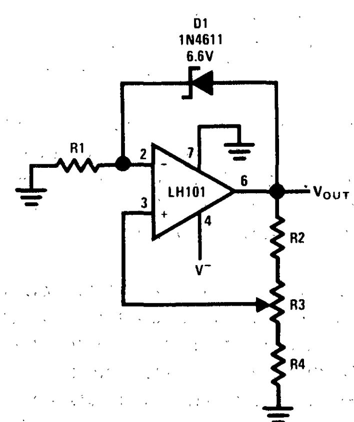


FIGURE 19b. Negative Voltage Reference

High precision extended temperature applications of the circuit of Figure 19 require that the range of adjustment of V_{OUT} be restricted. When this is done, R1 may be chosen to provide optimum zener current for minimum zener T.C. Since I_Z is not a function of V^+, reference T.C. will be independent of V^+.

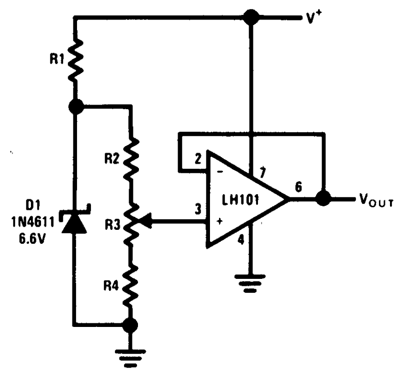


FIGURE 20a. Positive Voltage Reference

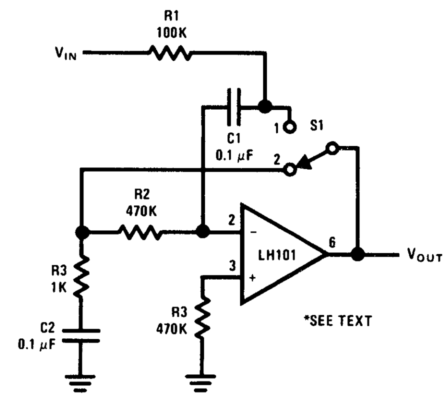


FIGURE 21. Reset Stabilized Amplifier

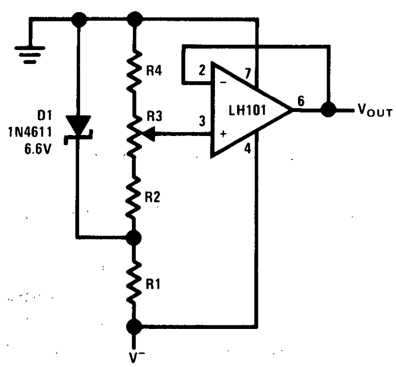


FIGURE 20b. Negative Voltage Reference

The circuit of Figure 20 is suited for high precision extended temperature service if V^+ is reasonably constant since I_Z is dependent on V^+. R1, R2, R3, and R4 are chosen to provide the proper I_Z for minimum T.C. and to minimize errors due to I_{bias}.

The circuits shown should both be compensated for unity-gain operation or, if large capacitive loads are expected, should be overcompensated. Output noise may be reduced in both circuits by bypassing the amplifier input.

The circuits shown employ a single power supply, this requires that common mode range be considered in choosing an amplifier for these applications. If the common mode range requirements are in excess of the capability of the amplifier, two power supplies may be used. The LH101 may be used with a single power supply since the common mode range is from V^+ to within approximately 2 volts of V^-.

THE RESET STABILIZED AMPLIFIER

The reset stabilized amplifier is a form of chopper-stabilized amplifier and is shown in Figure 21. As shown, the amplifier is operated closed-loop with a gain of one.

The connection is useful in eliminating errors due to offset voltage and bias current. The output of this circuit is a pulse whose amplitude is equal to V_{IN}. Operation may be understood by considering the two conditions corresponding to the position of S_1. When S_1 is in position 2, the amplifier is connected in the unity gain connection and the voltage at the output will be equal to the sum of the input offset voltage and the drop across R2 due to input bias current. The voltage at the inverting input will be equal to input offset voltage. Capacitor C1 will charge to the sum of input offset voltage and V_{IN} through R1. When C1 is charged, no current flows through the source resistance and R1 so there is no error due to input resistance. S_1 is then changed to position 1. The voltage stored on C1 is inserted between the output and inverting input of the amplifier and the output of the amplifier changes by V_{IN} to maintain the amplifier input at the input offset voltage. The output then changes from $(V_{OS} + I_{bias}R2)$ to $V_{IN} + I_{bias}R2)$ as S_1 is changed from position 2 to position 1. Amplifier bias current is supplied through R2 from the output of the amplifier or from C2 when S_1 is in position 2 and position 1 respectively. R3 serves tc reduce the offset at the amplifier output if the amplifier must have maximum linear range or if it is desired to DC couple the amplifier.

An additional advantage of this connection is that input resistance approaches infinity as the capacitor C1 approaches full charge, eliminating errors due to loading of the source resistance. The time spent in position 2 should be long with respect to the changing time of C1 for maximum accuracy.

The amplifier used must be compensated for unity gain operation and it may be necessary to overcompensate because of the phase shift across R2 due to C1 and the amplifier input capacity. Since this connection is usually used at very low switching speeds, slew rate is not normally a practical consideration and overcompensation does not reduce accuracy.

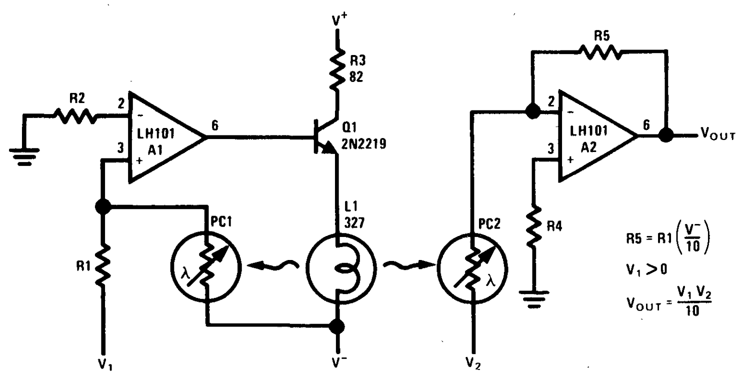


FIGURE 22. Analog Multiplier

THE ANALOG MULTIPLIER

A simple embodiment of the analog multiplier is shown in Figure 22. This circuit circumvents many of the problems associated with the log-antilog circuit and provides three quadrant analog multiplication which is relatively temperature insensitive and which is not subject to the bias current errors which plague most multipliers.

Circuit operation may be understood by considering A2 as a controlled gain amplifier, amplifying V_2, whose gain is dependent on the ratio of the resistance of PC2 to R5 and by considering A1 as a control amplifier which establishes the resistance of PC2 as a function of V_1. In this way it is seen that V_{OUT} is a function of both V_1 and V_2.

A1, the control amplifier, provides drive for the lamp, L1, When an input voltage, V_1, is present, L1 is driven by A1 until the current to the summing junction from the negative supply through PC1 is equal to the current to the summing junction from V_1 through R1. Since the negative supply voltage is fixed, this forces the resistance of PC1 to a value proportional to R1 and to the ratio of V_1 to V^-. L1 also illuminated PC2 and, if the photoconductors are matched, causes PC2 to have a resistance equal to PC1.

A2, the controlled gain amplifier, acts as an inverting amplifier whose gain is equal to the ratio of the resistance of PC2 to R5. If R5 is chosen equal to the product of R1 and V^-, then V_{OUT} becomes simply the product of V_1 and V_2. R5 may be scaled in powers of ten to provide any required output scale factor.

PC1 and PC2 should be matched for best tracking over temperature since the T.C. of resistance is related to resistance match for cells of the same geometry. Small mismatches may be compensated by varying the value of R5 as a scale factor adjustment. The photoconductive cells should receive equal illumination from L1, a convenient method is to mount the cells in holes in an aluminum block and to mount the lamp midway between them. This mounting method provides controlled spacing and also provides a thermal bridge between the two cells to reduce differences in cell temperature. This technique may be extended to the use of FET's or other devices to meet special resistance or environment requirements.

The circuit as shown gives an inverting output whose magnitude is equal to one-tenth the product of the two analog inputs. Input V_1 is restricted to positive values, but V_2 may assume both positive and negative values. This circuit is restricted to low frequency operation by the lamp time constant.

R2 and R4 are chosen to minimize errors due to input offset current as outlined in the section describing the photocell amplifier. R3 is included to reduce in-rush current when first turning on the lamp, L1.

THE FULL-WAVE RECTIFIER AND AVERAGING FILTER

The circuit shown in Figure 23 is the heart of an average reading, rms calibrated AC voltmeter. As shown, it is a rectifier and averaging filter. Deletion of C2 removes the averaging function and provides a precision full-wave rectifier, and deletion of C1 provides an absolute value generator.

Circuit operation may be understood by following the signal path for negative and then for positive inputs. For negative signals, the output of amplifier A1 is clamped to +0.7V by D1 and disconnected from the summing point of A2 by D2. A2 then functions as a simple unity-gain inverter with input resistor, R1, and feedback resistor, R2, giving a positive going output.

For positive inputs, A1 operates as a normal amplifier connected to the A2 summing point through resistor, R5. Amplifier A1 then acts as a simple unity-gain inverter with input resistor, R3, and

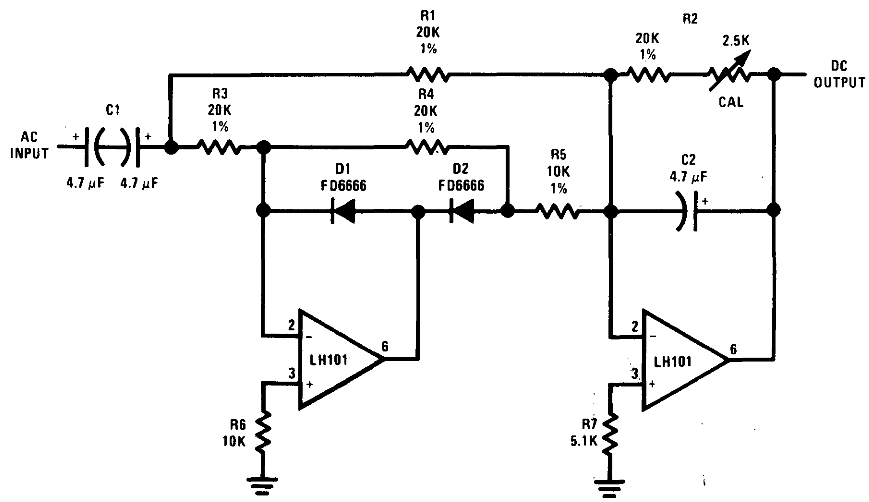


FIGURE 23. Full-Wave Rectifier and Averaging Filter

feedback resistor, R5. A1 gain accuracy is not affected by D2 since it is inside the feedback loop. Positive current enters the A2 summing point through resistor, R1, and negative current is drawn from the A2 summing point through resistor, R5. Since the voltages across R1 and R5 are equal and opposite, and R5 is one-half the value of R1, the net input current at the A2 summing point is equal to and opposite from the current through R1 and amplifier A2 operates as a summing inverter with unity gain, again giving a positive output.

The circuit becomes an averaging filter when C2 is connected across R2. Operation of A2 then is similar to the Simple Low Pass Filter previously described. The time constant R2C2 should be chosen to be much larger than the maximum period of the input voltage which is to be averaged.

Capacitor C1 may be deleted if the circuit is to be used as an absolute value generator. When this is done, the circuit output will be the positive absolute value of the input voltage.

The amplifiers chosen must be compensated for unity-gain operation and R6 and R7 must be chosen to minimize output errors due to input offset current.

SINE WAVE OSCILLATOR

An amplitude-stabilized sine-wave oscillator is shown in Figure 24. This circuit provides high purity sine-wave output down to low frequencies with minimum circuit complexity. An important advantage of this circuit is that the traditional tungsten filament lamp amplitude regulator is eliminated along with its time constant and linearity problems.

In addition, the reliability problems associated with a lamp are eliminated.

The Wien Bridge oscillator is widely used and takes advantage of the fact that the phase of the voltage across the parallel branch of a series and a parallel RC network connected in series, is the same as the phase of the applied voltage across the two networks at one particular frequency and that the phase lags with increasing frequency and leads with decreasing frequency. When this network—the Wien Bridge—is used as a positive feedback element around an amplifier, oscillation occurs at the frequency at which the phase shift is zero. Additional negative feedback is provided to set loop gain to unity at the oscillation frequency. To stabilize the frequency of oscillation, and to reduce harmonic distortion.

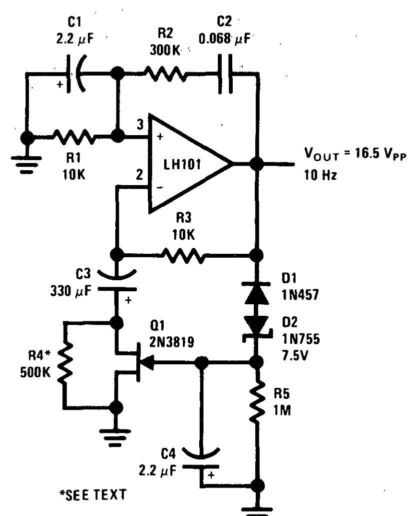


FIGURE 24. Wien Bridge Sine Wave Oscillator

The circuit presented here differs from the classic usage only in the form of the negative feedback stabilization scheme. Circuit operation is as follows: negative peaks in excess of −8.25V cause D1 and D2 to conduct, charging C4. The charge stored in C4 provides bias to Q1, which determines amplifier gain. C3 is a low frequency roll-off capacitor in the feedback network and prevents offset voltage and offset current errors from being multiplied by amplifier gain.

Distortion is determined by amplifier open-loop gain and by the response time of the negative feedback loop filter, R5 and C4. A trade-off is necessary in determining amplitude stabilization time constant and oscillator distortion. R4 is chosen to adjust the negative feedback loop so that the FET is operated at a small negative gate bias. The circuit shown provides optimum values for a general-purpose oscillator.

TRIANGLE-WAVE GENERATOR

A constant amplitude triangular-wave generator is shown in Figure 25. This circuit provides a variable frequency triangular wave whose amplitude is independent of frequency.

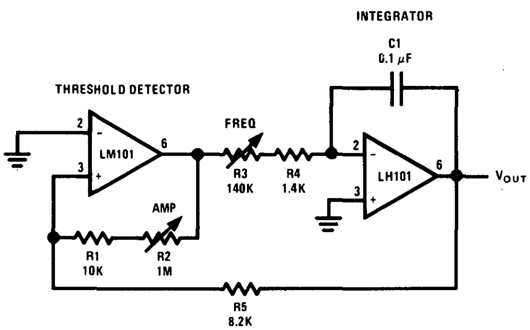


FIGURE 25. Triangular-Wave Generator

The generator embodies an integrator as a ramp generator and a threshold detector with hysterisis as a reset circuit. The integrator has been described in a previous section and requires no further explanation. The threshold detector is similar to a SchmittTrigger in that it is a latch circuit with a large dead zone. This function is implemented by using positive feedback around an operational amplifier. When the amplifier output is in either the positive or negative saturated state, the positive feedback network provides a voltage at the non-inverting input which is determined by the attenuation of the feed-back loop and the saturation voltage of the amplifier. To cause the amplifier to change states, the voltage at the input of the amplifier must be caused to change polarity by an amount in excess of the amplifier input offset voltage. When this is done the amplifier saturates in the opposite direction and remains in that state until the voltage at its input again reverses. The complete circuit operation may be understood by examining the operation with the output of the threshold detector in the positive state. The detector positive saturation voltage is applied to the integrator summing junction through the combination R3 and R4 causing a current I^+ to flow.

The integrator then generates a negative-going ramp with a rate of $I^+/C1$ volts per second until its output equals the negative trip point of the threshold detector. The threshold detector then changes to the negative output state and supplies a negative current, I^-, at the integrator summing point. The integrator now generates a positive-going ramp with a rate of $I^-/C1$ volts per second until its output equals the positive trip point of the threshold detector where the detector again changes output state and the cycle repeats.

Triangular-wave frequency is determined by R3, R4 and C1 and the positive and negative saturation voltages of the amplifier A1. Amplitude is determined by the ratio of R5 to the combination of R1 and R2 and the threshold detector saturation voltages. Positive and negative ramp rates are equal and positive and negative peaks are equal if the detector has equal positive and negative saturation voltages. The output waveform may be offset with respect to ground if the inverting input of the threshold detector, A1, is offset with respect to ground.

The generator may be made independent of temperature and supply voltage if the detector is clamped with matched zener diodes as shown in Figure 26.

The integrator should be compensated for unity-gain and the detector may be compensated if power supply impedance causes oscillation during its transition time. The current into the integrator should be large with respect to I_{bias} for maximum symmetry, and offset voltage should be small with respect to V_{OUT} peak.

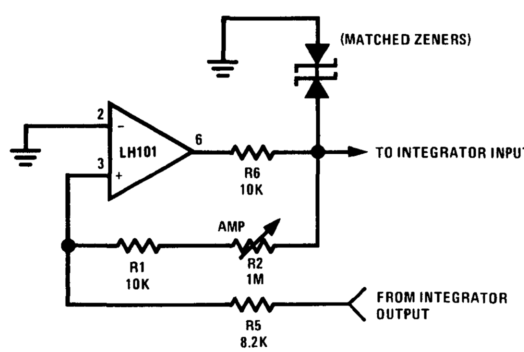


FIGURE 26. Threshold Detector with Regulated Output

TRACKING REGULATED POWER SUPPLY

A tracking regulated power supply is shown in Figure 27. This supply is very suitable for powering an operational amplifier system since positive and negative voltages track, eliminating common mode signals originating in the supply voltage. In addition, only one voltage reference and a minimum number of passive components are required.

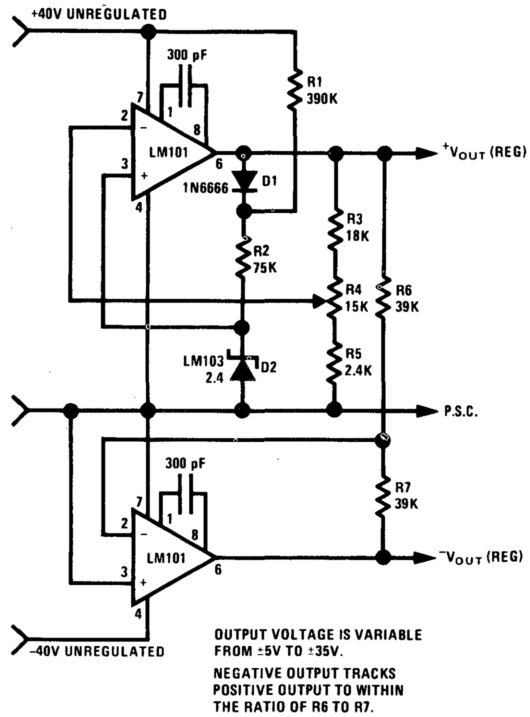


FIGURE 27. Tracking Power Supply

Power supply operation may be understood by considering first the positive regulator. The positive regulator compares the voltage at the wiper of R4 to the voltage reference, D2. The difference between these two voltages is the input voltage for the amplifier and since R3, R4, and R5 form a negative feedback loop, the amplifier output voltage changes in such a way as to minimize this difference. The voltage reference current is supplied from the amplifier output to increase power supply line regulation. This allows the regulator to operate from supplies with large ripple voltages. Regulating the reference current in this way requires a separate source of current for supply start-up. Resistor R1 and diode D1 provide this start-up current. D1 decouples the reference string from the amplifier output during start-up and R1 supplies the start-up current from the unregulated positive supply. After start-up, the low amplifier output impedance reduces reference current variations due to the current through R1.

The negative regulator is simply a unity-gain inverter with input resistor, R6, and feedback resistor, R7.

The amplifiers must be compensated for unity-gain operation.

The power supply may be modulated by injecting current into the wiper of R4. In this case, the output voltage variations will be equal and opposite at the positive and negative outputs. The power supply voltage may be controlled by replacing D1, D2, R1 and R2 with a variable voltage reference.

PROGRAMMABLE BENCH POWER SUPPLY

The complete power supply shown in Figure 28 is a programmable positive and negative power supply. The regulator section of the supply comprises two voltage followers whose input is provided by the voltage drop across a reference resistor of a precision current source.

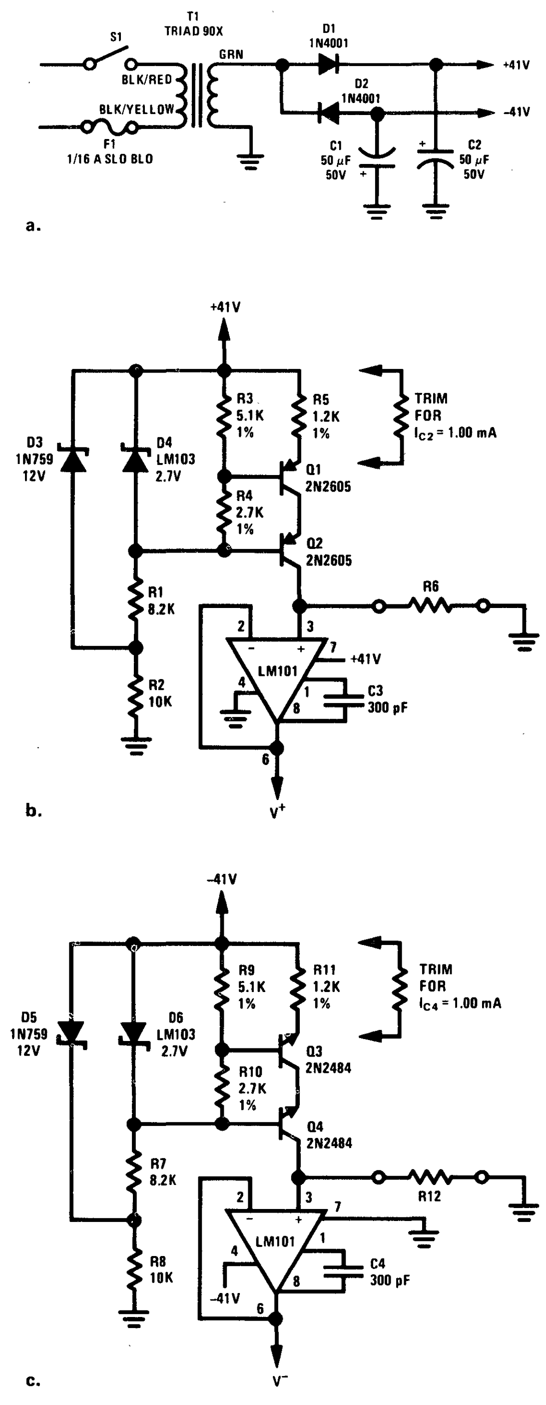


FIGURE 28. Low-Power Supply for Integrated Circuit Testing

Programming sensitivity of the positive and negative supply is 1V/1000Ω of resistors R6 and R12 respectively. The output voltage of the positive regulator may be varied from approximately +2V to +38V with respect to ground and the negative regulator output voltage may be varied from −38V to 0V with respect to ground. Since LH101 amplifiers are used, the supplies are inherently short circuit proof. This current limiting feature also serves to protect a test circuit if this supply is used in integrated circuit testing.

Internally compensated amplifiers may be used in this application if the expected capacitive loading is small. If large capacitive loads are expected, an externally compensated amplifier should be used and the amplifier should be overcompensated for additional stability. Power supply noise may be reduced by bypassing the amplifier inputs to ground with capacitors in the 0.1 to 1.0 μF range.

CONCLUSIONS

The foregoing circuits are illustrative of the versatility of the integrated operational amplifier and provide a guide to a number of useful applications. The cautions noted in each section will show the more common pitfalls encountered in amplifier usage.

APPENDIX I
DEFINITION OF TERMS

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Bias Current: The average of the two input currents.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Common Mode Rejection Ratio: The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other gounded.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltage producing it.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

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December 1968

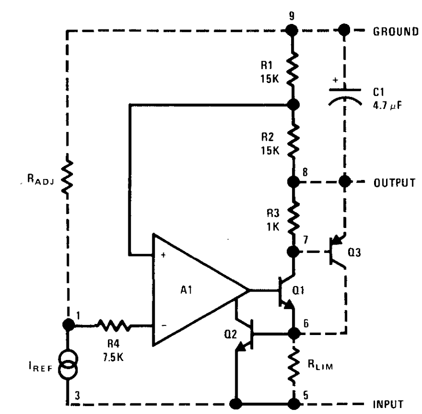
DESIGNS FOR NEGATIVE VOLTAGE REGULATORS

INTRODUCTION

A number of IC voltage regulators have been introduced to date, but these have been designed primarily to regulate positive voltages. Most can be adapted as negative regulators, at some sacrifice in complexity, performance and flexibility. This note, however, describes an IC, which is designed specifically as a negative regulator. It is intended to complement the LM100 and LM105 positive regulators, providing a line of IC's for practically every regulator application.

Unique features of the circuit are that it supplies any output voltage from 0V down to −40V, while operating from a single unregulated supply. The output voltage is proportional to a single programming resistor, and remote sensing can be done at the load. It also regulates within 0.01% in circuits using a separate, floating bias supply, where the maximum output voltage is limited only by the breakdown of external pass transistors. The device is designed for either linear or switching regulator applications.

In the circuits described, emphasis is placed on practical considerations for the design of reliable regulators. Many of the pitfalls which cause unexpected failures are explained, and protection schemes for many of the hazards facing regulators are given. Most of the design hints are sufficiently general to apply equally to other IC's or even regulators designed entirely with discrete components.



A functional diagram of the LM104 regulator and external circuitry (dash line) is shown in the figure. The internal reference is a temperature compensated current source, I_{ref}. A voltage which is proportional to an external programming resistor, R_{adj}, is fed into an error amplifier, A1. This drives an internal series pass transistor, Q1, to supply an output voltage equal to twice the voltage across the programming resistor. External pass transistors can be added, as is Q3, to increase the output-current capability. Short-circuit protection makes the circuit exhibit a constant-current characteristic when Q2 is turned on by the voltage drop across an external current-limit resistor, R_{lim}. A more complete description of the integrated circuit itself is given in the back of the text.

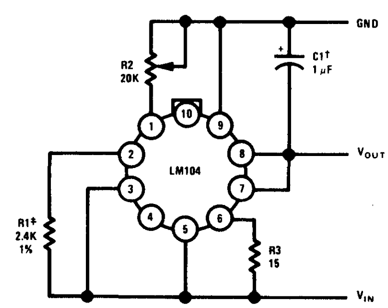
LOW POWER REGULATOR OR BIAS SUPPLY

This circuit can provide output voltages between 0V and −40V at currents up to 25 mA. The output voltage is linearly dependent on the value of R2, giving approximately 2V for each 1 KΩ of resistance. The exact scale factor can be set up by trimming R1. This should be done at the maximum output voltage setting in order to compensate for any mismatch in the internal divider resistors of the integrated circuit.

Short-circuit protection is provided by R3. The value of this resistor should be chosen so that the voltage drop across it is 300 mV at the maximum load current. This insures worst-case operation up to full load over a −55°C to 125°C temperature range. With a lower maximum operating temperature, the design value for this voltage can be increased linearly to 525 mV at 25°C.

For an output voltage setting of 15V, the regulation, no load to full load, is better than 0.05%; and the line regulation is better than 0.2% for a ±20% input voltage variation. Noise and ripple can be greatly reduced by bypassing R2 with a 10 μF capacitor. This will keep the ripple on the output less than 0.5 mV for a 1V, 120 Hz ripple on the unregulated input. The capacitor also improves the line-transient response by a factor of five.

An output capacitor of at least 1 μF is required to keep the regulator from oscillating. This should be a low inductance capacitor, preferably solid tantalum, installed with short leads. It is not usually necessary to bypass the input, but at least a 0.01 μF bypass is advisable when there are long leads connecting the circuit to the unregulated power source.

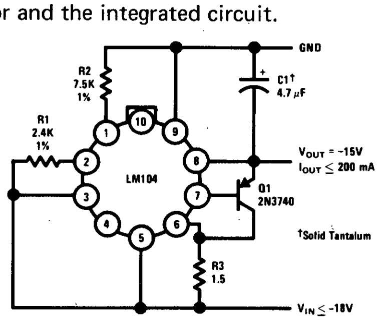


†Solid Tantalum
‡Trim R1 for exact scale factor

It is important to watch power dissipation in the integrated circuit even with load currents of 25 mA or less. The dissipation can be in excess of 1W with large input-output voltage differentials, and this is above ratings for the device.

INCREASED OUTPUT CURRENT

When output currents above 25 mA are required or when the dissipation in the series pass transistor can be higher than about 0.2W, under worst-case conditions, it is advisable to add an external transistor to the LM104 to handle the power. The connection of an external booster transistor is shown here. The output current capability of the regulator is increased by the current gain of the added PNP transistor, but it is still necessary to watch dissipation in the external pass transistor. Excessive dissipation can burn out both the series pass transistor and the integrated circuit.



For example, with the circuit shown, the worst-case input voltage can be 25V. With a shorted output at 125°C, the current through the pass transistor will be 300 mA; and the dissipation in it will be 7.5W. This clearly establishes the need for an efficient heat sink.

For lower-power operation, a 2N2905 with a clip on heat sink can be used for the external pass transistor. However, when the worst case dissipation is above 0.5W, it is advisable to employ a power device such as the 2N3740 with a good heat sink.

The current limit resistor is chosen so that the voltage drop across it is 300 mV, with maximum load current, for operation to 125°C. With lower maximum ambients this voltage drop could be increased by 2.2 mV/°C. If possible, a fast-acting fuse rated about 25% higher than the maximum load current should be included in series with the unregulated input.

When a booster transistor is used, the minimum input-output voltage differential of the regulator will be increased by the emitter-base voltage of the added transistor. This establishes the minimum differential at 2 to 3V, depending on the base drive required by the external transistor.

HIGH CURRENT REGULATOR

When output currents in the ampere range are needed, it is necessary to add a second booster transistor to the LM104 circuitry. This connection is shown in the accompanying figure. The output current capability of the LM104 is increased by the product of the current gains of Q1 and Q2. However, it is still necessary to watch the dissipation in both the series pass transistor, Q2, and its driver, Q1. A clip-on heat sink is definitely required for Q1, and it is advisable to replace the 2N2905 with a 2N3740 which has a good heat sink when output currents greater than 1A are needed. A 1000 pF capacitor should also be added between Pins 4 and 5 to compensate for the poorer frequency response of the 2N3740. The need for an efficient heat sink on Q2 should be obvious.

Experience shows that a single-diffused transistor such as a 2N3055 (or a 2N3772 for higher currents) is preferred over a double diffused, high-frequency transistor for the series pass element. The slower, single-diffused devices are less prone to secondary breakdown and oscillations in linear regulator applications.

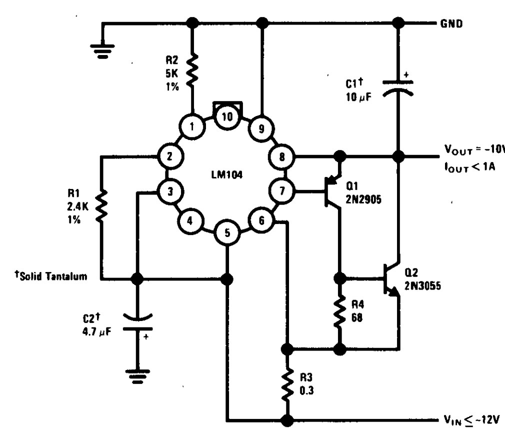
As with the lower-current regulators, C1 is required to frequency compensate the regulator and prevent oscillations. It is also advisable to bypass the input with C2 if the regulator is located any distance from the output filter of the unregulated supply. The resistor across the emitter base junction of Q2 fixes the minimum collector current of Q1 to minimize oscillation problems with light loads. It is still possible to experience oscillations with certain physical layouts, but these can almost always be eliminated by stringing a ferrite bead, such as a Ferroxcube K5-001-00/3B, on the emitter lead of Q2.

The use of two booster transistors does not appreciably increase the minimum input-output voltage differential over that for a single transistor. The minimum differential will be 2 to 3V, depending on the drive current required from the integrated circuit.

With high current regulators, remote sensing is sometimes required to eliminate the effect of line resistance between the regulator and the load. This can be accomplished by returning R2 and Pin 9 of the LM104 to the ground end of the load and connecting Pin 8 directly to the high end of the load.

The low resistance values required for the current limit resistor, R3, are sometimes not readily available. A suitable resistor can be made using a piece of resistance wire or even a short length of kovar lead wire from a standard TO-5 transistor.

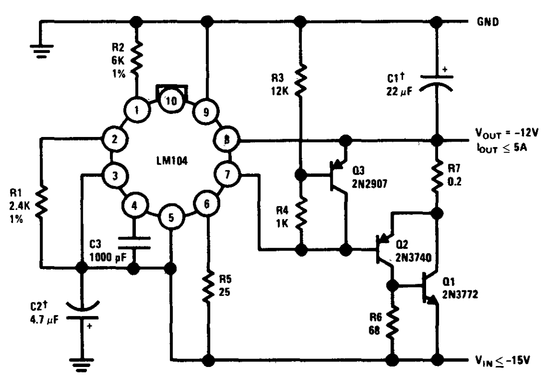
The current limit sense voltage can be reduced to about 400 mV by inserting a germanium diode (or a diode-connected germanium transistor) in series with Pin 6 of the LM104. This diode will also compensate the sense voltage and make the short circuit current essentially independent of temperature.



With high current regulators it is especially important to use a low-inductance capacitor on the output. The lead length on this capacitor must also be made short. Otherwise, the capacitor leads can resonate with smaller bypass capacitors (like 0.1 µF ceramic) which may be connected to the output. These resonances can lead to oscillations. With short leads on the output capacitor, the Q of the tuned circuit can be made low enough so that it cannot cause trouble.

FOLDBACK CURRENT LIMITING

High current regulators dissipate a considerable amount of power in the series pass transistor under full-load conditions. When the output is shorted, this dissipation can easily increase by a factor of four. Hence, with normal current limiting, the heat sink must be designed to handle much more power than the worst case full load dissipation if the circuit is to survive short-circuit conditions. This can increase the bulk of the regulator substantially.



†Solid Tantalum

This situation can be eased considerably by using foldback current limiting. With this method of current limiting, the available output current actually decreases as the maximum load on the regulator is exceeded and the output voltage falls off. The short-circuit current can be adjusted to be a fraction of the full load current, minimizing dissipation in the pass transistor.

The circuit shown here accomplishes just this. Normally Q3 is held in a non-conducting state by the voltage developed across R4. However, when the voltage across the current limit resistor, R7, increases to where it equals the voltage across R4 (about 1V), Q3 turns on and begins to rob base drive from the driver transistor, Q1. This causes an increase in the output current of the LM104, and it will go into current limiting at a current determined by R5. Since the base drive to Q1 is clamped, the output voltage will drop with heavier loads. This reduces the voltage drop across R4 and, therefore, the available output current. With the output completely shorted, the current will be about one-fifth the full-load current.

In design, R7 is chosen so that the voltage drop across it will be 1 to 2V under full load conditions. The resistance of R3 should be one-thousand times the output voltage. R4 is then determined from

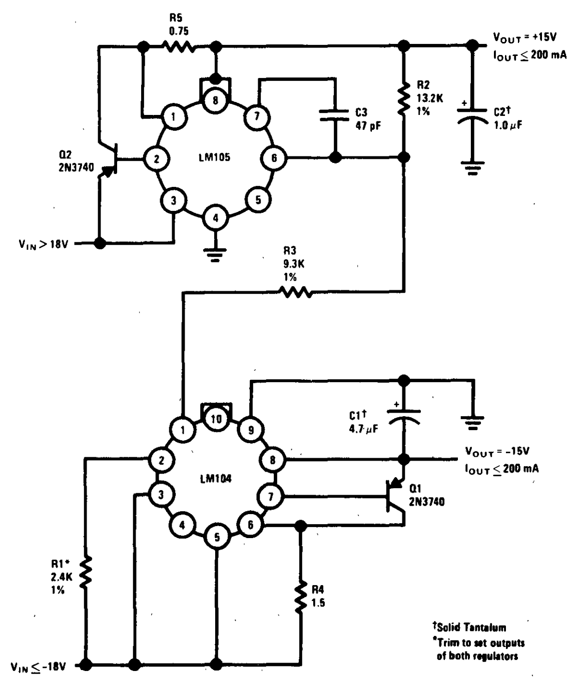
$$R_4 \cong \frac{R_7 R_3 I_{FL}}{V_{OUT} + 0.5}$$

where I_{FL} is the load current at which limiting will occur.

If it is desired to reduce the ratio of full load to short circuit current, this can be done by connecting a resistance of 2 to 10 KΩ across the emitter-base of Q3.

SYMMETRICAL POWER SUPPLIES

In many applications, such as powering operational amplifiers, there is a need for symmetrical positive and negative supply voltages. A circuit which is a particularly-economical solution to this design problem is shown in the adjoining figure. It uses a minimum number of components, and the voltage at both outputs can be set up within ±1.5% by a single adjustment. Further, the output voltages will tend to track with temperature and variations on the unregulated supply.

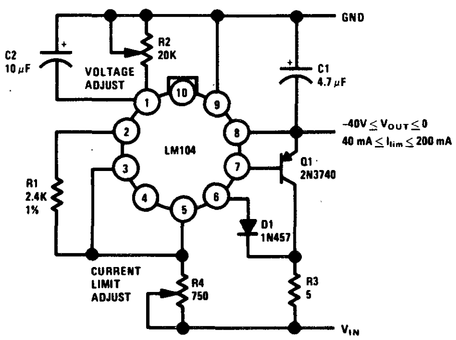


The positive voltage is regulated by an LM105, while an LM104 regulates the negative supply. The unusual feature is that the two regulators are interconnected by R3. This not only eliminates one precision resistor, but the reference current of the LM104 stabilizes the LM105 so that a ±10% variation in its reference voltage is only seen as a ±3% change in output voltage. This means that in many cases the output voltage of both regulators can be set up with sufficient accuracy by trimming a single resistor, R1.

The line regulation and temperature drift of the circuit is determined primarily by the LM104, so both output voltages will tend to track. Output ripple can be reduced by about a factor of five to less than 2 mV/V by bypassing Pin 1 of the LM104 to ground with a 10 µF capacitor. A center-tapped transformer with a bridge rectifier can be used for the unregulated power source.

ADJUSTABLE CURRENT LIMITING

In laboratory power supplies, it is often necessary to adjust the limiting current of a regulator. This, of course, can be done by using a variable resistance for the current limit resistor. However, the current-limit resistor can easily have a value below that of commercially-available potentiometers. Discrete resistance values can be switched to vary the limiting current, but this does not provide continuously-variable adjustment.



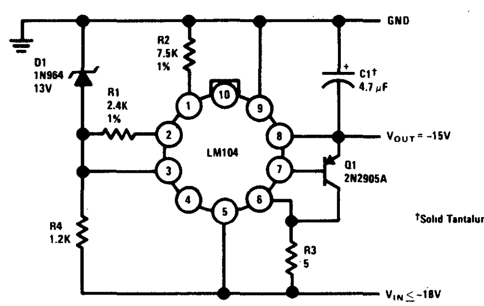
The circuit shown here solves this problem, giving a linear adjustment of limiting current over a five-to-one range. A silicon diode, D1, is included to reduce the current limit sense voltage to approximately 50 mV. Approximately 1.3 mA from the reference supply is passed through a potentiometer, R4, to buck out the diode voltage. Therefore, the effective current limit sense voltage is nearly proportional to the resistance of R4. The current through R4 is fairly insensitive to changes in ambient temperature, and D1 compensates for temperature variations in the current limit sense voltage of the LM104. Therefore, the limiting current will not be greatly affected by temperature.

It is important that a potentiometer be used for R4 and connected as shown. If a rheostat connection were used, it could open while it was being adjusted and momentarily increase the current limit sense voltage to many times its normal value. This could destroy the series pass transistors under short-circuit conditions.

The inclusion of R4 will soften the current limiting characteristics of the LM104 somewhat because it acts as an emitter-degeneration resistor for the current-limit transistor. This can be avoided by reducing the value of R4 and developing the voltage across R4 with additional bleed current to ground.

IMPROVING LINE REGULATION

The line regulation for voltage variations on the reference supply terminal of the LM104 is about five times worse than it is for changes on the unregulated input. Therefore, a zener-diode pre-regulator can be used on the reference supply to improve line regulation. This is shown in the figure.



The design of this circuit is fairly simple. It is only necessary that the minimum current through R4 be greater than 2 mA with low input voltage. Further, the zener voltage of D1 must be five volts greater than one-half the maximum output voltage to keep the transistors in the reference current source from saturating.

USING PROTECTIVE DIODES

It is a little known fact that most voltage regulators can be damaged by shorting out the unregulated input voltage while the circuit is operating—even though the output may have short-circuit protection. When the input voltage to the regulator falls instantaneously to zero, the output capacitor is still charged to the nominal output voltage. This applies voltage of the wrong polarity across the series pass transistor and other parts of the regulator, and they try to discharge the output capacitor into the short. The resulting current surge can damage or destroy these parts.

When the LM104 is used as the control element of the regulator, the discharge path is through internal junctions forward biased by the voltage reversal. If the charge on the output capacitor is in the order of 40 volt • μF, the circuit can be damaged during the discharge interval. However, the problem is not only seen with integrated circuit regulators. It also happens with discrete regulators where the series-pass transistor usually gets blown out.

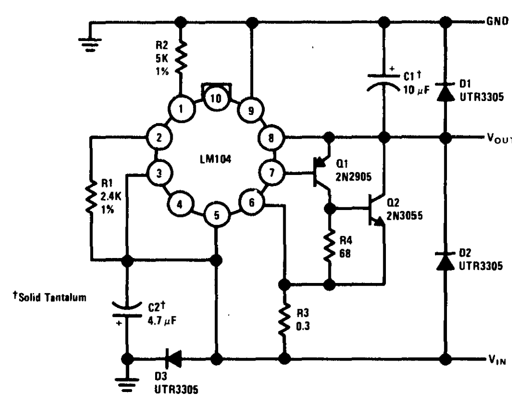
The problem can be eliminated by connecting a diode between the output and the input such that it discharges the output capacitor when the input is shorted. The diode should be capable of handling large current surges without excessive voltage drop, but it does not have to be a power diode since it does not carry current continuously. It should also be relatively fast. Ordinary rectifier diodes will not do because they look like an open circuit in the forward direction until minority carriers are injected into the intrinsic base region of the PIN structure.

This problem is not just caused by accidental physical shorts on the input. It has shown up more than once when regulators are driven from high-frequency dc-dc converters. Tantalum capacitors are frequently used as output filters for the rectifiers. When these capacitors are operated near their maximum voltage ratings with excessive high frequency ripple across them, they have a tendency to sputter—that is, short momentarily and clear themselves. When they short, they can blow out the regulator; but they look innocent after the smoke has cleared.

The solution to this problem is to use capacitors with conservative voltage ratings, to observe the maximum ripple ratings for the capacitor and to include a protective diode between the input and output of the regulator to protect it in case sputtering does occur.

Heavy loads operating from the unregulated supply can also destroy a voltage regulator. When the input power is switched off, the input voltage can drop faster than the output voltage, causing a voltage reversal across the regulator, especially when the output of the regulator is lightly loaded. Inductive loads such as a solenoid are particularly troublesome in this respect. In addition to causing a voltage reversal between the input and the output, they can reverse the input voltage causing additional damage.

In cases like this, it is advisable to use a multiple-pole switch or relay to disconnect the regulator from the unregulated supply separate from the other loads. If this cannot be done, it is necessary to put a diode across the input of the regulator to clamp any reverse voltages, in addition to the protective diode between the input and the output.

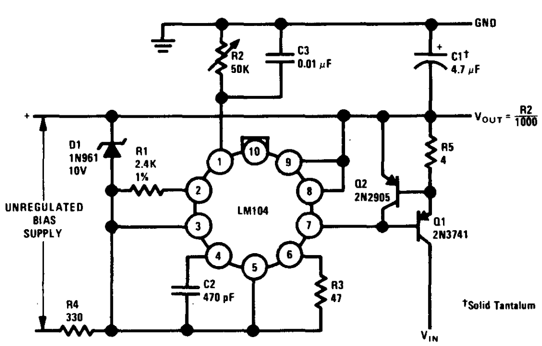


Yet another failure mode can occur if the regulated supply drives inductive loads. When power is shut off, the inductive current can reverse the output voltage polarity, damaging the regulator and the output capacitor. This can be cured with a clamp diode on the output. Even without inductive loads it is usually good practice to include this clamp diode to protect the regulator if its output is accidentally shorted to a negative supply.

A regulator with all these protective diodes is shown here. D1 protects against output voltage reversal. D2 prevents a voltage reversal between the input and the output of the regulator. And D3 prevents a reversal of the input-voltage polarity. In many cases, D3 is not needed if D1 and D2 are used, since these diodes will clamp the input voltage within two diode drops of ground. This is adequate if the input voltage reversals are of short duration.

HIGH VOLTAGE REGULATOR

In the design of commercial power supplies, it is common practice to use a floating bias supply to power the control circuitry of the regulator. As shown here, this connection can be used with the LM104 to regulate output voltages that are higher than the ratings of the integrated circuit. Better regulation can also be obtained because it is a simple matter to preregulate the low current bias supply so that the integrated circuit does not see ripple or line voltage variations and because the reduced operating voltage minimizes power dissipation and associated thermal effects from the current delivered to the booster transistor.



The bias for the LM104, which is normally obtained from a separate winding on the main power transformer, is preregulated by D1. R4 is selected so that it can provide the 3 mA operating current for the integrated circuit as well as the base drive of the booster transistor, Q1, with full load and minimum line voltage. The booster transistor regulates the voltage from the main supply, and its breakdown voltage will determine the maximum operating voltage of the complete regulator.

The connection of the LM104 is somewhat different than usual: the internal divider for the error amplifier is shorted out by connecting Pins 8 and 9 together. This makes the output voltage equal to the voltage drop across the adjustment resistor, R2, instead of twice this voltage as is normally the case. C2 and C3 must also be added to prevent oscillation. The value of C3 can be increased to 4.7 μF to reduce noise on the output.

It is necessary to add Q2 and R5 to provide current limiting. When the output current becomes high enough to turn on Q2, there will be an abrupt rise in the output current of the LM104 as Q2 tries to remove base drive from the booster transistor. Any further increases in load current will cause the LM104 to limit at a current determined by R3, and the output voltage will collapse. The value of R3 must be selected so that the integrated circuit can deliver the base current of Q1, at full load, without limiting.

A second, NPN booster transistor can be used in a compound connection with Q1 to increase the output current of the regulator. However, with very-high-voltage regulators, the most economical solution may be to use a high voltage PNP driving a vacuum tube for the series pass element.

Remote sensing, which eliminates the effects of voltage dropped in the leads connecting the regulator to the load, can be provided by connecting R2 to the ground end of the load and Pins 8 and 9 to the high end of the load.

SWITCHING REGULATOR

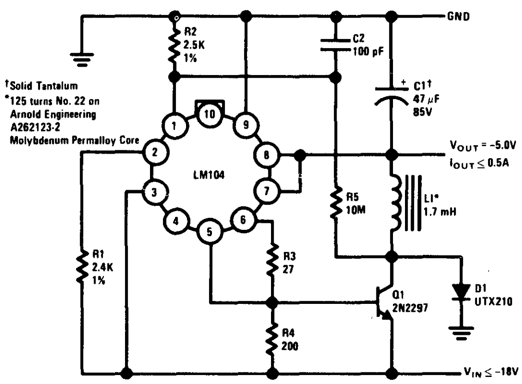
Linear regulators have the advantages of fast response to load transients as well as low noise and ripple. However, since they must dissipate the difference between the unregulated-supply power and the output power, they sometimes have a low efficiency. This is not always a problem with ac line-operated equipment because the power loss is easily afforded, because the input voltage is already fairly-well regulated and because losses can be minimized by adjustment of transformer ratios in the power supply. In systems operating from a fixed dc input voltage, the situation is often much different. It might be necessary to regulate a 28V input voltage down to 5V. In this case, the power loss can quickly become excessive. This is true even if efficiency is not one of the more important criteria, since high power dissipation calls for expensive power transistors and elaborate heat sinking methods.

Switching regulators can be used to greatly reduce dissipation. Efficiencies approaching 90% can be realized even though the regulated output voltage is only a fraction of the input voltage. With proper design, transient response and ripple can also be made quite acceptable.

This circuit, which uses the LM104 as a self-oscillating switching regulator, operates in much the same way as a linear regulator. The reference current is set up at 1 mA with R1, and R2 determines the output voltage in the normal fashion. The circuit is made to oscillate by applying positive feedback through R5 to the non-inverting input on the error amplifier of the LM104. When the output voltage is low, the internal pass transistor of the integrated circuit turns on and drives Q1 into saturation. The current feedback through R5 then increases the magnitude of the reference voltage developed across R2. Q1 will remain on until the output voltage comes up to twice this reference voltage. At this point, the error amplifier goes into linear operation, and the positive feedback makes the circuit switch off. When this happens, the reference voltage is lowered by feedback through R5, and the circuit will stay off until the output voltage drops to where the error amplifier again goes into linear operation. Hence, the circuit regulates with the output voltage oscillating about the nominal value with a peak-to-peak ripple of around 40 mV.

The power conversion from the input voltage to a lower output voltage is obtained by the action of the switch transistor, Q1, the catch diode, D1, and the LC filter. The inductor is made large enough so that the current through it is essentially constant throughout the switching cycle. When Q1 turns on, the voltage on its collector will be nearly equal to the unregulated input voltage. When it turns off, the magnetic field in L1 begins to collapse, driving the collector voltage of Q1 to ground where it is clamped by D1.

If, for example, the input voltage is 10V and the switch transistor is driven at a 50% duty cycle, the average voltage on the collector of Q1 will be 5V. This waveform will be filtered by L1 and C1 and appear as a 5V dc voltage on the output. Since the inductor current comes from the input while Q1 is on but from ground through D1 while Q1 is off, the average value of the input current will be half the output current. The power output will therefore equal the input power if switching losses are neglected.



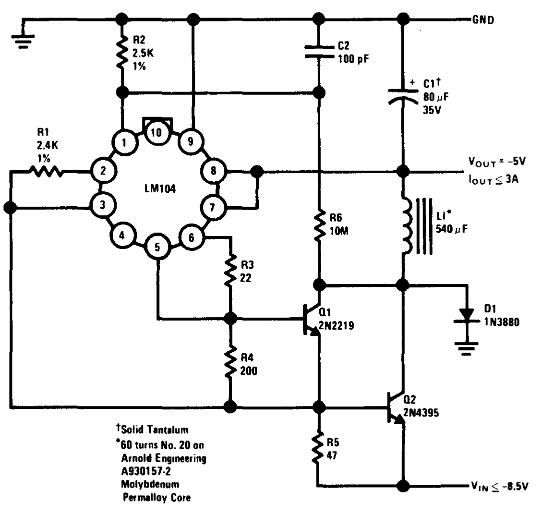
In design, the value of R3 is chosen to provide sufficient base drive to Q1 at the maximum load current. R4 must be low enough so that the bias current coming out of Pin 5 of the LM104 (approximately 300 μA) does not turn on the switch transistor. The purpose of C2 is to remove transients that can appear across R2 and cause erratic switching. It should not be made so large that it severely integrates the waveform fed back to this point.

For additional information on switching regulators see "Designing Switching Regulators," National Semiconductor AN-2, August, 1968.

HIGH CURRENT SWITCHING REGULATOR

Output currents up to 3A can be obtained using the switching regulator circuit shown here. The circuit is identical to the one described previously, except that Q2 has been added to increase the output current capability by about an order of magnitude. It should be noted that the reference supply terminal is returned to the base of Q2, rather than the unregulated input. This is done because the LM104 will not function properly if Pin 5 gets more than 2V more positive than Pin 3. The reference current, as well as the bias currents for Pins 3 and 5, is supplied from the unregulated input through R5, so its resistance must be low enough so that Q2 is not turned on with about 2 mA flowing through it.

The line regulation of this circuit is worsened somewhat by the unregulated input voltage being fed back into the reference for the regulator through R6. This effect can be eliminated by connecting a 0.01 μF capacitor in series with R6 to remove the dc component of the feedback.



There are a number of precautions that should be observed with all switching regulators, although they are more inclined to cause problems in high-current applications:

For one, fast switching diodes and transistors must be used. If D1 is an ordinary junction rectifier, voltages in the order of 10V can be developed across it in the forward direction when the switch transistor turns off. This happens because low-frequency rectifiers are usually manufactured with a PIN structure which presents a high forward impedance until enough minority carriers are injected into the diode base region to increase its conductance. This not only causes excessive dissipation in the diode, but the diode also presents a short circuit to the switch transistor, when it first turns on, until all the charge stored in the base region of the diode is removed. Similarly, a high frequency switch transistor must be used as excessive switching losses in low frequency transistors, like the 2N3055, make them overheat.

It is important that the core material used for the inductor have a soft saturation characteristic. Cores that saturate abruptly produce excessive peak currents in the switch transistor if the output current becomes high enough to run the core close to saturation. Powdered molybdenum-permalloy cores, on the other hand, exhibit a gradual reduction in permeability with excessive current, so the only effect of output currents above the design value is a gradual increase in switching frequency.

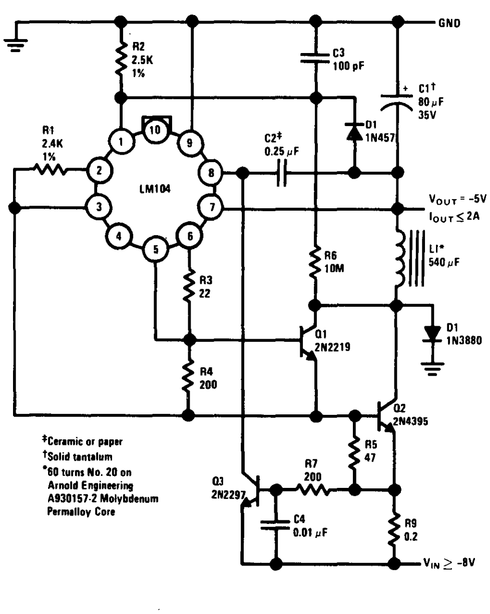
One thing that is frequently overlooked in the design of switching circuits is the ripple rating of the filter capacitors. Excessive high-frequency ripple can cause these capacitors to fail. This is an especially-important consideration for capacitors used on the unregulated input as the ripple current through them can be higher than the dc load current. The situation is eased somewhat for the filter capacitor on the output of the regulator since the ripple current is only a fraction of the load current. Nonetheless, proper design usually requires that the voltage rating of this capacitor be higher than that dictated by the dc voltage across it for reliable operation.

One unusual problem that has been noted in working with switching regulators is excessive dissipation in the switch transistors caused by high emitter-base saturation voltage. This can also show up as erratic operation if Q1 is the defective device. This saturation voltage can be as high as 5V and is the result of poor alloying on the base contact of the transistor. A defective transistor will not usually show up on a curve tracer because the low base current needed for linear operation does not produce a large voltage drop across the poorly-alloyed contact. However, a bad device can be spotted by probing on the bases of the switch transistors while the circuit is operating.

It is necessary that the catch diode, D1, and any bypass capacitance on the unregulated input be returned to ground separately from the other parts of the circuit. These components carry large current transients and can develop appreciable voltage transients across even a short length of wire. If C1, C2, or R2 have any common ground impedance with the catch diode or the input bypass capacitor, the transients can appear directly on the output.

SWITCHING REGULATOR WITH CURRENT LIMITING

The switching regulator circuits described previously are not protected from overloads or a short-circuited output. The current limiting of the LM104 is used to limit the base drive of the switch transistor, but this does not effectively protect the switch transistor from excessive current. Providing short circuit protection is no simple problem, since it is necessary to keep the regulator operating in the switching mode when the output is shorted. Otherwise, the dissipation in the switch transistor will become excessive even though the current is limited.



A circuit which provides current limiting and protects the regulator from short circuits is shown here. The current through the switch transistor produces a voltage drop across R9. When this voltage becomes large enough to turn on Q3, current limiting is initiated. This occurs because Q3 takes over as the control transistor and regulates the voltage on Pin 8 of the LM104. This point, which is the feedback terminal of the error amplifier, is separated from the actual output of the regulator by not shorting the regulated output and booster output terminals of the integrated circuit. Hence, with excessive output current, the circuit still operates as a switching regulator with Q3 regulating the voltage fed back to the error amplifier as the output voltage falls off.

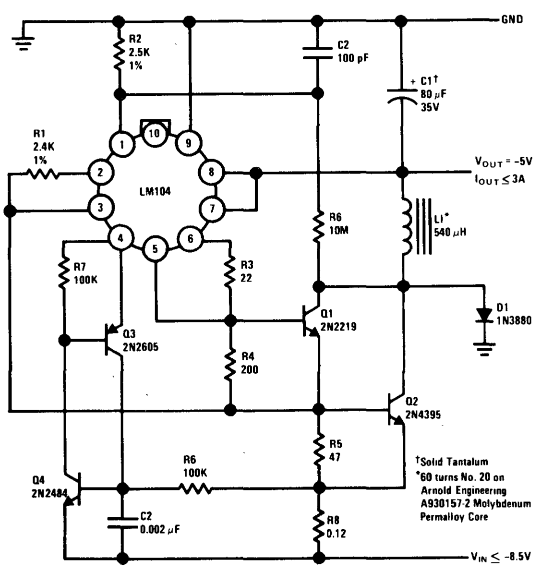
A resistor, R7, is included so that excessive base current will not be driven into the base of Q3. C4 insures that Q3 does not turn on from the current spikes through the switch transistor caused by pulling the stored charge out of the catch diode (these are about twice the load current). This capacitor also operates in conjunction with C2 to produce sufficient phase delay in the feedback loop so that the circuit will oscillate in current limiting. However, C4 should not be made so large that it appreciably integrates the rectangular waveform of the current through the switch transistor.

As the output voltage falls below half the design value, D1 pulls down the reference voltage across R2. This permits the current limiting circuitry to keep operating when the unregulated input voltage drops below the design value of output voltage, with a short on the output of the regulator.

A transistor with good high-current capability was chosen for Q3 so that it does not suffer from secondary breakdown effects from the large peak currents (about 200 mA) through it. With a shorted output, these peak currents occur with the full input voltage across Q3. The average dissipation in Q3 is, however, low.

SWITCHING REGULATOR WITH OVERLOAD SHUTOFF

An alternate method for protecting a switching regulator from excessive output currents is shown here. When the output current becomes too high, the voltage drop across the current-sense resistor, R8, fires an SCR which shuts off the regulator. The regulator remains off, dissipating practically no power, until it is reset by removing the input voltage.

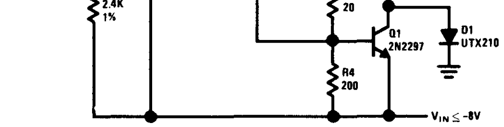


In the actual circuit, complementary transistors, Q3 and Q4, replace the SCR since it is difficult to find devices with a low enough holding current (about 25 μA). When the voltage drop across R8 becomes large enough to turn on Q4, this removes the base drive for the output transistors of the LM104 through Pin 4. When this happens Q3 latches Q4, holding the regulator off until the input voltage is removed. It will then start when power is applied if the overload has been removed.

With this circuit, it is necessary that the shutoff current be 1.5 times the full load current. Otherwise, the circuit will shut off when it is switched on with a full load because of the excess current required to charge the output capacitor. The shutoff current can be made closer to the full load current by connecting a 10 μF capacitor across R2 which will limit the charging current for C1 by slowing the risetime of the output voltage when the circuit is turned on. However, this capacitor will also bypass the positive feedback from R6 which makes the regulator oscillate. Therefore, it is necessary to put a 270Ω resistor in the ground end of the added capacitor and provide feedback to this resistor from the collector of Q1 through a 1 MΩ resistor.

DRIVEN SWITCHING REGULATOR

When a number of switching regulators are operated from a common power source, it is desirable to synchronize their operation to more uniformly distribute the switched current waveforms in the input line. Synchronous operation can also be beneficial when a switching regulator is operated in conjunction with a power converter.



A circuit which synchronizes the switching regulator with a square wave drive signal is shown here. It differs from the switching regulators described previously in that positive feedback is not used. Instead, a triangular wave with a peak-to-peak amplitude of 25 mV is applied to the noninverting input of the error amplifier. The waveform is obtained by integrating the square wave synchronizing signal. This triangular wave causes the error amplifier to switch because its gain is high enough that the waveform easily overdrives it. The switching duty cycle is controlled by the output voltage fed back to the error amplifier. If the output voltage goes up, the duty cycle will decrease since the error amplifier will pick off a smaller portion of the triangular wave. Similarly, the duty cycle will decrease if the output voltage drops. Hence, the duty cycle is controlled to produce the desired output voltage.

Without a synchronous drive signal, the circuit will self oscillate at a frequency determined by L1 and C1. This self-oscillation frequency must be lower than the synchronous drive frequency. Therefore, more filtering is required for a driven regulator than for a self-oscillating regulator operating at the same frequency. This also means that a driven regulator will have less output ripple.

The value of C2 is chosen so that its capacitive reactance at the drive frequency is less than one-tenth the resistance of R2. The amplitude of the triangular wave is set at 25 mV with R5. It is advisable to ac couple the drive signal by putting a capacitor in series with R5 so that it does not disturb the dc reference voltage developed for the error amplifier.

THE LM104 REGULATOR

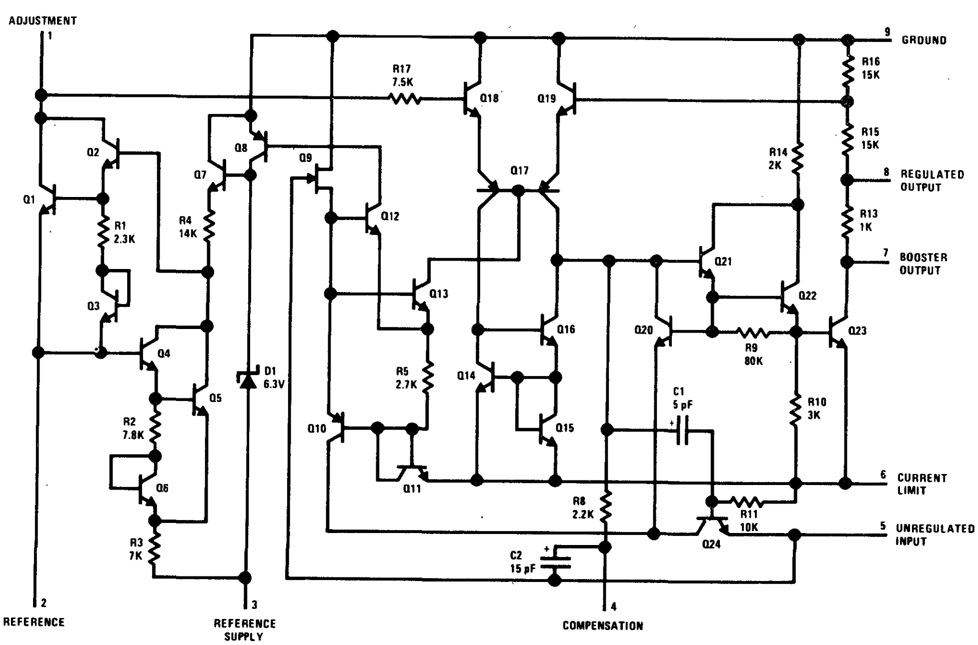
The basic reference for the regulator is zener diode D1. The reference diode is supplied from a PNP current source, Q8, which has a fixed current gain of 2. This arrangement permits the circuit to operate with unregulated input voltages as low as 7V, substantially increasing the efficiency of low-voltage regulators.

The reference supply is temperature compensated by using the negative temperature coefficient of the transistor emitter-base voltages to cancel the positive coefficient of the zener diode. The design produces a nominal 2.4V between the reference and reference supply terminals of the integrated circuit. Connecting an external 2.4 KΩ resistor between those terminals gives a 1 mA reference current from the collectors of Q1 and Q2, which is independent of temperature. The reference voltage supplied to the error amplifier is developed across a second external resistor connected between the adjustment terminal and ground.

The reference supply terminal is normally connected to the unregulated supply. However, improved line regulation can be obtained by pre-regulating the voltage on this terminal. This improvement occurs because Q1, Q2, and Q7 do not see changes in input voltage. Normally, it is the change in the emitter-base voltage of these transistors with changes in collector-base voltage which determines the line regulation.

When the reference supply and unregulated input terminals are operated from separate voltage sources, it is important to make sure that the unregulated input terminal of the integrated circuit does not get more than 2V more positive than the reference supply terminal. If this happens, the collector-isolation junction of Q6 becomes forward biased and disrupts the reference.

The error amplifier of the regulator is quite similar to the LM101 operational amplifier. Emitter



follower input transistors, Q18 and Q19, drive a dual PNP which is operated in the common-base configuration. The current gain of these PNP transistors is fixed at 4 so that the base can be driven by a current source (Q13). Active collector loads are used for the input stage so that a voltage gain of 2000 is obtained. Q21 and Q22 provide enough current gain to keep the internal, series-pass transistor from loading the input stage. R14 limits the base drive on Q23 when it saturates with low, unregulated input voltages. The collector of Q23 is brought out separately so that an external booster transistor can be added for increased output current capability. R13 established the minimum operating current in Q23 when booster transistors are used.

One feature of the error amplifier is that it operates properly with common mode voltages all the way up to ground. Because of this, the circuit will regulate with output voltages to zero volts.

Current limiting is provided by Q24. When the voltage between the current limit and unregulated input terminals becomes large enough to turn on Q24, it will pull Q10 out of saturation and remove base drive from Q21 through Q20. This causes the series pass transistor to exhibit a constant current characteristic. The pre-load current, provided for Q24 by Q10 before current limiting is initiated, gives a much sharper current-limit characteristic. C1 and R11 are included in the limiting circuitry to suppress oscillations.

The error amplifier is connected to a divider on the output (R15 and R16) to keep the reference current generator from saturating with low input-output voltage differentials. A compensating resistor, R17, which is equal to the equivalent resistance of the divider is included to minimize offset error in the error amplifier.

The major feedback loop is frequency compensated by the brute-force method of rolling off the response with a relatively large capacitor on the output. C2 is included on the integrated circuit to compensate for the effects of series resistance in the output capacitor. A compensation point is also brought out so that more capacitance can be added across C2 for certain regulator configurations. R8 improves the load-transient response, especially when compensation is added on Pin 4.

The purpose of Q9, which is a collector FET, is to bias the current-source transistors, Q12 and Q13. It also supplies the preload current for the current-limit transistor, Q24, through Q10.

January 1969

THE LM105 – AN IMPROVED POSITIVE REGULATOR

INTRODUCTION

IC voltage regulators are seeing rapidly increasing usage. The LM100, one of the first, has already been widely accepted. Designed for versatility, this circuit can be used as a linear regulator, a switching regulator, a shunt regulator, or even a current regulator. The output voltage can be set between 2V and 30V with a pair of external resistors, and it works with unregulated input voltages down to 7V. Dissipation limitations of the IC package restrict the output current to less than 20 mA, but external transistors can be added to obtain output currents in excess of 5A. The LM100 and an extensive description of its use in many practical circuits are described in References 1-3.

One complaint about the LM100 has been that it does not have good enough regulation for certain applications. In addition, it becomes difficult to prove that the load regulation is satisfactory under worst-case design conditions. These problems prompted development of the LM105, which is nearly identical to the LM100 except that a gain stage has been added for improved regulation. In the great majority of applications, the LM105 is a plug-in replacement for the LM100.

THE IMPROVED REGULATOR

The load regulation of the LM100 is about 0.1%, no load to full load, without current limiting. When short circuit protection is added, the regulation begins to degrade as the output current becomes greater than about half the limiting current. This is illustrated in Figure 1. The LM105, on the other hand, gives 0.1% regulation up to currents closely approaching the short circuit current. As shown in Figure 1b, this is particularly significant at high temperatures.

The current limiting characteristics of a regulator are important for two reasons: First, it is almost mandatory that a regulator be short-circuit protected because the output is distributed to enough

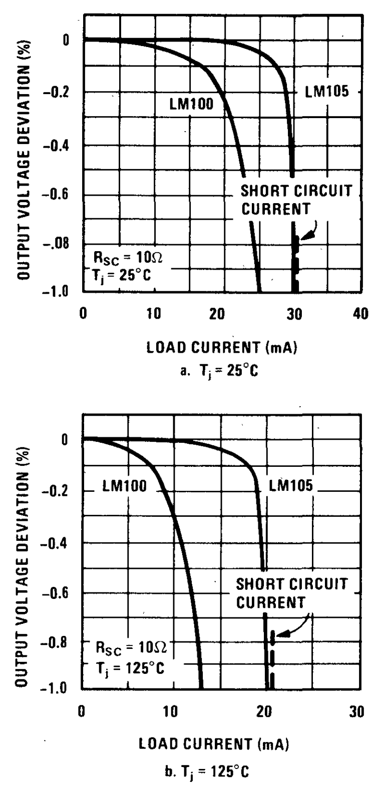


FIGURE 1. Comparison Between the Load Regulation of the LM100 and LM105 for Equal Short Circuit Currents

places that the probability of it becoming shorted is quite high. Secondly, the sharpness of the limiting characteristics is not improved by the addition of external booster transistors. External transistors can increase the maximum output current, but they do not improve the load regulation at currents approaching the short circuit current. Thus, it can be seen that the LM105 provides more than ten times better load regulation in practical power supply designs.

Figure 2 shows that the LM105 also provides better line regulation than the LM100. These curves give the percentage change in output voltage for an incremental change in the unregulated input voltage. They show that the line regulation is worst for small differences between the input and output voltages. The LM105 provides about three times better regulation under worst case conditions. Bypassing the internal reference of the regulator makes the ripple rejection of the LM105 almost a factor of ten better than the LM100 over the entire operating range, as shown in the figure. This bypass capacitor also eliminates noise generated in the internal reference zener of the IC.

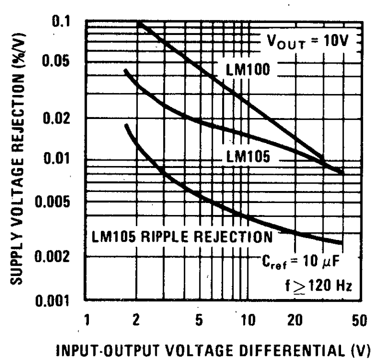


FIGURE 2. Comparison Between the Line Regulation Characteristics of the LM100 and LM105.

The LM105 has also benefited from the use of new IC components developed after the LM100 was designed. These have reduced the internal power consumption so that the LM105 can be specified for input voltages up to 50V and output voltages to 40V. The minimum preload current required by the LM100 is not needed on the LM105.

CIRCUIT DESCRIPTION

The differences between the LM100 and the LM105 can be seen by comparing the schematic diagrams in Figures 3 and 4. Q4 and Q5 have been added to the LM105 to form a common-collector, common-base, common-emitter amplifier, rather than the single common-emitter differential amplifier on the LM100.

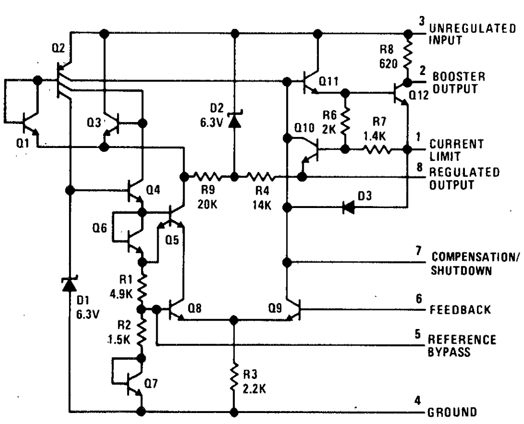


FIGURE 3. Schematic Diagram of the LM100 Regulator.

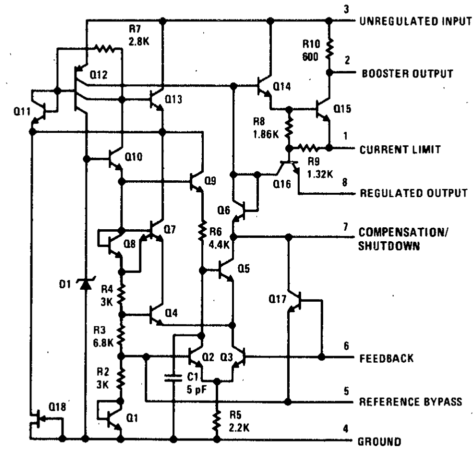


FIGURE 4. Schematic Diagram of the LM105 Regulator.

In the LM100, generation of the reference voltage starts with zener diode, D1, which is supplied with a fixed current from one of the collectors of Q2. This regulated voltage, which has a positive temperature coefficient, is buffered by Q4, divided down by R1 and R2 and connected in series with a diode-connected transistor, Q7. The negative temperature coefficient of Q7 cancels out the positive coefficient of the voltage across R2, producing a temperature-compensated 1.8V on the base of Q8. This point is also brought outside the circuit so that an external capacitor can be added to bypass any noise from the zener diode.

Transistors Q8 and Q9 make up the error amplifier of the circuit. A gain of 2000 is obtained from this single stage by using a current source, another collector on Q2, as a collector load. The output of the amplifier is buffered by Q11 and used to drive the series-pass transistor, Q12. The collector of Q12 is brought out so that an external PNP transistor, or PNP–NPN combination, can be added for increased output current.

Current limiting is provided by Q10. When the voltage across an external resistor connected between Pins 1 and 8 becomes high enough to turn on Q10, it removes the base drive from Q11 so the regulator exhibits a constant-current characteristic. Prebiasing the current limit transistor with a portion of the emitter-base voltage of Q12 from R6 and R7 reduces the current limit sense voltage. This increases the efficiency of the regulator, especially when foldback current limiting is used. With foldback limiting, the voltage dropped across the current sense resistor is about four times larger than the sense voltage.

As for the remaining details, the collector of the amplifier, Q9, is brought out so that external collector-base capacitance can be added to frequency-stabilize the circuit when it is used as a linear regulator. This terminal can also be grounded to shut the regulator off. R9 and R4 are used to start up the regulator, while the rest of the circuitry establishes the proper operating levels for the current source transistor, Q2.

The reference circuitry of the LM105 is the same, except that the current through the reference divider, R2, R3 and R4, has been reduced by a factor of two on the LM105 for reduced power consumption. In the LM105, Q2 and Q3 form an emitter coupled amplifier, with Q3 being the emitter-follower input and Q2 the common-base output amplifier. R6 is the collector load for this stage, which has a voltage gain of about 20. The second stage is a differential amplifier, using Q4 and Q5. Q5 actually provides the gain. Since it has a current source as a collector load, one of the collectors of Q12, the gain is quite high: about 1500. This gives a total gain in the error amplifier of about 30,000, which is ten times higher than the LM100.

It is not obvious from the schematic, but the first stage (Q2 and Q3) and second stage (Q4 and Q5) of the error amplifier are closely balanced when the circuit is operating. This will be true regardless of the absolute value of components and over the operating temperature range. The only thing affecting balance is component matching, which is good in a monolithic integrated circuit, so the error amplifier has good drift characteristics over a wide temperature range.

Frequency compensation is accomplished with an external integrating capacitor around the error amplifier, as with the LM100. This scheme makes the stability insensitive to loading conditions—resistive or reactive—while giving good transient response. However, an internal capacitor, C1, is added to prevent minor-loop oscillations due to the increased gain.

Additional differences between the LM100 and LM105 are that a field-effect transistor, Q18, connected as a current source starts the regulator when power is first applied. Since this current source is connected to ground, rather than the output, the minimum load current before the regulator drops out of operation with large input-output voltage differentials is greatly reduced. This also minimizes power dissipation in the integrated circuit when the difference between the input and output voltage is at the worst-case value. With the LM105 circuit configuration, it was also necessary to add Q17 to eliminate a latch-up mechanism which could exist with lower output-voltage settings. Without Q17, this could occur when Q3 saturated and cut off the second stage amplifiers, Q4 and Q5, causing the output to latch at a voltage nearly equal to the unregulated input.

POWER LIMITATIONS

Although it is desirous to put as much of the regulator as possible on the IC chip, there are certain basic limitations. For one, it is not a good idea to put the series pass transistor on the chip. The power that must be dissipated in the pass transistor is too much for practical IC packages. Further, IC's must be rated at a lower maximum operating temperature than power transistors. This means that even with a power package, a more-massive heat sink would be required if the pass transistor was included in the IC.

Assuming that these problems could be solved, it is still not advisable to put the pass transistor on the same chip with the reference and control circuitry: changes in the unregulated input voltage or load current produce gross variations in chip temperature. These variations worsen load and line regulation due to temperature interaction with the control and reference circuitry.

To elaborate, it is reasonable to neglect the package problem since it is potentially solvable. The lower, maximum operating temperatures of IC's, however, present a more basic problem. The control circuitry in an IC regulator runs at fairly low currents. As a result, it is more sensitive to leakage currents and other phenomena which degrades the performance of semiconductors at high temperatures. Hence, the maximum operating temperature is limited to 150°C in military temperature range applications. On the other hand, a power transistor operating at high currents may be run at temperatures up to 200°C, because even a 1 mA leakage current would not affect its operation in a properly designed circuit. Even if the pass transistor developed a permanent 1 mA leakage from channeling, operating under these conditions of high stress, it would not affect circuit operation. These conditions would not trouble the pass transistor, but they would most certainly cause complete failure of the control circuitry.

These problems are not eliminated in applications with a lower maximum operating temperature. Integrated circuits are sold for limited temperature range applications at considerably lower cost. This is mainly based on a lower maximum junction temperature. They may be rated so that they do not blow up at higher temperatures, but they are not guaranteed to operate within specifications at these temperatures. Therefore, in applications with a lower maximum ambient temperature, it is necessary to purchase an expensive full temperature range part in order to take advantage of the theoretical maximum operating temperatures of the IC.

Figure 5 makes the point about dissipation limitations more strongly. It gives the maximum short circuit output current for an IC regulator in a TO-5 package, assuming a 25°C temperature rise between the chip and ambient and a quiescent current of 2 mA. Dual-in-line or flat packages give results which are, at best, slightly better, but are usually worse. If the short circuit current is not of prime concern, Figure 5 can also be used to give the maximum output current as a function of input-output voltage differential. However, the increased dissipation due to the quiescent current flowing at the maximum input voltage must be taken into account. In addition, the input-output differential must be measured with the maximum expected input voltages.

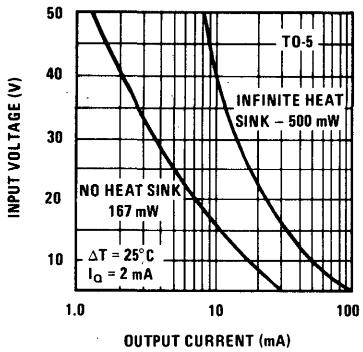


FIGURE 5. Dissipation Limited Short Circuit Output Current for an IC Regulator in a TO-5 Package.

The 25°C temperature rise assumed in arriving at Figure 5 is not at all unreasonable. With military temperature range parts, this is valid for a maximum junction temperature of 150°C with a 125°C ambient. For low cost parts, marketed for limited temperature range applications, this maximum differential appropriately derates the maximum junction temperature.

In practical designs, the maximum permissible dissipation will always be to the left of the curve shown for an infinite heat sink in Figure 5. This curve is realized with the package immersed in circulating acetone, freon or mineral oil. Most heat sinks are not quite as good.

To summarize, power transistors can be run with a temperature differential, junction to ambient, 3 to 5 times as great as an integrated circuit. This means that they can dissipate much more power, even with a smaller heat sink. This, coupled with the fact that low cost, multilead power packages are not available and that there can be thermal interactions between the control circuitry and the pass transistor, strongly suggests that the pass transistors be kept separate from the integrated circuit.

USING BOOSTER TRANSISTORS

Figure 6 shows how an external pass transistor is added to the LM105. The addition of an external PNP transistor does not increase the minimum input output voltage differential. This would happen if an NPN transistor was used in a compound emitter follower connection with the NPN output transistor of the IC. A single-diffused, wide base transistor like the 2N3740 is recommended because it causes fewer oscillation problems than double-diffused, planar devices. In addition, it seems to be less prone to failure under overload conditions; and low cost devices are available in power packages like the TO-66 or even TO-3.

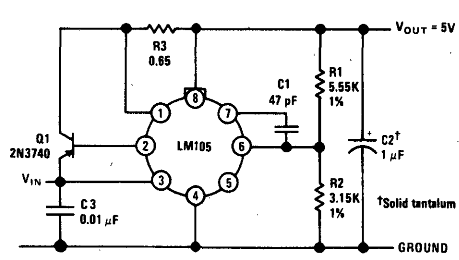


FIGURE 6. 0.2A Regulator.

When the maximum dissipation in the pass transistor is less than about 0.5W, a 2N2905 may be used as a pass transistor. However, it is generally necessary to carefully observe thermal deratings and provide some sort of heat sink.

In the circuit of Figure 6, the output voltage is determined by R1 and R2. The resistor values are selected based on a feedback voltage of 1.8V to Pin 6 of the LM105. To keep thermal drift of the output voltage within specifications, the parallel combination of R1 and R2 should be approximately 2K. However, this resistance is not critical. Variations of ±30% will not cause an appreciable degradation of temperature drift.

The 1 μF output capacitor, C2, is required to suppress oscillations in the feedback loop involving the external booster transistor, Q1, and the output transistor of the LM105. C1 compensates the internal regulator circuitry to make the stability independent for all loading conditions. C3 is not normally required if the lead length between the regulator and the output filter of the rectifier is short.

Current limiting is provided by R3. The current limit resistor should be selected so that the maximum voltage drop across it, at full load current, is equal to the voltage given in Figure 7 at the maximum junction temperature of the IC. This assures a no load to full load regulation better than 0.1% under worst-case conditions.

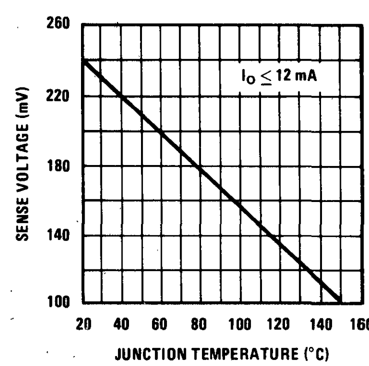


FIGURE 7. Maximum Voltage Drop Across Current Limit Resistor at Full Load for Worst Case Load Regulation of 0.1%.

The short circuit output current is also determined by R3. Figure 8 shows the voltage drop across this resistor, when the output is shorted, as a function of junction temperature in the IC.

With the type of current limiting used in Figure 6, the dissipation under short circuit conditions can be more than three times the worst-case full load dissipation. Hence, the heat sink for the pass tran-

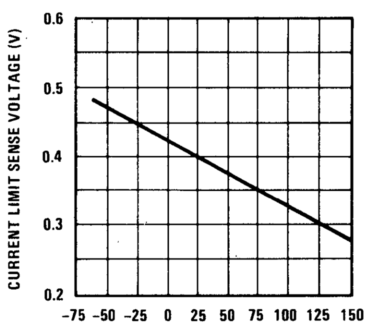


FIGURE 8. Voltage Drop Across Current Limit Resistor Required to Initiate Current Limiting.

sistor must be designed to accommodate the increased dissipation if the regulator is to survive more than momentarily with a shorted output. It is encouraging to note, however, that the short circuit current will decrease at higher ambient temperatures. This assists in protecting the pass transistor from excessive heating.

FOLDBACK CURRENT LIMITING

With high current regulators, the heat sink for the pass transistor must be made quite large in order to handle the power dissipated under worst-case conditions. Making it more than three times larger to withstand short circuits is sometimes inconvenient in the extreme. This problem can be solved with foldback current limiting, which makes the output current under overload conditions decrease below the full load current as the output voltage is pulled down. The short circuit current can be made but a fraction of the full load current.

A high current regulator using foldback limiting is shown in Figure 9. A second booster transistor, Q1, has been added to provide 2A output current without causing excessive dissipation in the LM105. The resistor across its emitter base junction bleeds off any collector base leakage and establishes a minimum collector current for Q2 to make the circuit easier to stabilize with light loads. The foldback characteristic is produced with R4 and R5. The voltage across R4 bucks out the voltage dropped across the current sense resistor,

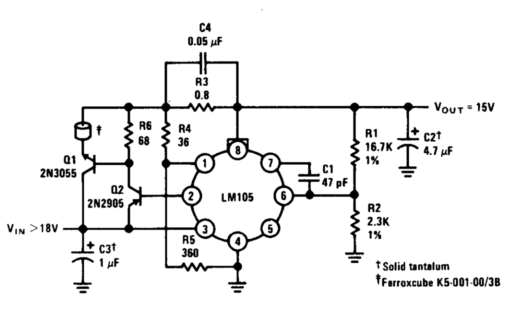


FIGURE 9. 2A Regulator with Foldback Current Limiting.

R3. Therefore, more voltage must be developed across R3 before current limiting is initiated. After the output voltage begins to fall, the bucking voltage is reduced, as it is proportional to the output voltage. With the output shorted, the current is reduced to a value determined by the current limit resistor and the current limit sense voltage of the LM105.

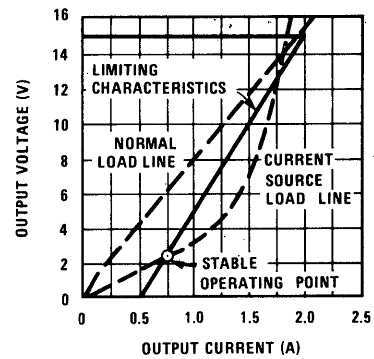


FIGURE 10. Limiting Characteristics of Regulator Using Foldback Current Limiting.

Figure 10 illustrates the limiting characteristics. The circuit regulates for load currents up to 2A. Heavier loads will cause the output voltage to drop, reducing the available current. With a short on the output, the current is only 0.5A.

In design, the value of R3 is determined from

$$R_3 = \frac{V_{lim}}{I_{SC}}, \tag{1}$$

where V_{lim} is the current limit sense voltage of the LM105, given in Figure 8, and I_{SC} is the design value of short circuit current. R5 is then obtained from

$$R_5 = \frac{V_{OUT} + V_{sense}}{I_{bleed} + I_{bias}}, \tag{2}$$

where V_{OUT} is the regulated output voltage, V_{sense} is maximum voltage across the current limit resistor for 0.1% regulation as indicated in Figure 7, I_{bleed} is the preload current on the regulator output provided by R5 and I_{bias} is the maximum current coming out of Pin 1 of the LM105 under full load conditions. I_{bias} will be equal to 2 mA plus the worst-case base drive for the PNP booster transistor, Q2. I_{bleed} should be made about ten times greater than I_{bias}.

Finally, R4 is given by

$$R_4 = \frac{I_{FL} R_3 - V_{sense}}{I_{bleed}} \tag{3}$$

where I_{FL} is the output current of the regulator at full load.

It is recommended that a ferrite bead be strung on the emitter of the pass transistor, as shown in Figure 9, to suppress oscillations that may show up with certain physical configurations. It is advisable to also include C4 across the current limit resistor.

In some applications, the power dissipated in Q2 becomes too great for a 2N2905 under worst-case conditions. This can be true even if a heat sink is used, as it should be in almost all applications. When dissipation is a problem, the 2N2905 can be replaced with a 2N3740. With a 2N3740, the ferrite bead and C4 are not needed because this transistor has a lower cutoff frequency.

One of the advantages of foldback limiting is that it sharpens the limiting characteristics of the IC. In addition, the maximum output current is less sensitive to variations in the current limit sense voltage of the IC: in this circuit, a 20% change in sense voltage will only affect the trip current by 5%. The temperature sensitivity of the full load current is likewise reduced by a factor of four, while the short circuit current is not.

Even though the voltage dropped across the sense resistor is larger with foldback limiting, the minimum input-output voltage differential of the complete regulator is not increased above the 3V specified for the LM105 as long as this drop is less than 2V. This can be attributed to the low sense voltage of the IC by itself.

Figure 10 shows that foldback limiting can only be used with certain kinds of loads. When the load looks predominately like a current source, the load line can intersect the foldback characteristic at a point where it will prevent the regulator from coming up to voltage, even without an overload. Fortunately, most solid state circuitry presents a load line which does not intersect. However, the possibility cannot be ignored, and the regulator must be designed with some knowledge of the load.

With foldback limiting, power dissipation in the pass transistor reaches a maximum at some point between full load and short circuited output. This is illustrated in Figure 11. However, if the maximum dissipation is calculated with the worst-case input voltage, as it should be, the power peak is not too high.

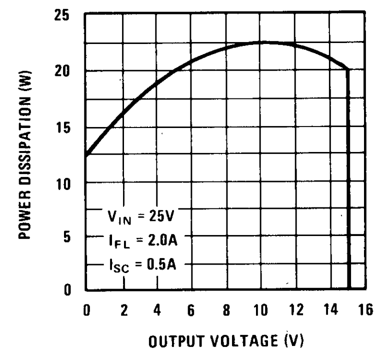


FIGURE 11. Power Dissipation in Series Pass Transistors Under Overload Conditions in Regulator Using Foldback Current Limiting.

HIGH CURRENT REGULATOR

The output current of a regulator using the LM105 as a control element can be increased to any desired level by adding more booster transistors, increasing the effective current gain of the pass transistors. A circuit for a 10A regulator is shown in Figure 12. A third NPN transistor has been included to get higher current. A low frequency device is used for Q3 because it seems to better withstand abuse. However, high frequency transistors must be used to drive it. Q2 and Q3 are both double-diffused transistors with good frequency response. This insures that Q3 will present the dominant lag in the feedback loop through the booster transistors, and back around the output transistor of the LM105. This is further insured by the addition of C3.

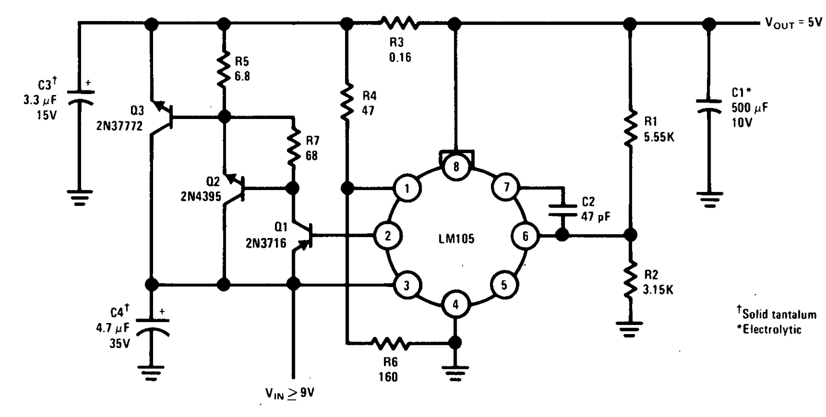


FIGURE 12. 10A Regulator with Foldback Current Limiting.

The circuit, as shown, has a full load capability of 10A. Foldback limiting is used to give a short circuit output current of 2.5A. The addition of Q3 increases the minimum input-output voltage differential, by 1V, to 4V.

DOMINANT FAILURE MECHANISMS

By far, the biggest reason for regulator failures is overdissipation in the series pass transistors. This has been borne out by experience with the LM100. Excessive heating in the pass transistors causes them to short out, destroying the IC. This has happened most frequently when PNP booster transistors in a TO-5 can, like the 2N2905, were used. Even with a good heat sink, these transistors cannot dissipate much more than 1W. The maximum dissipation is less in many applications. When a single PNP booster is used and power can be a problem, it is best to go to a transistor like the 2N3740, in a TO-66 power package, using a good heat sink.

Using a compound PNP/NPN booster does not solve all problems. Even when breadboarding with transistors in TO-3 power packages, heat sinks must be used. The TO-3 package is not very good, thermally, without a heat sink. Dissipation in the PNP transistor driving the NPN series pass transistor cannot be ignored either. Dissipation in the driver with worst-case current gain in the pass transistor must be taken into account. In certain cases, this could require that a PNP transistor in a power package be used to drive the NPN pass transistor. In almost all cases, a heat sink is required if a PNP driver transistor in a TO-5 package is selected.

With output currents above 3A, it is good practice to replace a 2N3055 pass transistor with a 2N3772. The 2N3055 is rated for higher currents than 3A, but its current gain falls off rapidly. This is especially true at either high temperatures or low input-output voltage differentials. A 2N3772 will give substantially better performance at high currents, and it makes life much easier for the PNP driver.

The second biggest cause of failures has been the output filter capacitors on power inverters providing unregulated power to the regulator. If these capacitors are operated with excessive ripple across them, and simultaneously near their maximum dc voltage rating, they will sputter. That is, they short momentarily and clear themselves. When they short, the output capacitor of the regulator is discharged back through the reverse biased pass transistors or the control circuitry, frequently causing destruction. This phenomenon is especially prevalent when solid tantalum capacitors are used with high-frequency power inverters. The maximum ripple allowed on these capacitors decreases linearly with frequency.

The solution to this problem is to use capacitors with conservative voltage ratings. In addition, the maximum ripple allowed by the manufacturer at the operating frequency should also be observed.

The problem can be eliminated completely by installing a diode between the input and output of the regulator such that the capacitor on the output is discharged through this diode if the input is shorted. A fast switching diode should be used as ordinary rectifier diodes are not always effective.

Another cause of problems with regulators is severe voltage transients on the unregulated input. Even if these transients do not cause immediate failure in the regulator, they can feed through and destroy the load. If the load shorts out, as is frequently the case, the regulator can be destroyed by subsequent transients.

This problem can be solved by specifying all parts of the regulator to withstand the transient conditions. However, when ultimate reliability is needed, this is not a good solution. Especially since the regulator can withstand the transient, yet severely overstress the circuitry on its output by feeding the transients through. Hence, a more logical recourse is to include circuitry which suppresses the transients. A method of doing this is shown in Figure 13. A zener diode, which can handle

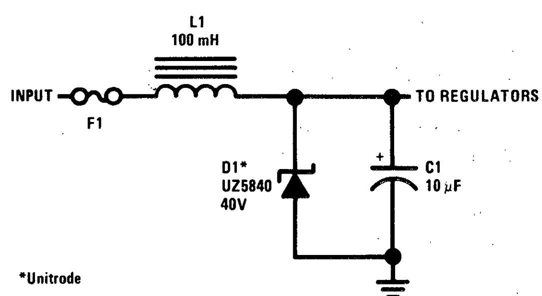


FIGURE 13. Suppression Circuitry to Remove Large Voltage Spikes from Unregulated Supplies.

large peak currents, clamps the input voltage to the regulator while an inductor limits the current through the zener during the transient. The size of the inductor is determined from

$$L = \frac{\Delta V \Delta t}{I} \tag{4}$$

where ΔV is the voltage by which the input transient exceeds the breakdown voltage of the diode, Δt is the duration of the transient and I is the peak current the zener can handle while still clamping the input voltage to the regulator. As shown, the suppression circuit will clamp 70V, 4 ms transients on the unregulated supply.

CONCLUSIONS

The LM105 is an exact replacement for the LM100 in the majority of applications, providing about ten times better regulation. There are, however, a few differences:

In switching regulator applications,[2] the size of the resistor used to provide positive feedback should be doubled as the impedance seen looking back into the reference bypass terminal is twice that of the LM100 (2 KΩ versus 1 KΩ). In addition, the minimum output voltage of the LM105 is 4.5V, compared with 2V for the LM100. In low voltage regulator applications, the effect of this is obvious. However, it also imposes some limitations on current regulator and shunt regulator designs.[3] Lastly, clamping the compensation terminal (Pin 7) within a diode drop of ground or the output terminal will not guarantee that the regulator is shut off, as it will with the LM100. This restricts the LM105 in the overload shutoff schemes[3] which can be used with the LM100.

Dissipation limitations of practical packages dictate that the output current of an IC regulator be less than 20 mA. However, external booster transistors can be added to get any output current desired. Even with satisfactory packages, considerably larger heat sinks would be needed if the pass transistors were put on the same chip as the reference and control circuitry, because an IC must be run at a lower maximum temperature than a power transistor. In addition, heat dissipated in the pass transistor couples into the low level circuitry and degrades performance. All this suggests that the pass transistor be kept separate from the IC.

Overstressing series pass transistors has been the biggest cause of failures with IC regulators. This not only applies to the transistors within the IC, but also to the external booster transistors. Hence, in designing a regulator, it is of utmost importance to determine the worst-case power dissipation in all the driver and pass transistors. Devices must then be selected which can handle the power. Further, adequate heat sinks must be provided as even power transistors cannot dissipate much power by themselves.

Normally, the highest power dissipation occurs when the output of the regulator is shorted. If this condition requires heat sinks which are so large as to be impractical, foldback current limiting can be used. With foldback limiting, the power dissipated under short circuit conditions can actually be made less than the dissipation at full load.

The LM105 is designed primarily as a positive voltage regulator. A negative regulator, the LM104, which is a functional complement to the LM105, is described in Reference 4.

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June 1969

A SIMPLIFIED TEST SET FOR OPERATIONAL AMPLIFIER CHARACTERIZATION

INTRODUCTION

The test set described in this paper allows complete quantitative characterization of all dc operational amplifier parameters quickly and with a minimum of additional equipment. The method used is accurate and is equally suitable for laboratory or production test—for quantitative readout or for limit testing. As embodied here, the test set is conditioned for testing the LM709 and LM101 amplifiers; however, simple changes discussed in the text will allow testing of any of the generally available operational amplifiers.

Amplifier parameters are tested over the full range of common mode and power supply voltages with either of two output loads. Test set sensitivity and stability are adequate for testing all presently available integrated amplifiers.

The paper will be divided into two sections, i.e., a functional description, and a discussion of circuit operation. Complete construction information will be given including a layout for the tester circuit boards.

FUNCTIONAL DESCRIPTION

The test set operates in one of three basic modes. These are: (1) Bias Current Test; (2) Offset Voltage, Offset Current Test; and (3) Transfer Function Test. In the first two of these tests, the amplifier under test is exercised throughout its full common mode range. In all three tests, power supply voltages for the circuit under test may be set at ±5V, ±10V, ±15V or ±20V.

POWER SUPPLY

Basic waveforms and dc operating voltages for the test set are derived from a power supply section comprising a positive and a negative rectifier and filter, a test set voltage regulator, a test circuit voltage regulator, and a function generator. The dc supplies will be discussed in the section dealing with detailed circuit description.

The waveform generator provides three output functions, a ±19V square wave, a −19V to +19V pulse with a 1% duty cycle, and a ±5V triangular wave. The square wave is the basic waveform from which both the pulse and triangular wave outputs are derived.

The square wave generator is an operational amplifier connected as an astable multivibrator. This amplifier provides an output of approximately ±19V at 16 Hz. This square wave is used to drive junction FET switches in the test set and to generate the pulse and triangular waveforms.

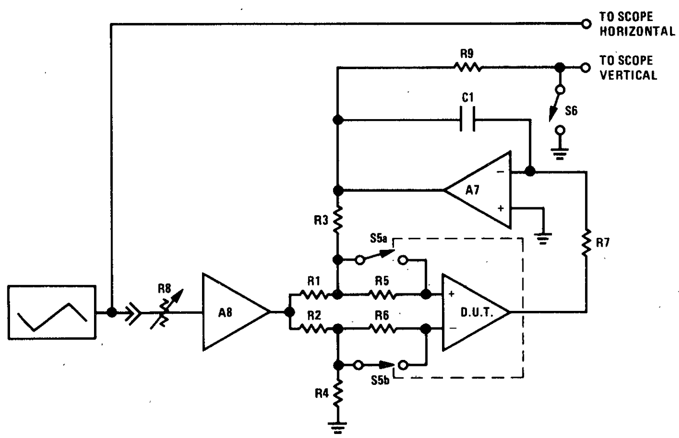


FIGURE 1. Functional Diagram of Bias Current Test Circuit

The pulse generator is a monostable multivibrator driven by the output of the square wave generator. This multivibrator is allowed to swing from negative saturation to positive saturation on the positive going edge of the square wave input and has a time constant which will provide a duty cycle of approximately 1%. The output is approximately −19V to +19V.

The triangular wave generator is a dc stabilized integrator driven by the output of the square wave generator and provides a ±5V output at the square wave frequency, inverted with respect to the square wave.

The purpose of these various outputs from the power supply section will be discussed in the functional description.

BIAS CURRENT TEST

A functional diagram of the bias current test circuit is shown in Figure 1. The output of the triangular wave generator and the output of the test circuit, respectively, drive the horizontal and vertical deflection of an oscilloscope.

The device under test, (cascaded with the integrator, A_7), is connected in a differential amplifier configuration by R_1, R_2, R_3, and R_4. The inputs of this differential amplifier are driven in common from the output of the triangular wave generator through attenuator R_8 and amplifier A_8. The inputs of the device under test are connected to the feedback network through resistors R_5 and R_6, shunted by the switch S_{5a} and S_{5b}.

The feedback network provides a closed loop gain of 1,000 and the integrator time constant serves to reduce noise at the output of the test circuit as well as allowing the output of the device under test to remain near zero volts.

The bias current test is accomplished by allowing the device under test to draw input current to one of its inputs through the corresponding input resistor on positive going or negative going halves of the triangular wave generator output. This is accomplished by closing S_{5a} or S_{5b} on alternate halves of the triangular wave input. The voltage appearing across the input resistor is equal to input current times the input resistor. This voltage is multiplied by 1,000 by the feedback loop and appears at the integrator output and the vertical input of the oscilloscope. The vertical separation of the traces representing the two input currents of the amplifier under test is equivalent to the total bias current of the amplifier under test.

The bias current over the entire common mode range may be examined by setting the output of A_8 equal to the amplifier common mode range. A photograph of the bias current oscilloscope display is given as Figure 2. In this figure, the total input

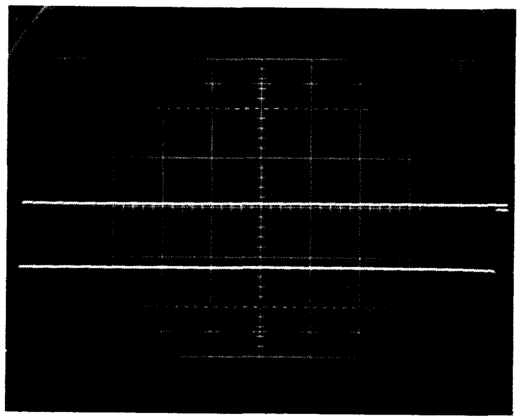


FIGURE 2. Bias Current and Common Mode Rejection Display

current of an amplifier is displayed over a ±10V common mode range with a sensitivity of 100 nA per vertical division.

The bias current display of Figure 2 has the added advantage that incipient breakdown of the input stage of the device under test at the extremes of the common mode range is easily detected.

If either or both the upper or lower trace in the bias current display exhibits curvature near the horizontal ends of the oscilloscope face, then the bias current of that input of the amplifier is shown to be dependent on common mode voltage. The usual causes of this dependency are low breakdown voltage of the differential input stage or current sink.

OFFSET VOLTAGE, OFFSET CURRENT TEST

The offset voltage and offset current tests are performed in the same general way as the bias current test. The only difference is that the switches S_{5a} and S_{5b} are closed on the same half-cycle of the triangular wave input.

The synchronous operation of S_{5a} and S_{5b} forces the amplifier under test to draw its input currents through matched high and low input resistors on alternate halves of the input triangular wave. The difference between the voltage drop across the two values of input resistors is proportional to the difference in input current to the two inputs of the amplifier under test and may be measured as the vertical spacing between the two traces appearing on the face of the oscilloscope.

Offset voltage is measured as the vertical spacing between the trace corresponding to one of the two values of source resistance and the zero volt baseline. Switch S_6 and Resistor R_9 are a base line chopper whose purpose is to provide a baseline reference which is independent of test set and oscilloscope drift. S_6 is driven from the pulse output of the function generator and has a duty cycle of approximately 1% of the triangular wave.

Figure 3 is a photograph of the various waveforms presented during this test. Offset voltage and offset current are displayed at a sensitivity of 1 mV and 100 nA per division, respectively, and both parameters are displayed over a common mode range of ±10V.

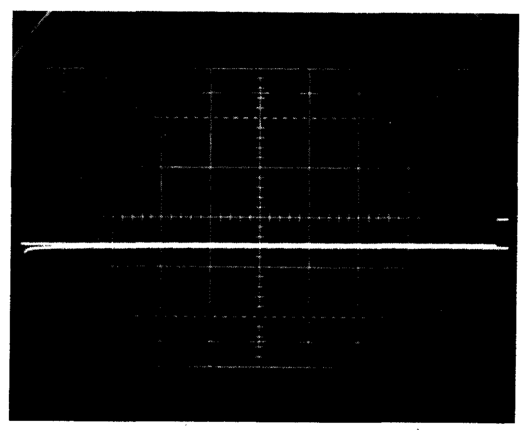


FIGURE 3. Offset Voltage, Offset Current and Common Mode Rejection Display

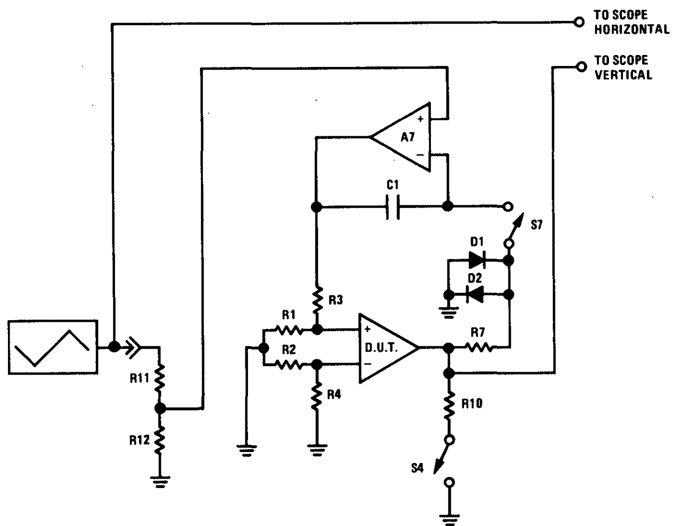


FIGURE 4. Functional Diagram of Transfer Function Circuit

TRANSFER FUNCTION TEST

A functional diagram of the transfer function test is shown in Figure 4. The output of the triangular wave generator and the output of the circuit under test, respectively, drive the horizontal and vertical inputs of an oscilloscope.

The device under test is driven by a ±2.5 mV triangular wave derived from the ±5V output of the triangular wave generator through the attenuators R_{11}, R_{12}, and R_1, R_3 and through the voltage follower, A_7. The output of the device under test is fed to the vertical input of an oscilloscope.

Amplifier A_7 performs a dual function in this test. When S_7 is closed during the bias current test, a voltage is developed across C_1 equal to the amplifier offset voltage multiplied by the gain of the feedback loop. When S_7 is opened in the transfer function test, the charge stored in C_1 continues to provide this offset correction voltage. In addition, A_7 sums the triangular wave test signal with the offset correction voltage and applies this sum to the input of the amplifier under test through the attenuator R_1, R_3. This input sweeps the input of the amplifier under test ±2.5 mV around its offset voltage.

Figure 5 is a photograph of the output of the test set during the transfer function test. This figure illustrates the function of amplifier A_7 in adjusting the dc input of the test device so that its transfer function is displayed on the center of the oscilloscope face.

The transfer function display is a plot of V_{in} vs V_{out} for an amplifier. This display provides information about three amplifier parameters: gain,

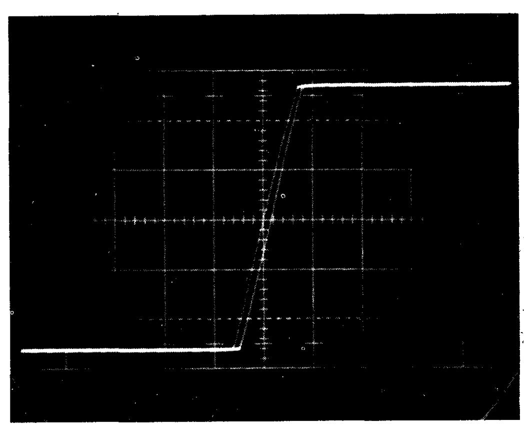


FIGURE 5. Transfer Function Display

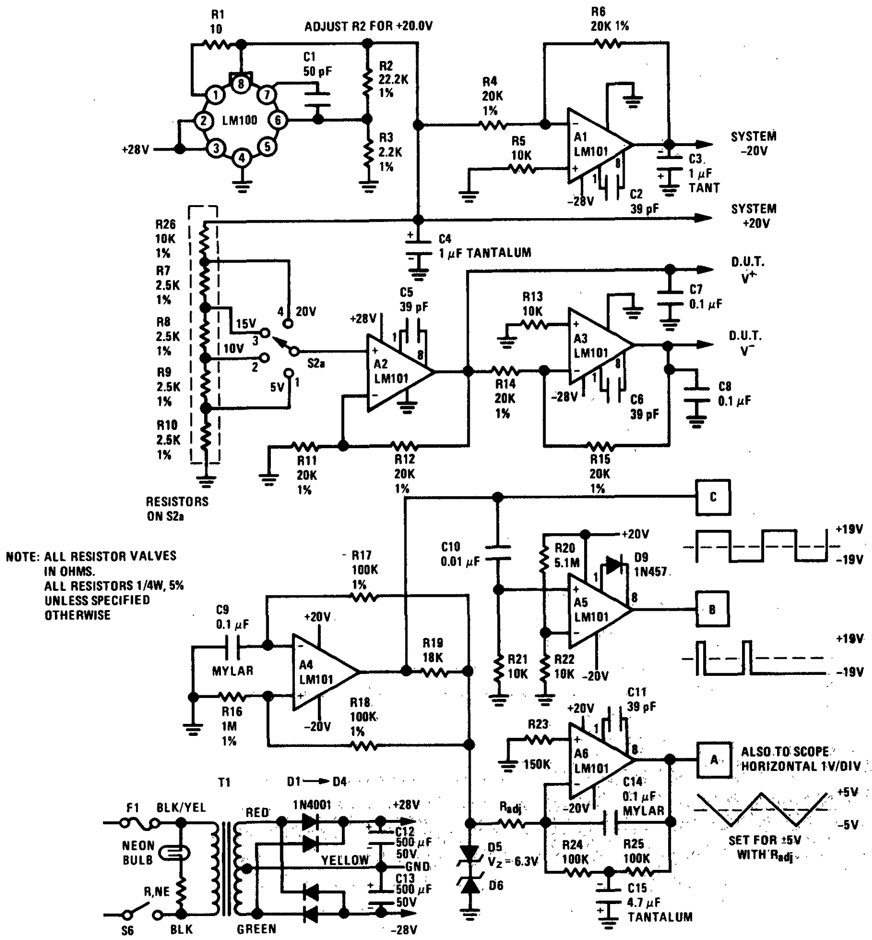


FIGURE 6. Power Supply and Function Generator

gain linearity, and output swing. Gain is displayed as the slope, $\Delta V_{out}/\Delta V_{in}$ of the transfer function. Gain linearity is indicated change in slope of the V_{out}/V_{in} display as a function of output voltage. This display is particularly useful in detecting crossover distortion in a Class B output stage. Output swing is measured as the vertical deflection of the transfer function at the horizontal extremes of the display.

DETAILED CIRCUIT DESCRIPTION

POWER SUPPLIES

As shown in Figure 6, which is a complete schematic of the power supply and function generator, two power supplies are provided in the test set. One supply provides a fixed ±20V to power the circuitry in the test set; the other provides ±5V to ±20V to power the circuit under test.

The test set power supply regulator accepts +28V from the positive rectifier and filter and provides +20V through the LM100 positive regulator. Amplifier A_1 is powered from the negative rectifier and filter and operates as a unity gain inverter whose input is +20V from the positive regulator, and whose output is −20V.

The test circuit power supply is referenced to the +20V output of the positive regulator through the variable divider comprising R_7, R_8, R_9, R_{10}, and R_{26}. The output of this divider is +10V to +2.5V according to the position of S_{2a} and is fed to the non-inverting, gain-of-two amplifier, A_2. A_2 is powered from +28V and provides +20V to +5V at its output. A_3 is a unity gain inverter whose input is the output of A_2 and which is powered from −28V. The complementary outputs of amplifiers A_2 and A_3 provide dc power to the circuit under test.

LM101 amplifiers are used as A_2 and A_3 to allow operation from one ground referenced voltage each and to provide protective current limiting for the device under test.

FUNCTION GENERATOR

The function generator provides three outputs, a ±19V square wave, a −19V to +19V pulse having a 1% duty cycle, and a ±5V triangular wave. The square wave is the basic function from which the pulse and triangular wave are derived, the pulse is referenced to the leading edge of the square wave, and the triangular wave is the inverted and integrated square wave.

Amplifier A_4 is an astable multivibrator generating a square wave from positive to negative saturation. The amplitude of this square wave is approximately ±19V. The square wave frequency is determined by the ratio of R_{18} to R_{16} and by the time constant, $R_{17}C_9$. The operating frequency is stabilized against temperature and power regulation effects by regulating the feedback signal with the divider R_{19}, D_5 and D_6.

Amplifier A_5 is a monostable multivibrator triggered by the positive going output of A_4. The pulse width of A_5 is determined by the ratio of R_{20} to R_{22} and by the time constant $R_{21}C_{10}$. The output pulse of A_5 is an approximately 1% duty cycle pulse from approximately −19V to +19V.

Amplifier A_6 is a dc stabilized integrator driven from the amplitude-regulated output of A_4. Its output is a ±5V triangular wave. The amplitude of the output of A_6 is determined by the square wave voltage developed across D_5 and D_6 and the time constant R_{adj} C_{14}. DC stabilization is accomplished by the feedback network R_{24}, R_{25}, and C_{15}. The ac attenuation of this feedback network is high enough so that the integrator action at the square wave frequency is not degraded.

Operating frequency of the function generator may be varied by adjusting the time constants associated with A_4, A_5, and A_6 in the same ratio.

TEST CIRCUIT

A complete schematic diagram of the test circuit is shown in Figure 7. The test circuit accepts the outputs of the power supplies and function generator and provides horizontal and vertical outputs for an X-Y oscilloscope, which is used as the measurement system.

The primary elements of the test circuit are the feedback buffer and integrator, comprising amplifier A_7 and its feedback network C_{16}, R_{31}, R_{32}, and C_{17}, and the differential amplifier network, comprising the device under test and the feedback network R_{40}, R_{43}, R_{44}, and R_{52}. The remainder of the test circuit provides the proper conditioning for the device under test and scaling for the oscilloscope, on which the test results are displayed.

The amplifier A_8 provides a variable amplitude source of common mode signal to exercise the amplifier under test over its common mode range. This amplifier is connected as a non-inverting gain-of-3.6 amplifier and receives its input from the triangular wave generator. Potentiometer R_{37} allows the output of this amplifier to be varied from ±0 volts to ±18 volts. The output of this amplifier drives the differential input resistors, R_{43} and R_{44}, for the device under test.

The resistors R_{46} and R_{47} are current sensing resistors which sense the input current of the device under test. These resistors are switched into the circuit in the proper sequence by the field effect transistors Q_6 and Q_7. Q_6 and Q_7 are driven from the square wave output of the function generator by the PNP pair, Q_{10} and Q_{11}, and the NPN pair, Q_8 and Q_9. Switch sections S_{1b} and S_{1c} select the switching sequence for Q_8 and Q_9 and hence for Q_6 and Q_7. In the bias current test, the FET drivers, Q_8 and Q_9, are switched by out of phase signals from Q_{10} and Q_{11}. This opens the FET switches Q_6 and Q_7 on alternate half cycles of the square wave output of the function generator. During the offset voltage, offset current test, the FET drivers are operated synchronously

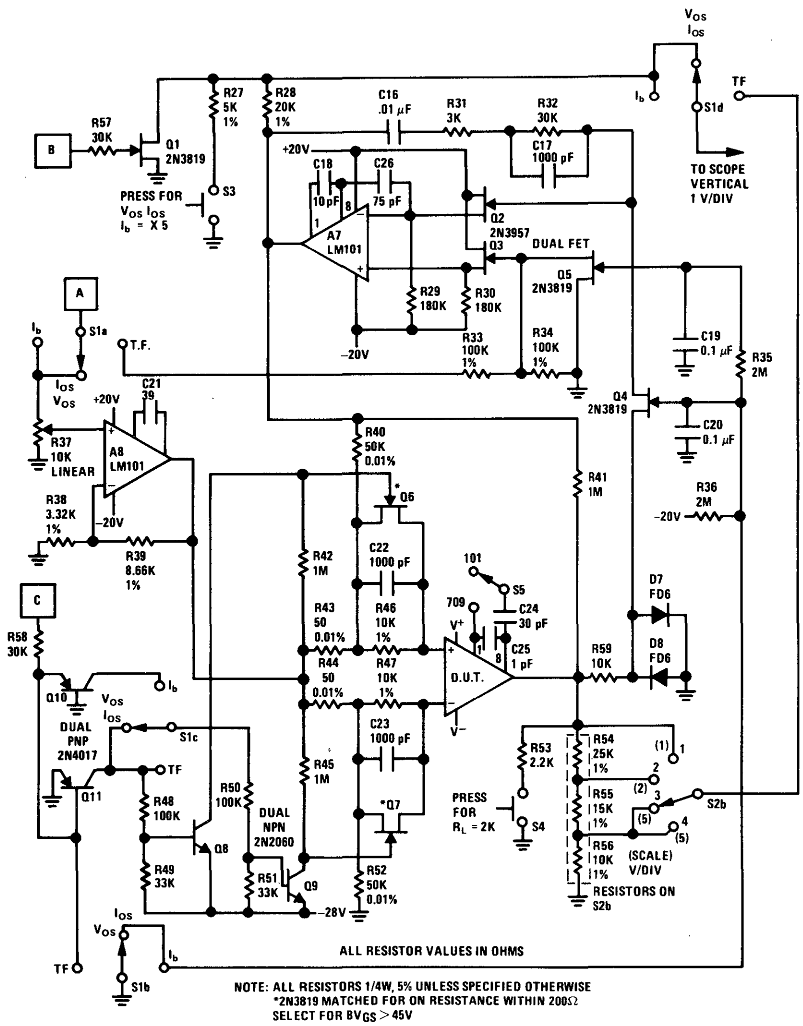


FIGURE 7. Test Circuit

from the output of Q_{11}. During the transfer function test, Q_6 and Q_7 are switched on continuously by turning off Q_{11}. R_{42} and R_{45} maintain the gates of the FET switches at zero gate to source voltage for maximum conductance during their on cycle. Since the sources of these switches are at the common mode input voltage of the device under test, these resistors are connected to the output of the common mode driver amplifier, A_8.

The input for the integrator-feedback buffer, A_7, is selected by the FET switches Q_4 and Q_5. During the bias current and offset voltage offset current tests, A_7 is connected as an integrator and receives its input from the output of the device under test. The output of A_7 drives the feedback resistor, R_{40}. In this connection, the integrator holds the output of the device under test near ground and serves to amplify the voltages corresponding to bias current, offset current, and offset voltage by a factor of 1,000 before presenting them to the measurement system. FET switches Q_4 and Q_5 are turned on by switch section S_{1b} during these tests.

FET switches Q_4 and Q_5 are turned off during the transfer function test. This disconnects A_7 from the output of the device under test and changes it from an integrator to a non-inverting unity gain amplifier driven from the triangular wave output of the function generator through the attenuator R_{33} and R_{34} and switch section S_{1a}. In this connection, amplifier A_7 serves two functions; first, to provide an offset voltage correction to the input of the device under test and, second, to drive the input of the device under test with a ±2.5 mV triangular wave centered about the offset voltage. During this test, the common mode driver amplifier is disabled by switch section S_{1a} and the vertical input of the measurement oscilloscope is transferred from the output of the integrator-buffer, A_7, to the output of the device under test by switch section S_{1d}. S_{2a} allows supply voltages for the device under test to be set at ±5, ±10, ±15, or ±20V. S_{2b} changes the vertical scale factor for the measurement oscilloscope to maintain optimum vertical deflection for the particular power supply voltage used. S_4 is a momentary contact pushbutton switch which is used to change the load on the device under test from 10kΩ to 2kΩ.

A delay must be provided when switching from the input tests to the transfer function tests. The purpose of this delay is to disable the integrator function of A_7 before driving it with the triangular wave. If this is not done, the offset correction voltage, stored on C_{16}, will be lost. This delay between opening FET switch Q_4, and switch Q_5, is provided by the RC filter, R_{35} and C_{19}.

Resistor R_{41} and diodes D_7 and D_8 are provided to control the integrator when no test device is present, or when a faulty test device is inserted. R_{41} provides a dc feedback path in the absence of a test device and resets the integrator to zero. Diodes D_7 and D_8 clamp the input to the integrator to approximately ±.7 volts when a faulty device is inserted.

FET switch Q_1 and resistor R_{28} provide a ground reference at the beginning of the 50-ohm-source, offset-voltage trace. This trace provides a ground reference which is independent of instrument or oscilloscope calibration. The gate of Q_1 is driven by the output of monostable multivibrator A_5, and shorts the vertical oscilloscope drive signal to ground during the time that A_5 output is positive.

Switch S_3, R_{27}, and R_{28} provide a 5X scale increase during input parameter tests to allow measurement of amplifiers with large offset voltage, offset current, or bias current.

Switch S_5 allows amplifier compensation to be changed for 101 or 709 type amplifiers.

CALIBRATION

Calibration of the test system is relatively simple and requires only two adjustments. First, the output of the main regulator is set up for 20V. Then, the triangular wave generator is adjusted to provide ±5V output by selecting R_{adj}. This sets the horizontal sweep for the X-Y oscilloscope used as the measurement system. The oscilloscope is then set up for 1V/division vertical and for a full 10 division horizontal sweep.

Scale factors for the three test positions are:

1. **Bias Current Display** (Figure 2)

I_{bias} total	100 nA/div. vertical
Common Mode Voltage	Variable horizontal

2. **Offset Voltage-Offset Current** (Figure 3)

I_{offset}	100 nA/div. vertical
V_{offset}	1 mV/div. vertical
Common Mode Voltage	Variable horizontal

3. **Transfer Function** (Figure 5)

V_{in}	0.5 mV/div.
V_{out}	5V/div. @ V_s ±20V
	5V/div. @ V_s ±15V
	2V/div. @ V_s ±10V
	1V/div. @ V_s ± 5V

$$\text{Gain} = \frac{\Delta V_{out}}{\Delta V_{in}}$$

CONSTRUCTION

Test set construction is simplified through the use of integrated circuits and etched circuit layout.

Figure 8 gives photographs of the completed tester. Figure 9 shows the parts location for the components on the circuit board layout of Figure 10. An attempt should be made to adhere to this layout to insure that parasitic coupling between elements will not cause oscillations or give calibration problems.

Table 1 is a listing of special components which are needed to fit the physical layout given for the tester.

TABLE 1. Partial Parts List

T_1	Triad F-90X
S_1	Centralab PA2003 non-shorting
S_2	Centralab PA2015 non-shorting
S_3, S_4	Grayhill 30-1 Series 30 subminiature pushbutton switch
S_5, S_6	Alcoswitch MST-105D SPDT

CONCLUSIONS

A semi-automatic test system has been described which will completely test the important operational amplifier parameters over the full power supply and common mode ranges. The system is simple, inexpensive, easily calibrated, and is equally suitable for engineering or quality assurance usage.

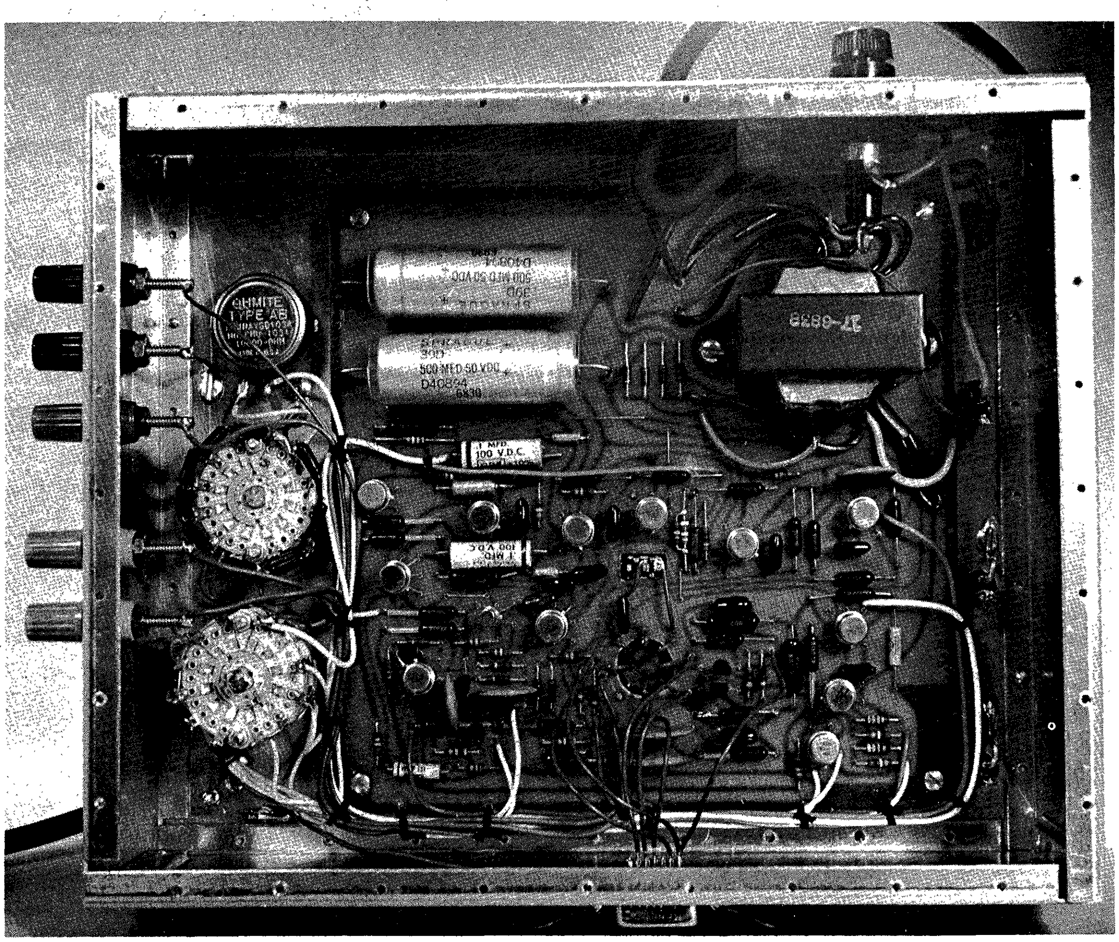


FIGURE 8a. Bottom of Test Set

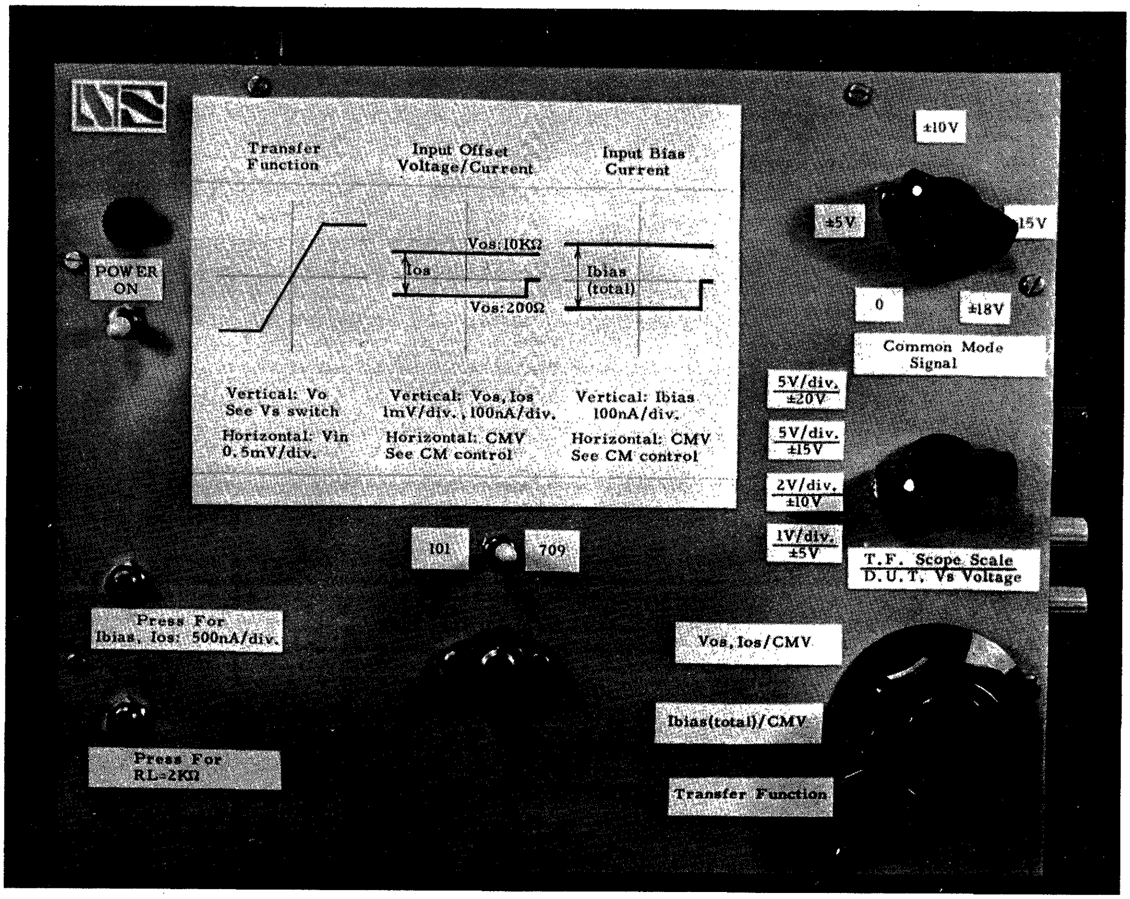


FIGURE 8b. Front Panel

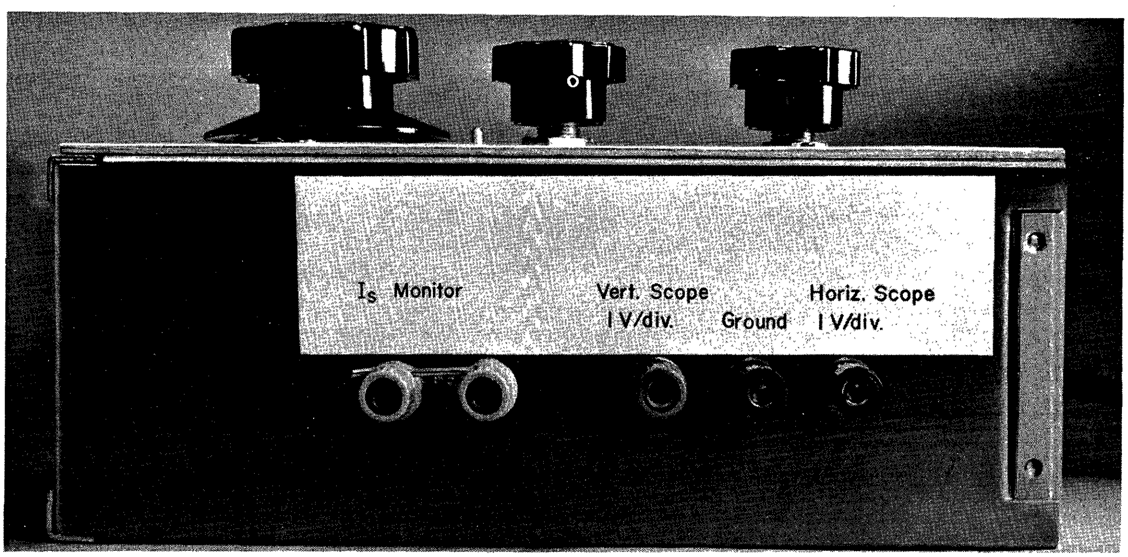


FIGURE 8c. Jacks

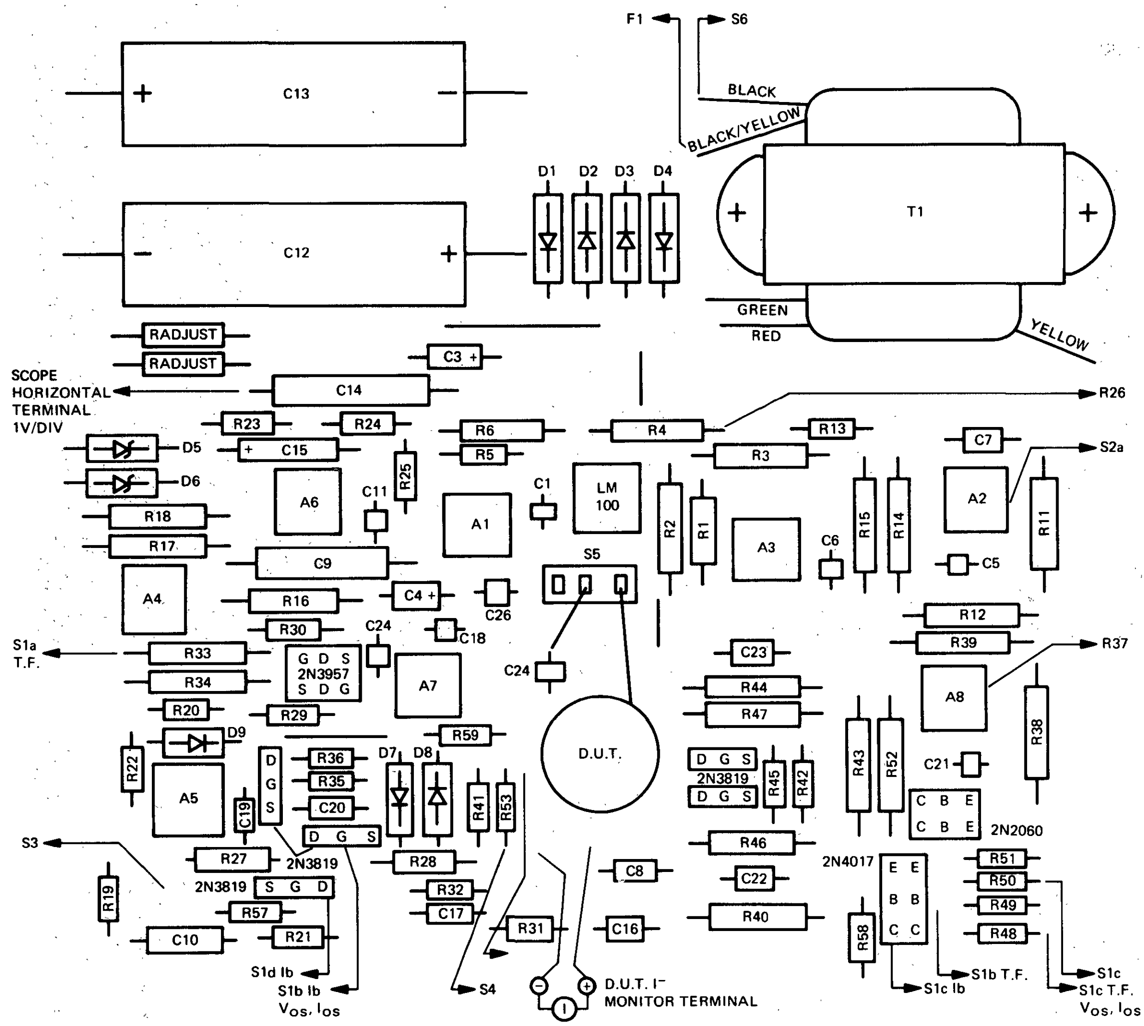


FIGURE 9. Component Location, Top View

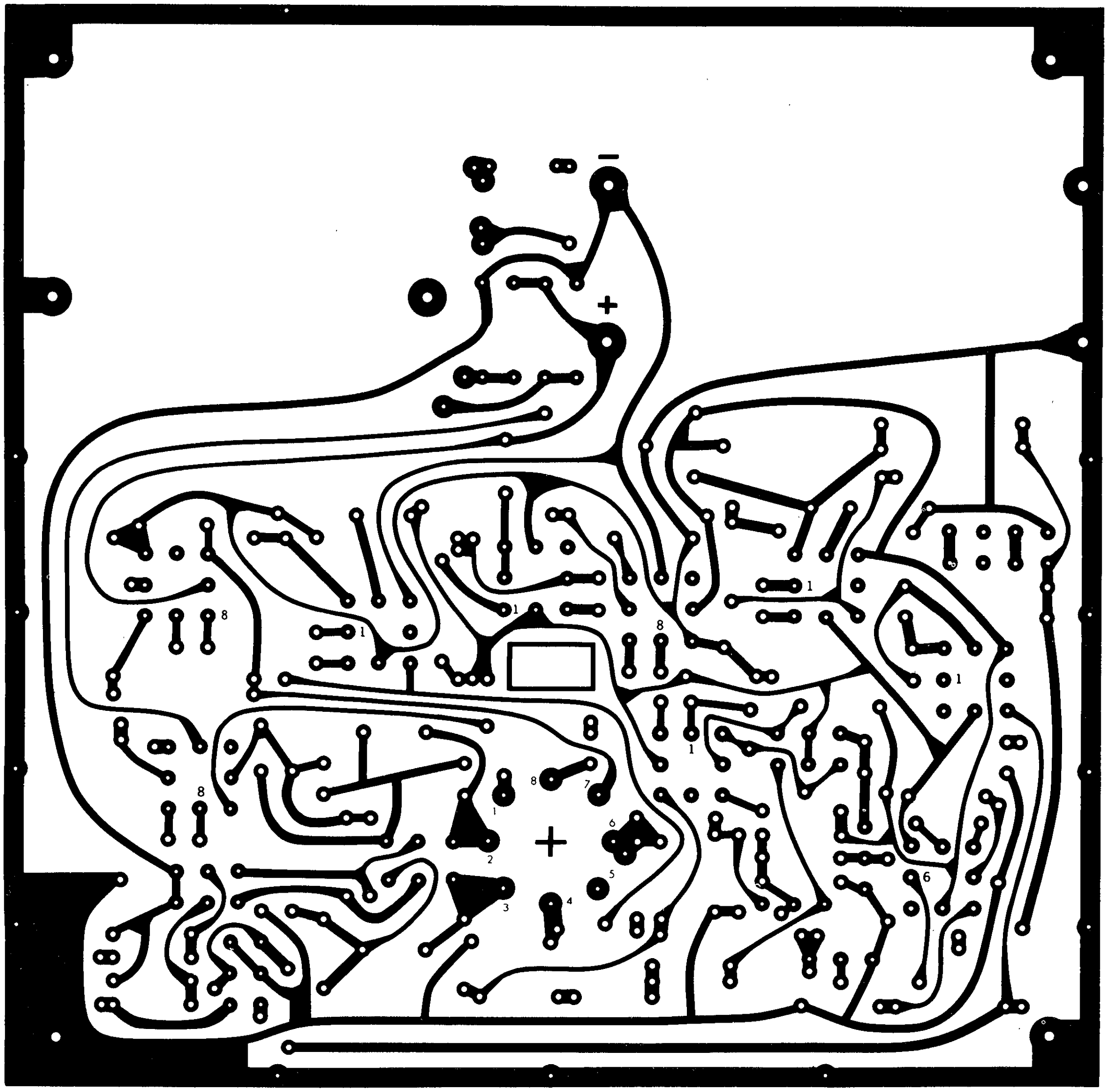


FIGURE 10. Circuit Board Layout

January 1970

HIGH-SPEED MOS COMMUTATORS

Speed and accuracy of MOS analog commutators are being improved sharply by techniques initially developed to make large-scale MOS digital integrated circuits compatible with bipolar logic circuits. Now, TTL logic can drive an MOS commutator at rates up to 20 MHz, with signal accuracies better than 90%. And at lower frequencies, accuracies very close to 100% can be achieved.

In the past, MOS monolithic commutators and multiplexers were recommended for precision analog switching only at relatively low rates, on the order of 10 kHz. Commutation at higher rates was considered risky because of large noise transients produced by the MOS switching transistors. Considerable time had to be allowed for the transients to settle down before the signal could be sampled accurately.

Transient noises have been reduced to at least half their former level by processes that lower the switching-voltage threshold of the MOS transistors. The processes also cut impedance and leakage current, permitting low-impedance designs that further enhance commutator performance.

Although they switch analog voltages, the MOS field-effect transistors in these commutators can be interfaced with logic ICs almost as readily as low-voltage MOS ICs. Either MOS or bipolar logic can control the MOSFET gate voltages. Only a few volts change in the gate voltage will turn the MOSFETs on or off.

Examples of new multichannel designs for analog/digital data-gathering applications are shown in Figures 1 and 2. Circuit impedances have been optimized in each so that commutation rates are much higher than the normal 200 to 500 kHz rate of low-voltage MOS commutators (rates, incidentally, about twice as high as the maximum rates of high-threshold commutators). The all-MOS system in Figure 1 operates at 1 MHz, while the MOS/TTL system in Figure 2 achieves 20 MHz.

LOWERING THRESHOLD VOLTAGES

Reducing the MOSFET switching-threshold voltage, V_{TH}, improves most of the characteristics that affect commutator performance. Chief result is a reduction in the gate-voltage change needed to

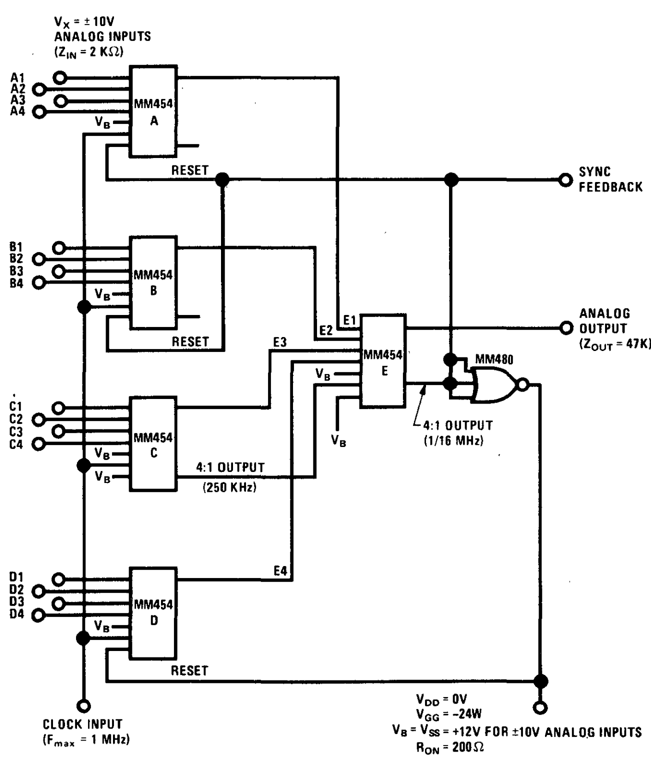


FIGURE 1. All-MOS 1-MHz Multiplexer or Commutator

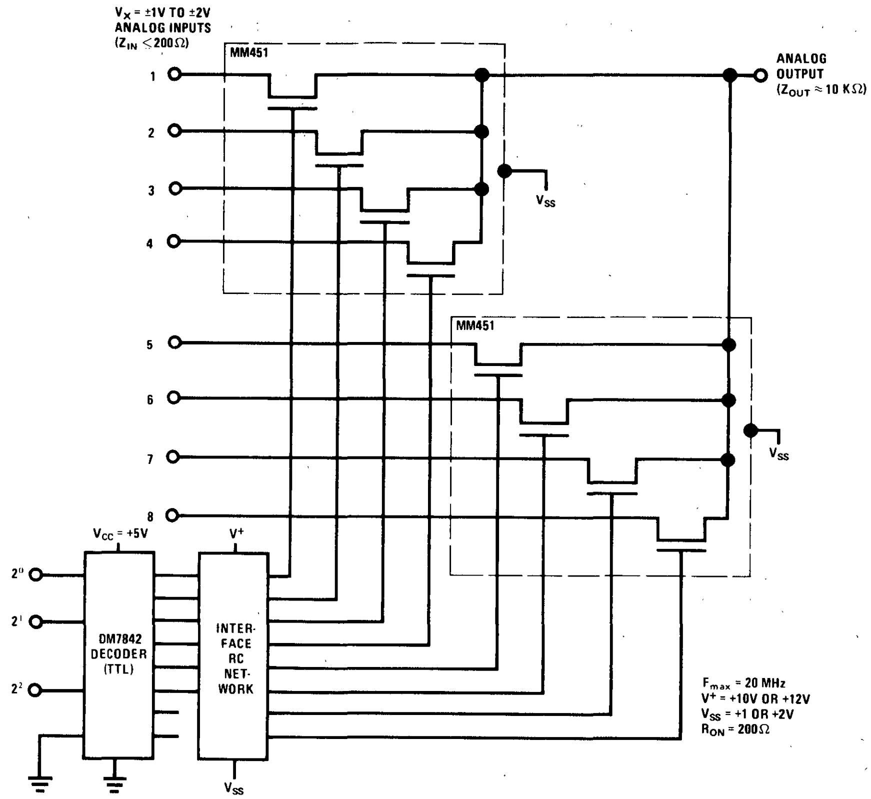


FIGURE 2. Hybrid MOS/TTL 20-MHz Commutator for Low-Level Signals

switch the MOSFET on and off. In turn, switching times and the noise transients and circuit impedances that produce signal errors can all be reduced. The benefits of lowering V_{TH} are additive, particularly in multichannel commutators. The signal may go through several switches in series.

The importance of the threshold voltage is illustrated in Figure 3, which shows schematically the operation of a p-channel enhancement type of MOSFET (the basic element of most MOS integrated circuits). It conducts when the gate voltage is more negative than the potential of the source and the bulk semiconductor substrate V_{SS} by at least V_{TH}. The oxide under the gate electrode acts as the dielectric of a capacitor. The electric field applied to the gate electrode cause holes (absence of electrons) to appear in the channel region starting from the source. The n-type silicon there is converted to p-type, eliminating the p-n diode junctions that had blocked current flow between source and drain (the source is the most positive terminal). V_{TH} is the bias at which the layer of intrinsic semiconductor, with no surplus of electrons or holes, and the p-channel reach the drain diffusion. Conduction begins at this point and increases as V_G goes more negative than V_{TH} (that is, when the gate-to-source voltage $-V_{GS}$ is more than V_{TH}).

The (1-0-0) silicon process described in the appendix produces MOSFETs whose V_{TH} is 1.8 to 2.5 volts when there is no bias between bulk (substrate) and source ($V_{BS} = 0$). In comparison, a conventional MOSFET made with (1-1-1) silicon has a V_{TH} of about 4V. Practical MOS circuits do have some V_{BS} bias and usually some additional signal voltage at the source, which raise the working value of V_{TH}. As the typical V_{TH} curves in Figure 4 show, the threshold of a device rises with V_{BS}.

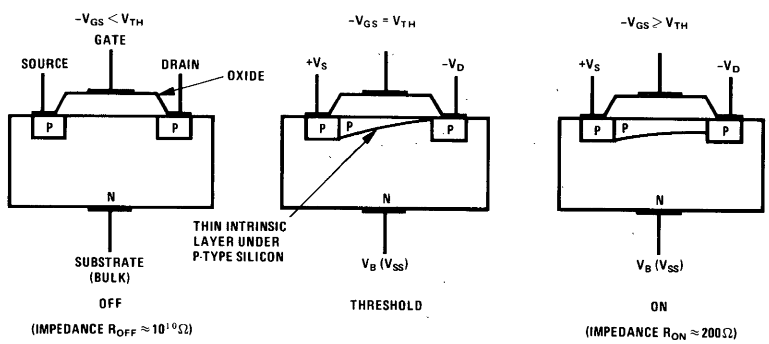


FIGURE 3. Channel Enhancement in MOS Transistors (P Channel)

A general equation describing these relationships is

$$V_{TH} = -K\left[\pm(2\phi_F + V_{BG})\right]^{1/2} + V_{SS}$$

where K is a device constant (usually 0.8 to 1.2) and $\pm 2\phi_F$ is the zero-bias threshold. This equation produces curves such as those in Figure 4.

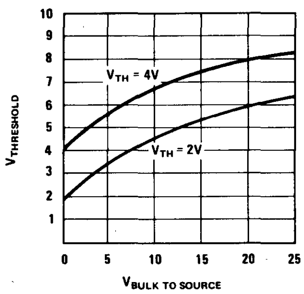


FIGURE 4. Typical Threshold-Voltage Curves

The MOSFET equivalent circuit (Figure 5) offers further insight into the importance of lowering V_{TH}. The smaller change in V_G means that smaller transient voltages will appear at source and drain. The transients are caused by charging and discharging of the capacitances. The time required to change V_G and the duration of the transients will be smaller, too. The value of R_{ON}, the MOSFET's impedance while conducting, will also be less at any given value of V_G more negative than V_{TH}. Any reduction in R_{ON} will make V_{OUT} more nearly equal to V_{IN}. The accuracy of an analog switch is determined by the ratio V_{OUT}/V_{IN}.

CONTROL VOLTAGES

Signal voltage V_X often varies between positive and negative values in commutator applications. To make certain that the MOSFET switches on under all signal conditions, V_G must swing from at least V_X to $(V_{SS}-V_{TH}-\Delta V-VX)$, where $\pm V_X$ are the signal limits and ΔV is the overdrive needed to lower the switch's series resistance to the desired level (mainly, reduction in R_{ON} obtained by making $-V_{GS}$ more negative).

If the signal range is fairly wide, say ±10V, the gate voltage of a MOSFET with a 4V to 6V threshold must swing from +10V to about −26V for accurate commutation. In contrast, a 2V threshold makes the necessary swing only from +10V to about −20V. The difference becomes more significant at lower signal voltages. At $V_X = \pm 1V$, for instance, the high V_{TH} device requires a swing from at least +1V to −10V, while the low V_{TH} device does the job with +1V to −6V – about a third less. High-speed, low-impedance TTL gates can control a commutator in the latter voltage range, as shown in Figure 2, because such small transitions can be made very rapidly. They are close enough to bipolar logic transitions for the use of simple, high-speed TTL-to-MOS interfaces.

Multichannel switches made with (1-0-0) silicon typically operate with a maximum change in control voltage of from +14V to −30V, which permits $V_X = \pm 14V$. Relatively few practical applications require so large a swing. If larger signal voltage must be handled, it would be cheaper to use a scaler than to pay the cost of a high-voltage multiplexer with beefed-up control circuitry.

ON AND OFF RESISTANCES

For best signal accuracy and maximum switching rate, impedances should be low. The resistance of a MOSFET while on, R_{ON}, varies with signal voltage, so it cannot be compensated readily. This produces a variable error term called R_{ON} modulation.

MOS commutators are usually structured as series switches (Figure 6a). Two or more ranks of commutators are generally used, as in Figure 1, to minimize the control circuitry. The added ranks put additional MOSFETs in each signal channel and enlarge the amount and variation in R_{ON} of the conducting channel. If V_X varies, the error ratio V_{OUT}/V_{IN} tends to vary because R_{ON} is a function of the effective switching threshold which rises and falls with V_X.

There is no simple way of keeping R_{ON} constant. Usually, the effect of the variation is reduced by increasing the other impedances, but that lowers the maximum switching rate. A low-V_{TH} eases this problem greatly. All other conditions being equal, the MOSFET with the lowest V_{TH} will conduct better at any given value of V_G more negative than V_{TH}. The p-channel enhancement will be greater

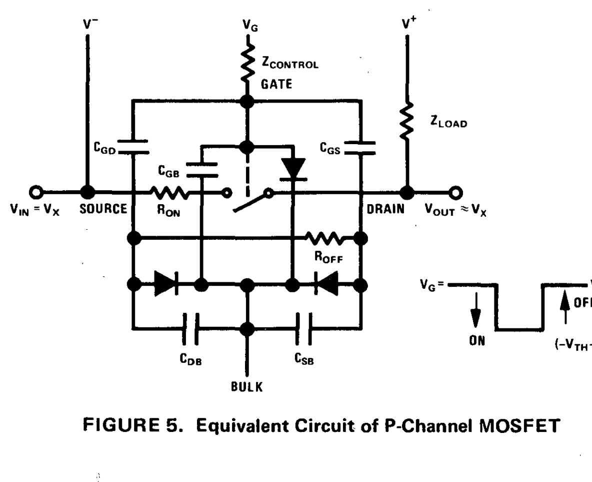


FIGURE 5. Equivalent Circuit of P-Channel MOSFET

and the channel electrically larger. Figure 6c is a typical curve of R_{ON} versus gate bias. Low-V_{TH} analog switches made with (1-0-0) silicon by National Semiconductor as integrated circuits achieve R_{ON} values comparable to those of larger, but higher-V_{TH}, discrete MOSFETs--from 250 to 300 ohms at $V_X = -10V$ and about 100 ohms when $V_X = +10V$. The R_{ON} of a high-V_{TH} integrated commutator, in contrast, is typically a few hundred ohms higher and some reportedly reach a few kilohms.

To swamp out the voltage-divider effect in Figure 6b, it has been customary to make the load, R_L, much larger than the combination of R_{ON} and R_S. Output impedances in the megohm range are often used with high-V_{TH} devices. But note in Figure 2 that very low values of source and load impedance can be used with low-V_{TH} commutators. These low impedances and the very low impedance of the TTL circuit controlling the gate are two of the main reasons for this commutator's exceptionally high speed.

Source impedance is usually made equal or less than R_{ON} so that leakage currents of the turned-off MOSFETs can return to a low-impedance turned-on channel signal source. Leakage per switch is small in an integrated circuit commutator, but there are several switching devices with a common output in the same semiconductor substrate. Leakage currents could add up to a value that seriously degrades signal accuracy. In any semiconductor device, leakage increases rapidly with temperature. However, the leakage specification is so small in our commutator made with (1-0-0) silicon that they will work well up to a temperature of 125°C, while commutators made with (1-1-1) silicon have been specified for a maximum operating temperature of only 85°C.

Regardless of the process, the OFF resistance, R_{OFF}, of a well-made MOSFET is generally high enough to prevent the signal in the OFF channel (channel V_Y in Figure 6a) from appearing at the output and degrading the accuracy of the signal through the on channel (V_X in the figure). R_{OFF} is usually around 10^{10} ohms. If V_Y is a high-frequency signal, there may be significant AC feedthrough, but this can be prevented by techniques to be discussed shortly.

SWITCHING SPEED AND NOISE

The absolute switching speed of a commutator is limited by the time required to charge and discharge the device capacitances. Circuit impedances affect speed by contributing to the RC time constants. However, the practical switching rate of a precision commutator depends upon the time required for the output signal to recover from the noise transients produced during the charge-discharge cycles. Low-V_{TH} processing cuts transient recovery time because the transients' duration and amplitude are reduced. Some designs make the recovery time negligible.

In all MOSFETs, transmission of a turn-on or turn-off signal is followed by a delay whose length depends upon the magnitude and rate of change of the gate-control voltage. At turn-on, the delay is lengthened by the RC time constant of the gate-bulk capacitance (see Figure 5) and the impedance in the control circuit. Capacitances and impedances in the signal path cause a similar delay at turn-off. As V_{GS} goes negative, turning the switch on, energy is pulled from the source and load impedances through the gate-source and gate-drain capacitances, as in the simplified equivalent circuit of Figure 7a. At turn-off, V_{GS} goes to zero volts or positive, and energy is pushed out through the same paths.

Thus, negative turn-on and positive turn-off transients appear at the summing node. The transient waveforms of low V_{TH} and high V_{TH} MOSFETs are shown simplified and superimposed in Figure 7b. The levels are typical for devices with V_{TH} = 2V and V_{TH} = 4V at $V_X = \pm 1V$. The larger gate voltages used at higher signal voltages would make durations and amplitudes proportionately larger

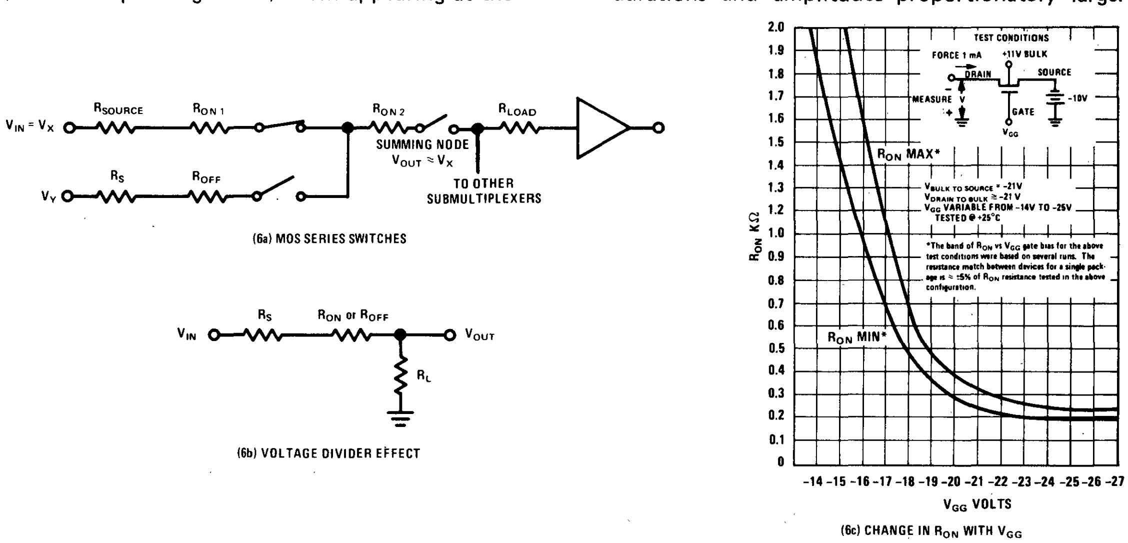
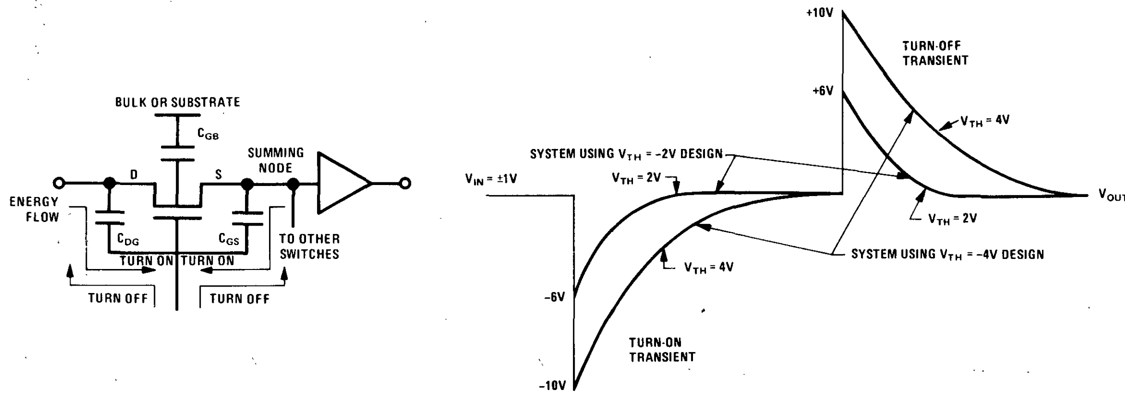


FIGURE 6. MOS Commutator Switching Impedances



(7a) EQUIVALENT CIRCUIT

(7b) TRANSIENT NOISE VOLTAGE

FIGURE 7. Transient Noise Generation

(another reason why the Figure 2 circuit is faster than the Figure 1 circuit).

The transients can be much larger than signal voltages, so even the relatively small transients of a low-V_{TH} MOSFET can saturate the buffer amplifier. One of the ways that designers of discrete commutators minimized transients at the summing node was to drive adjacent channels with coincident turn-on and turn-off signals. In this way, negative-going transients from the channels turning on will partially cancel out positive-going transients from the channels turning off. When the output amplifier is an integrator, the amounts of energy pulled through the summing node will be minimized by, in effect, being averaged out.

Coincident drive, discrete component circuits are fairly complex and expensive. Essentially the same effect is obtained in the Figure 2 commutator, at much less cost. The TTL decoder selects channels at such a high rate of speed that a channel is turning on while another channel is turning off. Transitions of the control voltage occur in less time than the turn-on and turn-off delays of the MOSFETs. So the transients are suppressed in a matter of nanoseconds. In fact, when the gate voltage is going negative or positive simultaneously, the transient is practically invisible at the output. That is, the transient actually helps change the output signal to the correct level more rapidly.

You might say that the high commutation rate makes the high commutation rate possible, but it is more pertinent to stress that the TTL decoder could not directly control a high-V_{TH} commutator. Low-impedance drivers are essential for high commutation rates, because they quickly source and sink transients. In this respect, TTL integrated circuits make almost ideal drivers.

In principle, the gate turning on and the gate turning off in a multichannel IC commutator are part of a closed-loop circuit charging the gate capacitance. The noise energy that does get into the summing node should be dissipated quickly to improve the data channel's recovery time. The energy is dissipated in the parallel combination of the summing node resistance and channel-source impedance. The RC time constant of the equivalent circuit in Figure 8 should be optimized to obtain the maximum commutation frequency.

$$F_{max} = [(R_S/R_{node})\, C_{node}]\, [(C_1 + C_2)/2C_{node}]\, [V_{G1} - V_{G0}] \text{ to } 1$$

This equation relates the time constants, gate and transient voltages and transient recovery tolerance. V_{G1} and V_{G0} are the turn-on and turn-off values of V_G; other terms are defined in Figure 8.

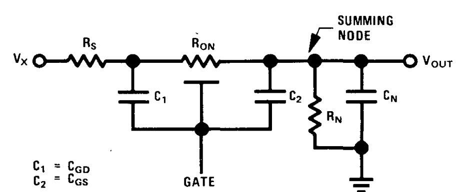


FIGURE 8. RC Network Governing Switching Frequency

HIGH-FREQUENCY NOISE CONTROL

In some cases, the analog input signal is AC rather than DC. That is, it may fluctuate rapidly between positive and negative values. This can vary the effective values of V_{SG}, R_{ON} and perhaps R_{OFF}, and may also cause spurious charging or discharging of the MOSFET capacitance. The condition results in output-voltage fluctuations due to the appearance at the summing node of signal voltages from a channel that is supposed to be off—a problem known as AC feedthrough or channel-feedthrough noise. The main cause is charge transfer through the gate-source and gate-drain capacitances of the turned-off MOSFETs.

Fortunately, most transducer voltage outputs are below 10 kHz in frequency and simply using a low-impedance gate driver prevents the problem. The transients sink into the driver rather than go to the output. A high signal source impedance would make this technique more effective, but would also cause larger transients in the turned-on channel, imposing longer recovery times and slower commutation rates.

There is a simple detour around this impasse, too. The dynamic impedance of the gate driver is allowed to approach a zero-ohm impedance when the channel is turned off (Figure 9). Theoretically, this will prevent any channel feedthrough noise at signal frequencies up to 2 MHz. In practical circuits, signal frequency is limited by load impedance, but can usually be pushed above 1 MHz. The driver impedance itself must also be low at high frequencies, of course.

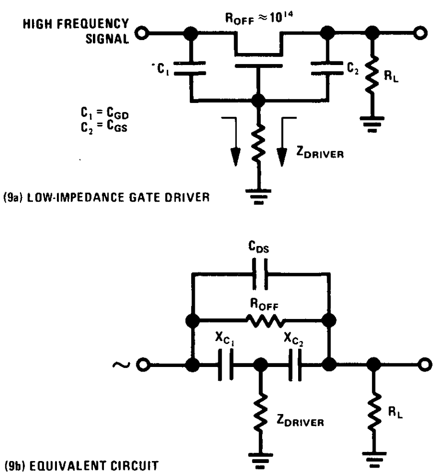


FIGURE 9. Zero-Impedance Driver Return Prevents AC Feedthrough

HIGH-SPEED SYSTEMS

All of these factors have been optimized in the Figure 2 system. At 20 MHz, its accuracy with $V_X = \pm 1V$ is nearly as good as 99%. Source and load impedance are made very low because R_{ON} is not greater than about 200 ohms per channel. The gate change is only 8V (from +2V to −6V), and the high-speed TTL control makes the transients coincide.

The 8-channel configuration shown can be the building block of very large solid-state commutators. Each 4-channel MOSFET switch is a monolithic chip (National Semiconductor MM451). The TTL channel selector is a decoder (DM7842) designed to convert 4-bit binary-coded-decimal inputs into decimal-number outputs. Only 8 outputs are needed here, so the decoder's fourth input is grounded.

The TTL outputs are translated to MOS control signals with an interface network consisting of identical passive circuits on each control line. An interface and its voltage levels are shown in Figure 10. The author used discrete components, but all 16 resistors in the network could be made as a thick-film printed circuit because the values are not large and the tolerances are not critical.

TTL logic outputs are positive, while MOSFETs require negative or positive gate biases to turn on or off. The necessary voltage changes are made with the capacitor in Figure 10.

Assume first that the TTL output is at a logic "1". R1 will pull the decoder output up to $V^+ = +10V$. With $V_{SS} = +2V$, there will be +8V across the capacitor, V_G will be equal to V_{SS}, and that channel will be held off.

When the TTL output switches from a logic "1" to a logic "0" level, the decoder output will go from $V^+ = 10V$ to about 0.4V. Bias on the gate will therefore drop from +2V to about −6V, turning the channel on. The commutator is controlled, then, by selecting the location of an "0" bit in the decoder output and making all other outputs "1".

R1 is connected to a voltage higher than +6V to assure that the TTL output rises rapidly during a transition from logic "0" to logic "1". This is needed for quick, clean turnoff of a channel (a similar technique of interfacing TTL and low-V_{TH} MOS digital circuits enables the MOS circuits to operate at about twice the normal MOS rate). The opposite transition, to the more negative level, is normally quite fast and is assisted by the excellent current-sinking capability of TTL.

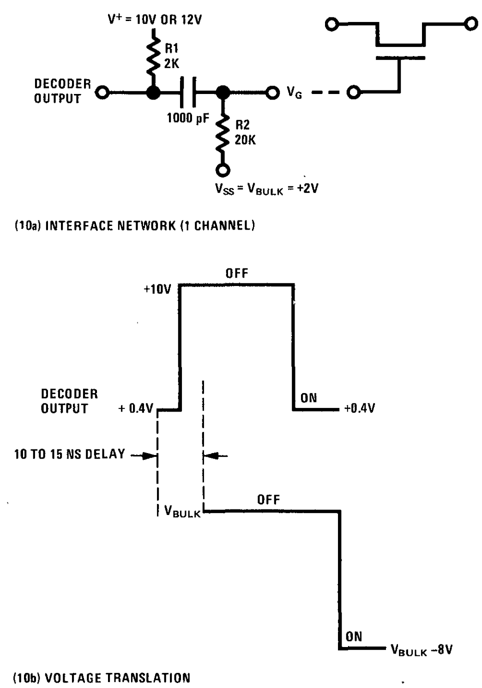


FIGURE 10. High-Speed TTL-to-MOS Control Interface

Care must be taken to select TTL drivers that do not break down when their outputs are pulled up to +10V or +12V. The DM7842 has a diode in the output stage that protects the output transistor at high voltages, and other devices in the National TTL family have similar output stages. These are equivalent to Series 54 TTL. Suitable TTL control logic can be assembled from other ICs, but the DM7842 is convenient because only one driver chip is needed for every eight channels in the commutator system.

There is a delay of 10 to 15 nanoseconds between a transition in the TTL output and the switching of a channel on or off, mainly due to the RC time constant of the RC interface. However, the delay occurs equally on all channels and does not affect the commutation rate or significantly reduce the 50 ns sampling time permitted by a 20 MHz rate. Commutator output can be kept synchronized to any following data processing subsystem by putting a comparable delay in the line from the system clock to the processor.

The MM451 chip is also available with a DTL monolithic driver in a flatpack. This hybrid IC, the MH453, does not require an external interface network. It will operate at frequencies to 500 kHz and switch analog signals of ±10V under direct control of TTL or DTL logic. The four MOSFETs of the MM451 are connected in a dual differential configuration, useful for combining and comparing signal voltages.

ALL-MOS COMMUTATORS

Commutators built entirely of MOS devices need not be limited to low-frequency operation, despite their larger voltage swings and transients. The system in Figure 2 has better than 99% accuracy at 1 MHz with $V_X = \pm 10V$ when the previously discussed characteristics of low-V_{TH} devices in this signal range are optimized.

Similar systems, optimized for smaller signal-voltage ranges, have not been built by the author but it is reasonable to expect higher frequencies or accuracies in such systems. Accuracy, of course, would be further improved by operating the optimized designs at lower than their maximum frequency. Longer recovery times would be permitted.

Each of the MM454 4-channel commutators contains four MOSFETs like those in the MM451 and, in the same chip, a 2-bit MOS counter and decoder for channel selection and all-channel blanking (Figure 11).

As shown, the system samples the 16 channels sequentially, much like a rotary driven mechanical commutator. The MM454 is designed as a building block for large sequential sampling systems. However, any particular channel could be selected with external output-gating logic. If random channel selection were the normal operating mode, the MM451 and external selection logic can be used. Two ranks of commutators, similar to Figure 1, simplify the control logic. For example, one gate driver would turn on channels A1, B1, C1 and D1, and a second driver would select channel A1 by turning on channel E1—which takes a lot less control circuitry than selecting 1 out of 16 channels directly and requires only one more monolithic commutator.

Either way, a very critical system design requirement is to guarantee that only the selected channel conducts during the sampling interval. The single 3-input NOR gate in Figure 1 accomplishes that. Commutator C is used as the master element. It divides down the 1 MHz clock signal through a 4:1 countdown circuit, which is provided in the MM454 to facilitate submultiplexing. Commutator E's four channels therefore sequence at a 250 kHz rate. Meanwhile, the four channels in commutators A, B, C and D are each sequencing at 1 MHz. The analog sequences through A1, A2, A3 and A4 in order when E1 is on, B1 through B4 when E2 is on, and so forth.

The 4:1 count-down output of commutator E (1/16 MHz) is fed back through the NOR gate to the reset inputs of commutators A, B and D. The reset every cycle keeps them in step with commu-

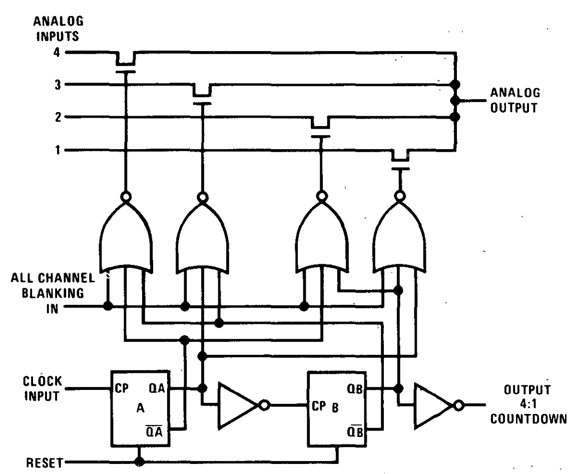


FIGURE 11. MM454 Four-Channel MOS Submultiplexer

tator C and therefore commutator E. The NOR gate's output also can be used to maintain synchronization of the commutator with other signal processing systems.

ANALOG/DIGITAL SYSTEMS

Techniques developed, and being developed, to directly couple bipolar and large-scale MOS digital circuits also depend heavily upon the lowering of threshold voltages. A report compiling and detailing coupling techniques is in preparation. In general, the ability of the MOS digital circuit to accept small, positive transitions in signal voltage, and to operate with smaller differentials in bias and gate voltages are the critical requirements for direct coupling.

Directly coupling MOS digital outputs to bipolar logic also enhances operating speed, again because impedances are lowered. Some of the high-speed TTL/MOS hybrid systems that have been developed are similar in principle to commutators, except that V_X is digital data and scores of MOSFET switching stages are used in each MOS chip. One data-storage system built by the author has achieved data transfer rates up to 16 MHz, by multiplexing high-speed bipolar data into parallel MOS storage circuits.

With all three classes of bipolar/MOS interfaces—analog/digital, logic/logic and logic/analog—now available, system designs can exploit more fully the many speed/cost tradeoffs offered by hybrid bipolar/MOS systems. Bipolar control logic and MOS large-scale storage is an extremely efficient, minimum cost combination suitable for medium-to-high-speed systems.

In other words, low-threshold processing has enabled MOS to move out of the low-frequency range and into the ranges where most modern analog/digital systems operate.

December 1969

IC OP AMP BEATS FETs ON INPUT CURRENT

ABSTRACT

A monolithic operational amplifier having input error currents in the order of 100 pA over a −55°C to 125°C temperature range is described. Instead of FETs, the circuit uses bipolar transistors with current gains of 5000 so that offset voltage and drift are not degraded. A power consumption of 1 mW at low voltage is also featured.

A number of novel circuits that make use of the low current characteristics of the amplifier are given. Further, special design techniques required to take advantage of these low currents are explored. Component selection and the treatment of printed circuit boards is also covered.

INTRODUCTION

A year ago, one of the loudest complaints heard about IC op amps was that their input currents were too high. This is no longer the case. Today ICs can provide the ultimate in performance for many applications—even surpassing FET amplifiers.

FET input stages have long been considered the best way to get low input currents in an op amp. Low-picoamp input currents can in fact be obtained at room temperature. However, this current, which is the leakage current of the gate junction, doubles every 10°C, so performance is severely degraded at high temperatures. Another disadvantage is that it is difficult to match FETs closely.[1] Unless expensive selection and trimming techniques are used, typical offset voltages of 50 mV and drifts of 50 μV/°C must be tolerated.

Super gain transistors[2] are now challenging FETs. These devices are standard bipolar transistors which have been diffused for extremely high current gains. Typically, current gains of 5000 can be obtained at 1 μA collector currents. This makes it possible to get input currents which are competitive with FETs. It is also possible to operate these transistors at zero collector base voltage, eliminating the leakage currents that plague the FET. Hence they can provide lower error currents at elevated temperatures. As a bonus, super gain transistors match much better than FETs with typical offset voltages of 1 mV and drifts of 3 μV/°C.

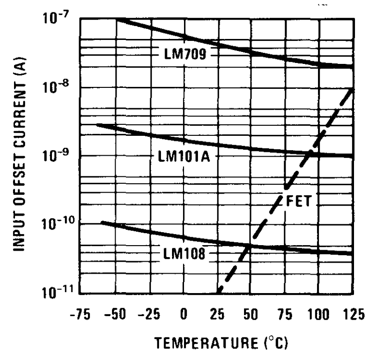


FIGURE 1. Comparing IC Op Amps With FET-Input Amplifier

Figure 1 compares the typical input offset currents of IC op amps and FET amplifiers. Although FETs give superior performance at room temperature, their advantage is rapidly lost as temperature increases. Still, they are clearly better than early IC amplifiers like the LM709.[3] Improved devices, like the LM101A,[4] equal FET performance over a −55°C to 125°C temperature range. Yet they use standard transistors in the input stage. Super gain transistors can provide more than an order of magnitude improvement over the LM101A. The LM108 uses these to equal FET performance over a 0°C to 70°C temperature range.

In applications involving 125°C operation, the LM108 is about two orders of magnitude better than FETs. In fact, unless special precautions are taken, overall circuit performance is often limited by leakages in capacitors, diodes, analog switches or printed circuit boards, rather than by the op amp itself.

EFFECTS OF ERROR CURRENT

In an operational amplifier, the input current produces a voltage drop across the source resis-

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tance, causing a dc error. This effect can be minimized by operating the amplifier with equal resistances on the two inputs.[5] The error is then proportional to the difference in the two input currents, or the offset current. Since the current gains of monolithic transistors tend to match well, the offset current is typically a factor of ten less than the input currents.

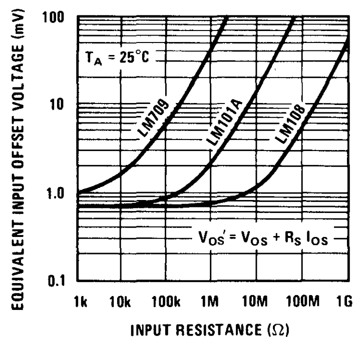


FIGURE 2. Illustrating The Effect Of Source Resistance On Typical Input Error Voltage

Naturally, error current has the greatest effect in high impedance circuitry. Figure 2 illustrates this point. The offset voltage of the LM709 is degraded significantly with source resistances greater than 10 kΩ. With the LM101A this is extended to source resistances high as 500 kΩ. The LM108, on the other hand, works well with source resistances above 10 MΩ.

High source resistances have an even greater effect on the drift of an amplifier, as shown in Figure 3. The performance of the LM709 is worsened with sources greater than 3 kΩ. The LM101A holds out to 100 kΩ sources, while the LM108 still works well at 3 MΩ.

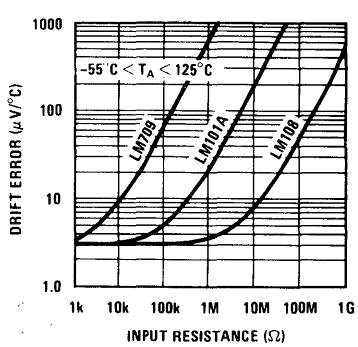


FIGURE 3. Degradation Of Typical Drift Characteristics With High Source Resistances

It is difficult to include FET amplifiers in Figure 3 because their drift is initially 50 μV/°C, unless they are selected and trimmed. Even though their drift may be well controlled (5 μV/°C) over a limited temperature range, trimmed amplifiers generally exhibit a much higher drift over a −55°C to 125°C temperature range. At any rate, their average drift rate would, at best, be like that of the LM101A where 125°C operation is involved.

Applications that require low error currents include amplifiers for photodiodes or capacitive transducers, as these usually operate at megohm impedance levels. Sample-and-hold circuits, timers, integrators and analog memories also benefit from low error currents. For example, with the LM709, worst case drift rates for these kinds of circuits is in the order of 1.5V/sec. The LM108 improves this to 3 mV/sec.—worst case over a −55°C to 125°C temperature range. Low input currents are also helpful in oscillators and active filters to get low frequency operation with reasonable capacitor values. The LM108 can be used at a frequency of 1 Hz with capacitors no larger than 0.01 μF. In logarithmic amplifiers, the dynamic range can be extended by nearly 60 dB by going from the LM709 to the LM108. In other applications, having low error currents often permits an entirely different design approach which can greatly simplify circuitry.

THE LM108

Figure 4 shows a simplified schematic of the LM108. Two kinds of NPN transistors are used on the IC chip: super gain (primary) transistors which have a current gain of 5000 with a breakdown voltage of 4V and conventional (secondary) transistors which have a current gain of 200 with an 80V breakdown. These are differentiated on the schematic by drawing the secondaries with a wider base.

Primary transistors (Q_1 and Q_2) are used for the input stage; and they are operated in a cascode connection with Q_5 and Q_6. The bases of Q_5 and Q_6 are bootstrapped to the emitters of Q_1 and Q_2 through Q_3 and Q_4, so that the input transistors are operated at zero collector-base voltage. Hence, circuit performance is not impaired by the low breakdown of the primaries, as the secondary transistors stand off the common mode voltage. This configuration also improves the common mode rejection since the input transistors do not see variations in the common mode voltage. Further, because there is no voltage across their collector-base junctions, leakage currents in the input transistors are effectively eliminated.

The second stage is a differential amplifier using high gain lateral PNPs (Q_9 and Q_{10}).[6] These devices have current gains of 150 and a breakdown voltage of 80V. R_1 and R_2 are the collector load resistors for the input stage. Q_7 and Q_8 are diode connected laterals which compensate for the

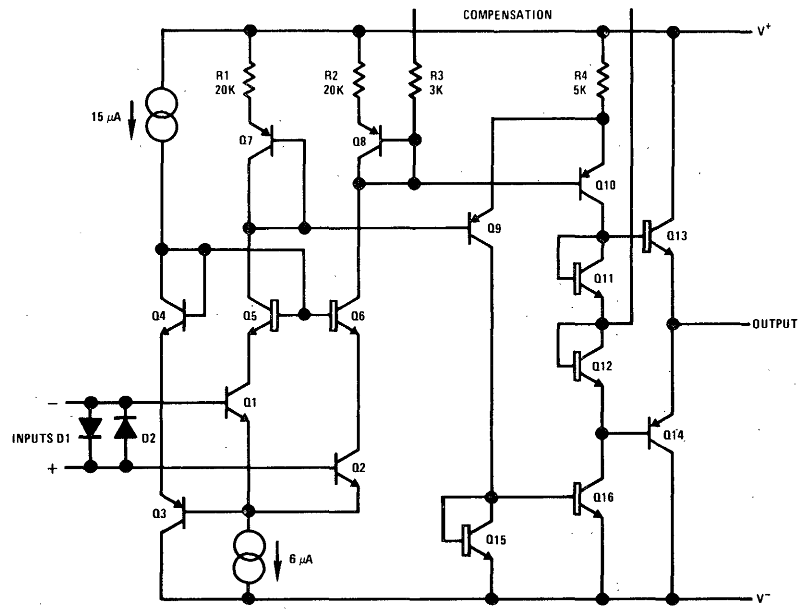


FIGURE 4. Simplified Schematic Of The LM108

emitter-base voltage of the second stage so that its operating current is set at twice that of the input stage by R_4.

The second stage uses an active collector load (Q_{15} and Q_{16}) to obtain high gain. It drives a complementary class-B output stage which gives a substantial load driving capability. The dead zone of the output stage is eliminated by biasing it on the verge of conduction with Q_{11} and Q_{12}.

Two methods of frequency compensation are available for the amplifier. In one a 30 pF capacitor is connected from the input to the output of the second stage (between the compensation terminals). This method is pin-compatible with the LM101 or LM101A. It can also be compensated by connecting a 100 pF capacitor from the output of the second stage to ground. This technique has the advantage of improving the high frequency power supply rejection by a factor of ten.

A complete schematic of the LM108 is given in the Appendix along with a description of the circuit. This includes such essential features as overload protection for the inputs and output.

PERFORMANCE

The primary design objective for the LM108 was to obtain very low input currents without sacrificing offset voltage or drift. A secondary objective was to reduce the power consumption. Speed was of little concern, as long as it was comparable with the LM709. This is logical as it is quite difficult to make high-impedance circuits fast; and low power circuits are very resistant to being made fast. In other respects, it was desirable to make the LM108 as much like the LM101A as possible.

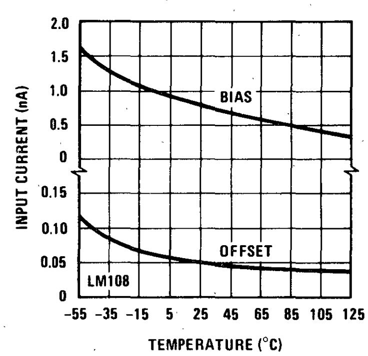


FIGURE 5. Input Currents

Figure 5 shows the input current characteristics of the LM108 over a −55°C to 125°C temperature range. Not only are the input currents low, but also they do not change radically over temperature. Hence, the device lends itself to relatively simple temperature compensation schemes, that will be described later.

There has been considerable discussion about using Darlington input stages rather than super gain transistors to obtain low input currents.[6,7] It is appropriate to make a few comments about that here.

Darlington inputs can give about the same input bias currents as super gain transistors—at room temperature. However, the bias current varies as the square of the transistor current gain. At low temperatures, super gain devices have a decided advantage. Additionally, the offset current of super gain transistors is considerably lower than Darlingtons, when measured as a percentage of bias current. Further, the offset voltage and offset voltage drift of Darlington transistors is both higher and more unpredictable.

Experience seems to tell the real truth about Darlingtons. Quite a few op amps with Darlington input stages have been introduced. However, none have become industry standards. The reason is that they are more sensitive to variations in the manufacturing process. Therefore, satisfactory performance specifications can only be obtained by sacrificing the manufacturing yield.

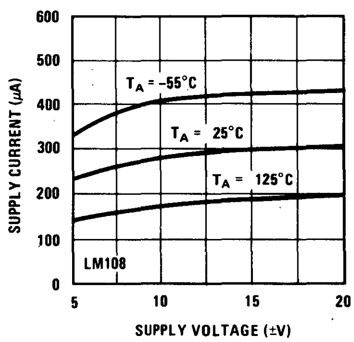


FIGURE 6. Supply Current

The supply current of the LM108 is plotted as a function of supply voltage in Figure 6. The operating current is about an order of magnitude lower than devices like the LM709. Furthermore, it does not vary radically with supply voltage which means that the device performance is maintained at low voltages and power consumption is held down at high voltages.

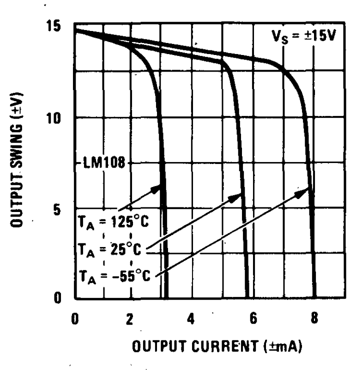


FIGURE 7. Output Swing

The output drive capability of the circuit is illustrated in Figure 7. The output swings to within a volt of the supplies, which is especially important when operating at low voltages. The output falls off rapidly as the current increases above a certain level and the short circuit protection goes into effect. The useful output drive is limited to about ±2 mA. It could have been increased by the addition of Darlington transistors on the output, but this would have restricted the voltage swing at low supply voltages. The amplifier, incidentally, works with common mode signals to within a volt of the supplies so it can be used with supply voltages as low as ±2V.

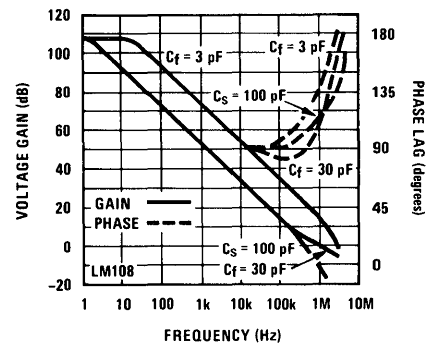


FIGURE 8. Open Loop Frequency Response

The open loop frequency response, plotted in Figure 8, indicates that the frequency response is about the same as that of the LM709 or the LM101A. Curves are given for the two compensa-

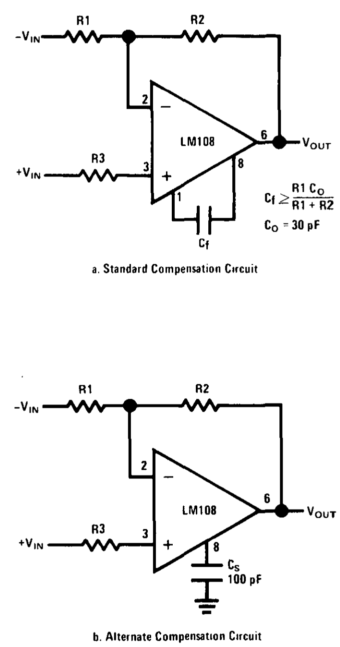


FIGURE 9. Compensation Circuits

tion circuits shown in Figure 9. The standard compensation is identical to that of the LM101 or LM101A. The alternate compensation scheme gives much better rejection of high frequency power supply noise, as will be shown later.

With unity gain compensation, both methods give a 75-degree stability margin. However, the shunt compensation has a 300 kHz small signal bandwidth as opposed to 1 MHz for the other scheme. Because the compensation capacitor is not included on the IC chip, it can be tailored to fit the application. When the amplifier is used only at low frequencies, the compensation capacitor can be increased to give a greater stability margin. This makes the circuit less sensitive to capacitive loading, stray capacitances or improper supply bypassing. Overcompensation also reduces the high frequency noise output of the amplifier.

With closed-loop gains greater than one, the high frequency performance can be optimized by making the compensation capacitor smaller. If unity-gain compensation is used for an amplifier with a gain of ten, the gain error will exceed 1-percent at frequencies above 400 Hz. This can be extended to 4 kHz by reducing the compensation capacitor to 3 pF. The formula for determining the minimum capacitor value is given in Figure 9a. It should be noted that the capacitor value does not really depend on the closed-loop gain. Instead, it depends on the high frequency attenuation in the feedback networks and, therefore, the values of R_1 and R_2. When it is desirable to optimize performance at high frequencies, the standard compensation should be used. With small capacitor values, the stability margin obtained with shunt compensation is inadequate for conservative designs.

The frequency response of an operational amplifier is considerably different for large output signals than it is for small signals. This is indicated in Figure 10. With unity-gain compensation, the small signal bandwidth of the LM108 is 1 MHz. Yet full output swing cannot be obtained above 2 kHz. This corresponds to a slew rate of 0.3V/µs. Both the full-output bandwidth and the slew rate can be increased by using smaller compensation capacitors, as is indicated in the figure. However, this is only applicable for higher closed loop gains. The results plotted in Figure 10 are for standard compensations. With unity gain compensation, the same curves are obtained for the shunt compensation scheme.

Classical op amp theory establishes output resistance as an important design parameter. This is not true for IC op amps: The output resistance of most devices is low enough that it can be ignored, because they use class-B output stages. At low frequencies, thermal feedback between the output

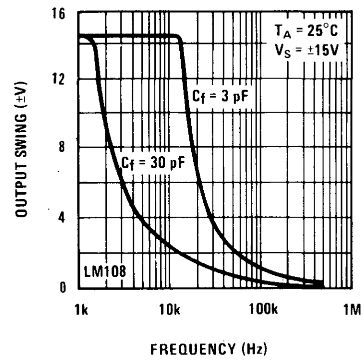


FIGURE 10. Large Signal Frequency Response

and input stages determines the effective output resistance, and this cannot be accounted for by conventional design theories. Semiconductor manufacturers take care of this by specifying the gain under full load conditions, which combines output resistance with gain as far as it affects overall circuit performance. This avoids the fictitious problem that can be created by an amplifier with infinite gain, which is good, that will cause the open loop output resistance to appear infinite, which is bad, although none of this affects overall performance significantly.

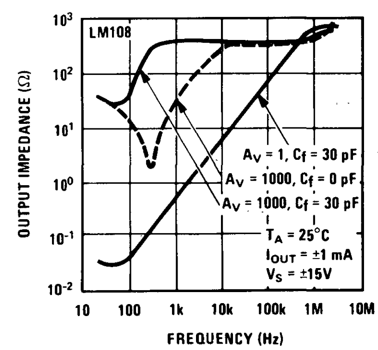


FIGURE 11. Closed Loop Output Impedance

The *closed loop* output impedance is, nonetheless, important in some applications. This is plotted for several operating conditions in Figure 11. It can be seen that the output impedance rises to about 500Ω at high frequencies. The increase occurs because the compensation capacitor rolls off the open loop gain. The output resistance can be reduced at the intermediate frequencies, for closed loop gains greater than one, by making the capacitor smaller. This is made apparent in the figure by comparing the output resistance with and without frequency compensation for a closed loop gain of 1000.

The output resistance also tends to increase at low frequencies. Thermal feedback is responsible for this phenomenon. The data for Figure 11 was taken under large-signal conditions with ±15V supplies, the output at zero and a ±1 mA current swing. Hence, the thermal feedback is accentuated more than would be the case for most applications.

In an op amp, it is desirable that performance be unaffected by variations in supply voltage. IC amplifiers are generally better than discretes in this respect because it is necessary for one single design to cover a wide range of uses. The LM108 has a power supply rejection which is typically in excess of 100 dB, and it will operate with supply voltages from ±2V to ±20V. Therefore, well-regulated supplies are unnecessary, for most applications, because a 20-percent variation has little effect on performance.

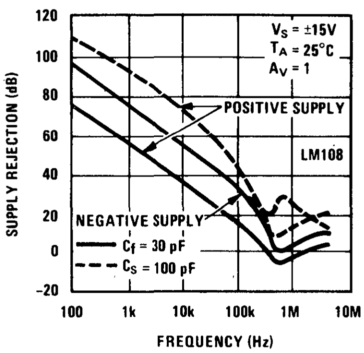


FIGURE 12. Power Supply Rejection

The story is different for high-frequency noise on the supplies, as is evident from Figure 12. Above 1 MHz, practically all the noise is fed through to the output. The figure also demonstrates that shunt compensation is about ten times better at rejecting high frequency noise than is standard compensation. This difference is even more pronounced with larger capacitor values. The shunt compensation has the added advantage that it makes the circuit virtually unaffected by the lack of supply bypassing.

Power supply rejection is defined as the ratio of the change in offset voltage to the change in the supply voltage producing it. Using this definition, the rejection at low frequencies is unaffected by the closed loop gain. However, at high frequencies, the opposite is true. The high frequency rejection is increased by the closed loop gain. Hence, an amplifier with a gain of ten will have an order of magnitude better rejection than that shown in Figure 12 in the vicinity of 100 kHz to 1 MHz.

The overall performance of the LM108 is summarized in Table 1*. It is apparent from the table and the previous discussion that the device is ideally suited for applications that require low input currents or reduced power consumption. The speed of the amplifier is not spectacular, but this is not usually a problem in high-impedance circuitry. Further, the reduced high frequency performance makes the amplifier easier to use in that less attention need be paid to capacitive loading, stray capacitances and supply bypassing.

APPLICATIONS

Because of its low input current, the LM108 opens up many new design possibilities. However, extra care must be taken in component selection and the assembly of printed circuit boards to take full advantage of its performance. Further, unusual design techniques must often be applied to get around the limitations of some components.

SAMPLE AND HOLD CIRCUITS

The holding accuracy of a sample and hold is directly related to the error currents in the components used. Therefore, it is a good circuit to start off with in explaining the problems in-

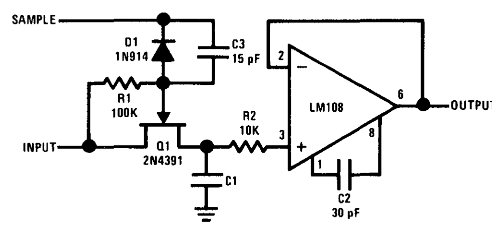


FIGURE 13. Sample And Hold Circuit

volved. Figure 13 shows one configuration for a sample and hold. During the sample interval, Q_1 is turned on, charging the hold capacitor, C_1, up to the value of the input signal. When Q_1 is turned off, C_1 retains this voltage. The output is obtained from an op amp that buffers the capacitor so that it is not discharged by any loading. In the holding mode, an error is generated as the capacitor looses charge to supply circuit leakages. The accumulation rate for error is given by

$$\frac{dV}{dt} = \frac{I_E}{C_1},$$

where dV/dt is the time rate of change in output voltage and I_E is the sum of the input current to the op amp, the leakage current of the holding capacitor, board leakages and the "off" current of the FET switch.

*See Appendix, page 19.

When high-temperature operation is involved, the FET leakage can limit circuit performance. This can be minimized by using a junction FET, as indicated, because commercial junction FETs have lower leakage than their MOS counterparts. However, at 125°C even junction devices are a problem. Mechanical switches, such as reed relays, are quite satisfactory from the standpoint of leakage. However, they are often undesirable because they are sensitive to vibration, they are too slow or they require excessive drive power. If this is the case, the circuit in Figure 14 can be used to eliminate the FET leakage.

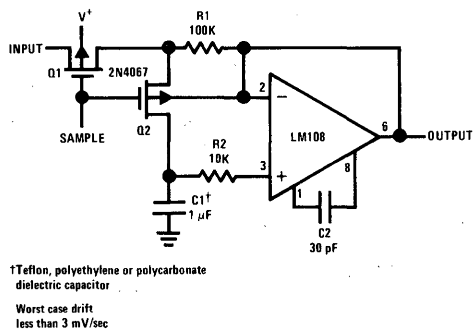


FIGURE 14. Sample And Hold That Eliminates Leakage In FET Switches

When using P-channel MOS switches, the substrate must be connected to a voltage which is always more positive than the input signal. The source-to-substrate junction becomes forward biased if this is not done. The troublesome leakage current of a MOS device occurs across the substrate-to-drain junction. In Figure 14, this current is routed to the output of the buffer amplifier through R_1 so that it does not contribute to the error current.

The main sample switch is Q_1, while Q_2 isolates the hold capacitor from the leakage of Q_1. When the sample pulse is applied, both FETs turn on charging C_1 to the input voltage. Removing the pulse shuts off both FETs, and the output leakage of Q_1 goes through R_1 to the output. The voltage drop across R_1 is less than 10 mV, so the substrate of Q_2 can be bootstrapped to the output of the LM108. Therefore, the voltage across the substrate-drain junction is equal to the offset voltage of the amplifier. At this low voltage, the leakage of the FET is reduced by about two orders of magnitude.

It is necessary to use MOS switches when bootstrapping the leakages in this fashion. The gate leakage of a MOS device is still negligible at high temperatures; this is not the case with junction FETs. If the MOS transistors have protective diodes on the gates, special arrangements must be made to drive Q_2 so the diode does not become forward biased.

In selecting the hold capacitor, low leakage is not the only requirement. The capacitor must also be free of dielectric polarization phenomena.[8] This rules out such types as paper, mylar, electrolytic, tantalum or high-K ceramic. For small capacitor values, glass or silvered-mica capacitors are recommended. For the larger values, ones with teflon, polyethylene or polycarbonate dielectrics should be used.

The low input current of the LM108 gives a drift rate, in hold, of only 3 mV/sec when a 1 µF hold capacitor is used. And this number is worst case over the military temperature range. Even if this kind of performance is not needed, it may still be beneficial to use the LM108 to reduce the size of the hold capacitor. High quality capacitors in the larger sizes are bulky and expensive. Further, the switches must have a low "on" resistance and be driven from a low impedance source to charge large capacitors in a short period of time.

If the sample interval is less than about 100 µs, the LM108 may not be fast enough to work properly. If this is the case, it is advisable to substitute the LM102A,[9] which is a voltage follower designed for both low input current and high speed. It has a 30V/µs slew rate and will operate with sample intervals as short as 1 µs.

When the hold capacitor is larger than 0.05 µF, an isolation resistor should be included between the capacitor and the input of the amplifier (R_2 in Figure 14). This resistor insures that the IC will not be damaged by shorting the output or abruptly shutting down the supplies when the capacitor is charged. This precaution is not peculiar to the LM108 and should be observed on any IC op amp.

INTEGRATORS

Integrators are a lot like sample-and-hold circuits and have essentially the same design problems. In an integrator, a capacitor is used as a storage element; and the error accumulation rate is again proportional to the input current of the op amp.

Figure 15 shows a circuit that can compensate for the bias current of the amplifier. A current is fed into the summing node through R_1 to supply the bias current. The potentiometer, R_2, is adjusted so that this current exactly equals the bias current, reducing the drift rate to zero.

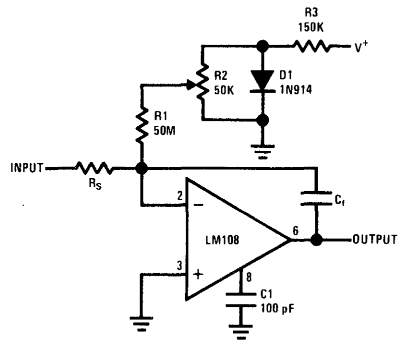


FIGURE 15. Integrator With Bias Current Compensation

The diode is used for two reasons. First, it acts as a regulator, making the compensation relatively insensitive to variations in supply voltage. Secondly, the temperature drift of diode voltage is approximately the same as the temperature drift of bias current. Therefore, the compensation is more effective if the temperature changes. Over a 0°C to 70°C temperature range, the compensation will give a factor of ten reduction in input current. Even better results are achieved if the temperature change is less.

Normally, it is necessary to reset an integrator to establish the initial conditions for integration. Resetting to zero is readily accomplished by shorting the integrating capacitor with a suitable switch. However, as with the sample and hold circuits, semiconductor switches can cause problems because of high-temperature leakage.

A connection that gets rid of switch leakages is shown in Figure 16. A negative-going reset pulse

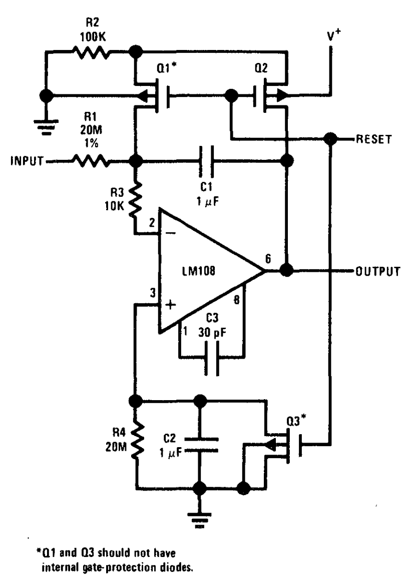


FIGURE 16. Low Drift Integrator With Reset

turns on Q_1 and Q_2, shorting the integrating capacitor. When the switches turn off, the leakage current of Q_2 is absorbed by R_2 while Q_1 isolates the output of Q_2 from the summing node. Q_1 has practically no voltage across its junctions because the substrate is grounded; hence, leakage currents are negligible.

The additional circuitry shown in Figure 16 makes the error accumulation rate proportional to the offset current, rather than the bias current. Hence, the drift is reduced by roughly a factor of 10. During the integration interval, the bias current of the non-inverting input accumulates an error across R_4 and C_2 just as the bias current on the inverting input does across R_1 and C_1. Therefore, if R_4 is matched with R_1 and C_2 is matched with C_1 (within about 5 percent) the output will drift at a rate proportional to the difference in these currents. At the end of the integration interval, Q_3 removes the compensating error accumulated on C_2 as the circuit is reset.

In applications involving large temperature changes, the circuit in Figure 16 gives better results than the compensation scheme in Figure 15—especially under worst case conditions. Over a −55°C to 125°C temperature range, the worst case drift is reduced from 3 mV/sec to 0.5 mV/sec when a 1 μF integrating capacitor is used. If this reduction in drift is not needed, the circuit can be simplified by eliminating R_4, C_2 and Q_3 and returning the non-inverting input of the amplifier directly to ground.

In fabricating low drift integrators, it is again necessary to use high quality components and minimize leakage currents in the wiring. The comments made on capacitors in connection with the sample-and-hold circuits also apply here. As an additional precaution, a resistor should be used to isolate the inverting input from the integrating capacitor if it is larger than 0.05 μF. This resistor prevents damage that might occur when the supplies are abruptly shut down while the integrating capacitor is charged.

Some integrator applications require both speed and low error current. The output amplifiers for photomultiplier tubes or solid-state radiation detectors are examples of this. Although the LM108 is relatively slow, there is a way to speed it up when it is used as an inverting amplifier. This is shown in Figure 17.

The circuit is arranged so that the high-frequency gain characteristics are determined by A_2, while A_1 determines the dc and low-frequency characteristics. The non-inverting input of A_1 is connected to the summing node through R_1. A_1 is operated as an integrator, going through unity gain at 500 Hz. Its output drives the non-inverting input

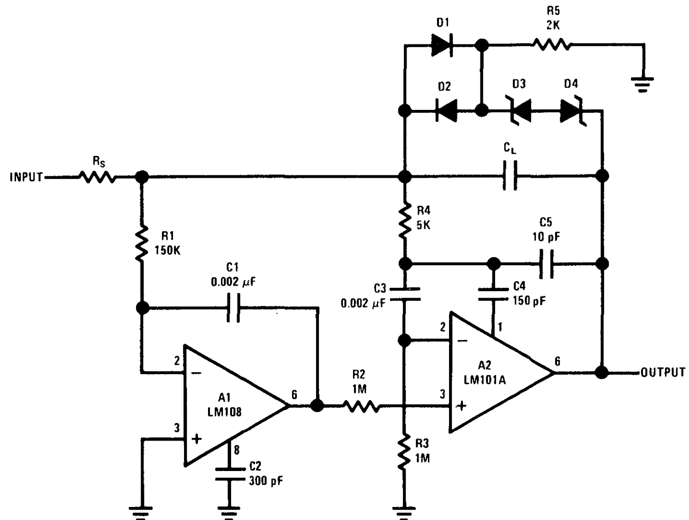


FIGURE 17. Fast Integrator

of A_2. The inverting input of A_2 is also connected to the summing node through C_3. C_3 and R_3 are chosen to roll off below 750 Hz. Hence, at frequencies above 750 Hz, the feedback path is directly around A_2, with A_1 contributing little. Below 500 Hz, however, the direct feedback path to A_2 rolls off; and the gain of A_1 is added to that of A_2.

The high frequency amplifier, A_2, is an LM101A connected with feed-forward compensation.[10] It has a 10 MHz equivalent small-signal bandwidth, a 10V/µs slew rate and a 250 kHz large-signal bandwidth, so these are the high-frequency characteristics of the complete amplifier. The bias current of A_2 is isolated from the summing node by C_3. Hence, it does not contribute to the dc drift of the integrator. The inverting input of A_1 is the only dc connection to the summing junction. Therefore, the error current of the composite amplifier is equal to the bias current of A_1.

If A_2 is allowed to saturate, A_1 will then start towards saturation. If the output of A_1 gets far off zero, recovery from saturation will be slowed drastically. This can be prevented by putting zener clamp diodes across the integrating capacitor. A suitable clamping arrangement is shown in Figure 17. D_1 and D_2 are included in the clamp circuit along with R_5 to keep the leakage currents of the zeners from introducing errors.

In addition to increasing speed, this circuit has other advantages. For one, it has the increased output drive capability of the LM101A. Further, thermal feedback is virtually eliminated because the LM108 does not see load variations. Lastly, the open loop gain is nearly infinite at low frequencies as it is the product of the gains of the two amplifiers.

SINE WAVE OSCILLATOR

Although it is comparatively easy to build an oscillator that approximates a sine wave, making one that delivers a high-purity sinusoid with a stable frequency and amplitude is another story. Most satisfactory designs are relatively complicated and require individual trimming and temperature compensation to make them work. In addition, they generally take a long time to stabilize to the final output amplitude.

A unique solution to most of these problems is shown in Figure 18. A_1 is connected as a two-pole low-pass active filter, and A_2 is connected as an integrator. Since the ultimate phase lag introduced by the amplifiers is 270 degrees, the circuit can be made to oscillate if the loop gain is high enough at the frequency where the lag is 180 degrees. The gain is actually made somewhat higher than is required for oscillation to insure starting. Therefore, the amplitude builds up until it is limited by some nonlinearity in the system.

Amplitude stabilization is accomplished with zener clamp diodes, D_1 and D_2. This does introduce distortion, but it is reduced by the subsequent low pass filters. If D_1 and D_2 have equal breakdown voltages, the resulting symmetrical clipping will

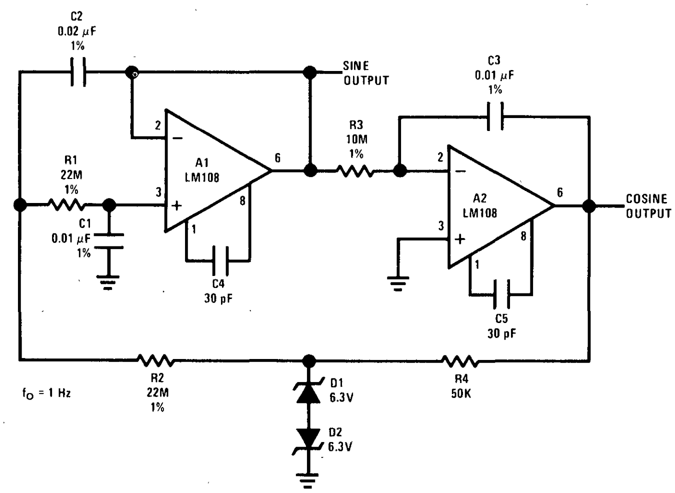


FIGURE 18. Sine Wave Oscillator

virtually eliminate the even-order harmonics. The dominant harmonic is then the third, and this is about 40 dB down at the output of A_1 and about 50 dB down on the output of A_2. This means that the total harmonic distortion on the two outputs is 1 percent and 0.3 percent, respectively.

The frequency of oscillation and the oscillation threshold are determined by R_1, R_2, R_3, C_1, C_2 and C_3. Therefore precision components with low temperature coefficients should be used. If R_3 is made lower than shown, the circuit will accept looser component tolerances before dropping out of oscillation. The start up will also be quicker. However, the price paid is that distortion is increased. The value of R_4 is not critical, but it should be made much smaller than R_2 so that the effective resistance at R_2 does not drop when the clamp diodes conduct.

The output amplitude is determined by the breakdown voltages of D_1 and D_2. Therefore, the clamp level should be temperature compensated for stable operation. Diode-connected (collector shorted to base) NPN transistors with an emitter-base breakdown of about 6.3V work well, as the positive temperature coefficient of the diode in reverse breakdown nearly cancels the negative temperature coefficient of the forward-biased diode. Added advantages of using transistors are that they have less shunt capacitance and sharper breakdowns than conventional zeners.

The LM108 is particularly useful in this circuit at low frequencies, since it permits the use of small capacitors. The circuit shown oscillates at 1 Hz, but uses capacitors in the order of 0.01 μF. This makes it much easier to find temperature-stable precision capacitors. However, some judgment must be used as large value resistors with low temperature coefficients are not exactly easy to come by.*

The LM108s are useful in this circuit for output frequencies up to 1 kHz. Beyond that, better performance can be realized by substituting an LM102A for A_1 and an LM101A with feedforward compensation for A_2. The improved high-frequency response of these devices extends the operating frequency out to 100 kHz.

CAPACITANCE MULTIPLIER

Large capacitor values can be eliminated from most systems just by raising the impedance levels, if suitable op amps are available. However, sometimes it is not possible because the impedance levels are already fixed by some element of the system like a low impedance transducer. If this is the case, a capacitance multiplier can be used to increase the effective capacitance of a small capacitor and couple it into a low impedance system.

Previously, IC op amps could not be used effectively as capacitance multipliers because the equivalent leakages generated due to offset current were significantly greater than the leakages of large tantalum capacitors. With the LM108, this has changed. The circuit shown in Figure 19 generates

*Large-value resistors are available from Victoreen Instrument, Cleveland, Ohio and Pyrofilm Resistor Co., Whippany, New Jersey.

an equivalent capacitance of 100,000 μF with a worst case leakage of 8 μA—over a −55°C to 125°C temperature range.

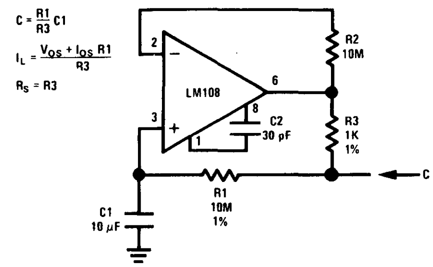


FIGURE 19. Capacitance Multiplier

The performance of the circuit is described by the equations given in Figure 19, where C is the effective output capacitance, I_L is the leakage current of this capacitance and R_s is the series resistance of the multiplied capacitance. The series resistance is relatively high, so high-Q capacitors cannot be realized. Hence, such applications as tuned circuits and filters are ruled out. However, the multiplier can still be used in timing circuits or servo compensation networks where some resistance is usually connected in series with the capacitor or the effect of the resistance can be compensated for.

One final point is that the leakage current of the multiplied capacitance is not a function of the applied voltage. It persists even with no voltage on the output. Therefore, it can generate offset errors in a circuit, rather than the scaling errors caused by conventional capacitors.

INSTRUMENTATION AMPLIFIER

In many instrumentation applications there is frequently a need for an amplifier with a high-impedance differential input and a single ended output. Obvious uses for this are amplifiers for bridge-type signal sources such as strain gages, temperature sensors or pressure transducers. General purpose op amps have satisfactory input characteristics, but feedback must be added to determine the effective gain. And the addition of feedback can drastically reduce the input resistance and degrade common mode rejection.

Figure 20 shows the classical op amp circuit for a differential amplifier. This circuit has three main disadvantages. First, the input resistance on the inverting input is relatively low, being equal to R_1. Second, there usually is a large difference in the input resistance of the two inputs, as is indicated by the equations on the schematic. Third, the common mode rejection is greatly affected by resistor matching and by balancing of the source resistances. A 1-percent deviation in any one of the resistor values reduces the common mode rejection to 46 dB for a closed loop gain of 1, to 60 dB for a gain of 10 and to 80 dB for a gain of 100.

Clearly, the only way to get high input impedance is to use very large resistors in the feedback network. The op amp must operate from a source resistance which is orders of magnitude larger than the resistance of the signal source. Older IC op amps introduced excessive offset and drift when operating from higher resistances and could not be used successfully. The LM108, however, is relatively unaffected by the large resistors, so this approach can sometimes be employed.

With large input resistors, the feedback resistors, R_3 and R_4, can get quite large for higher closed loop gains. For example, if R_1 and R_2 are 1 MΩ, R_3 and R_4 must be 100 MΩ for a gain of 100. It is difficult to accurately match resistors that are this high in value, so common mode rejection may suffer. Nonetheless, any one of the resistors can be trimmed to take out common mode feedthrough caused either by resistor mismatches or the amplifier itself.

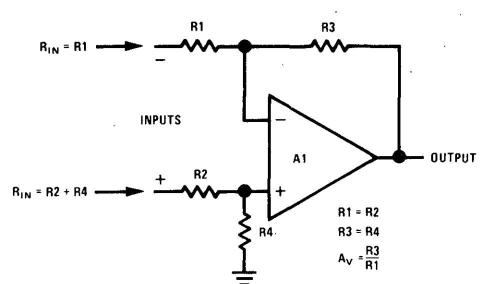


FIGURE 20. Feedback Connection For a Differential Amplifier

Another problem caused by large feedback resistors is that stray capacitance can seriously affect the high frequency common mode rejection. With 1 MΩ input resistors, a 1 pF mismatch in stray capacitance from either input to ground can drop the common mode rejection to 40 dB at 1500 Hz. The high frequency rejection can be improved at the expense of frequency response by shunting R_3 and R_4 with matched capacitors.

With high impedance bridges, the feedback resistances become prohibitively large even for the LM108, so the circuit in Figure 20 cannot be used. One possible alternative is shown in Figure 21. R_2 and R_3 are chosen so that their equivalent parallel resistance is equal to R_1. Hence, the output of the amplifier will be zero when the bridge is balanced.

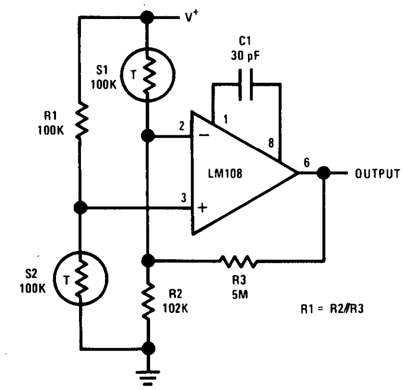


FIGURE 21. Amplifier For Bridge Transducers

When the bridge goes off balance, the op amp maintains the voltage between its input terminals at zero with current fed back from the output through R_3. This circuit does not act like a true differential amplifier for large imbalances in the bridge. The voltage drops across the two sensor resistors, S_1 and S_2, become unequal as the bridge goes off balance, causing some non-linearity in the transfer function. However, this is not usually objectionable for small signal swings.

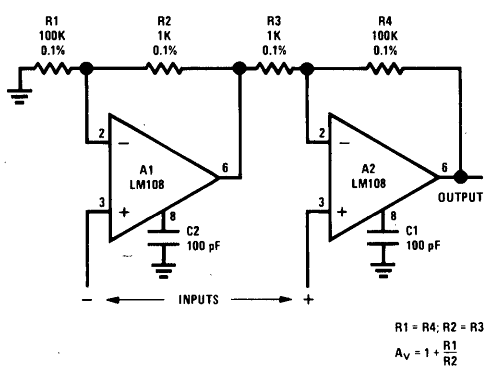


FIGURE 22. Differential Input Instrumentation Amplifier

Figure 22 shows a true differential connection that has few of the problems mentioned previously. It has an input resistance greater than $10^{10}\Omega$, yet it does not need large resistors in the feedback circuitry. With the component values shown, A_1 is connected as a non-inverting amplifier with a gain of 1.01; and it feeds into A_2 which has an inverting gain of 100. Hence, the total gain from the input of A_1 to the output of A_2 is 101, which is equal to the non-inverting gain of A_2. If all the resistors are matched, the circuit responds only to the differential input signal—not the common mode voltage.

This circuit has the same sensitivity to resistor matching as the previous circuits, with a 1 percent mismatch between two resistors lowering the common mode rejection to 80 dB. However, matching is more easily accomplished because of the lower resistor values. Further, the high frequency common mode rejection is less affected by stray capacitances. The high frequency rejection is limited, though, by the response of A_1.

LOGARITHMIC CONVERTER

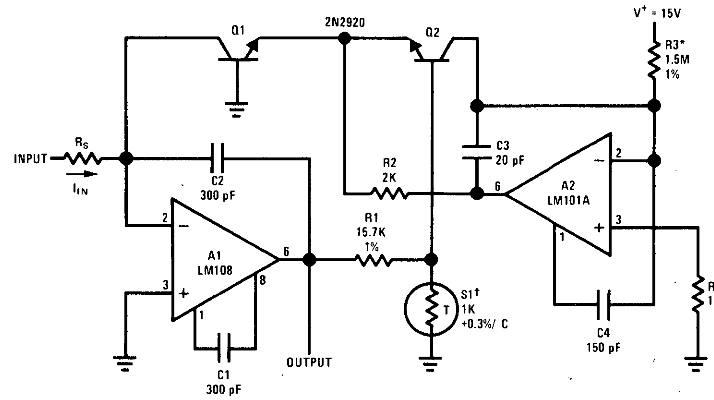
A logarithmic amplifier is another circuit that can take advantage of the low input current of an op amp to increase dynamic range. Most practical log converters make use of the logarithmic relationship between the emitter-base voltage of standard double-diffused transistors and their collector current. This logarithmic characteristic has been proven true for over 9 decades of collector current. The only problem involved in using transistors as logging elements is that the scale factor has a temperature sensitivity of 0.3 percent/°C. However, temperature compensating resistors have been developed to compensate for this characteristic, making possible log converters that are accurate over a wide temperature range.

Figure 23 gives a circuit that uses these techniques. Q_1 is the logging transistor, while Q_2 provides a fixed offset to temperature compensate the emitter-base turn on voltage of Q_1. Q_2 is operated at a fixed collector current of 10 μA by A_2, and its emitter-base voltage is subtracted from that of Q_1 in determining the output voltage of the circuit. The collector current of Q_2 is established by R_3 and V^+ through A_2.

The collector current of Q_1 is proportional to the input current through R_s and, therefore, proportional to the input voltage. The emitter-base voltage of Q_1 varies as the log of the input voltage. The fixed emitter-base voltage of Q_2 subtracts from the voltage on the emitter of Q_1 in determining the voltage on the top end of the temperature-compensating resistor, S_1.

The signal on the top of S_1 will be zero when the input current is equal to the current through R_3 at any temperature. Further, this voltage will vary logarithmically for changes in input current, although the scale factor will have a temperature coefficient of −0.3%/°C. The output of the converter is essentially multiplied by the ratio of R_1 to S_1. Since S_1 has a positive temperature coefficient of 0.3 percent/°C, it compensates for the change in scale factor with temperature.

In this circuit, an LM101A with feedforward compensation is used for A_2 since it is much faster than the LM108 used for A_1. Since both amplifiers are cascaded in the overall feedback loop, the reduced phase shift through A_2 insures stability.



$10\ nA < I_{IN} < 1\ mA$
Sensitivity is 1V per decade.

†Available from Tel Labs, Inc., Manchester, N.H., Type Q81.
*Determines current for zero crossing on output: 10 μA as shown.

FIGURE 23. Temperature Compensated One-Quadrant Logarithmic Converter

Certain things must be considered in designing this circuit. For one, the sensitivity can be changed by varying R_1. But R_1 must be made considerably larger than the resistance of S_1 for effective temperature compensation of the scale factor. Q_1 and Q_2 should also be matched devices in the same package, and S_1 should be at the same temperature as these transistors. Accuracy for low input currents is determined by the error caused by the bias current of A_1. At high currents, the behavior of Q_1 and Q_2 limits accuracy. For input currents approaching 1 mA, the 2N2920 develops logging errors in excess of 1 percent. If larger input currents are anticipated, bigger transistors must be used; and R_2 should be reduced to insure that A_2 does not saturate.

TRANSDUCER AMPLIFIERS

With certain transducers, accuracy depends on the choice of the circuit configuration as much as it does on the quality of the components. The amplifier for photodiode sensors, shown in Figure 24, illustrates this point. Normally, photodiodes are operated with reverse voltage across the junction. At high temperatures, the leakage currents can approach the signal current. However, photodiodes deliver a short-circuit output current, unaffected by leakage currents, which is not significantly lower than the output current with reverse bias.

The circuit shown in Figure 24 responds to the short-circuit output current of the photodiode. Since the voltage across the diode is only the offset voltage of the amplifier, inherent leakage is reduced by at least two orders of magnitude. Neglecting the offset current of the amplifier, the output current of the sensor is multiplied by R_1 plus R_2 in determining the output voltage.

Figure 25 shows an amplifier for high-impedance ac transducers like a piezoelectric accelerometer. These sensors normally require a high-input-resistance amplifier. The LM108 can provide input resistances in the range of 10 to 100 MΩ, using conventional circuitry. However, conventional designs are sometimes ruled out either because

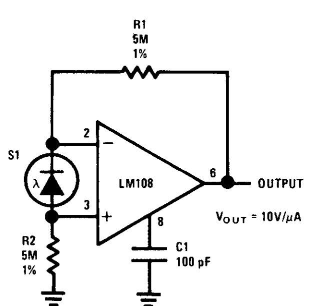


FIGURE 24. Amplifier For Photodiode Sensor

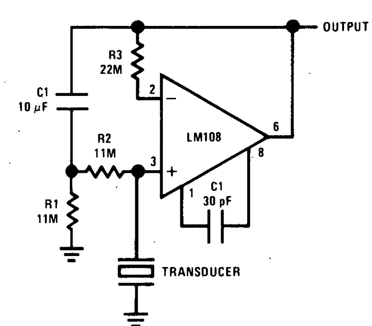


FIGURE 25. Amplifier For Piezoelectric Transducers

large resistors cannot be used or because prohibitively large input resistances are needed.

Using the circuit in Figure 25, input resistances that are orders of magnitude greater than the values of the dc return resistors can be obtained. This is accomplished by bootstrapping the resistors to the output. With this arrangement, the lower cutoff frequency of a capacitive transducer is determined more by the RC product of R_1 and C_1 than it is by resistor values and the equivalent capacitance of the transducer.

RESISTANCE MULTIPLICATION

When an inverting operational amplifier must have high input resistance, the resistor values required can get out of hand. For example, if a 2 MΩ input resistance is needed for an amplifier with a gain of 100, a 200 MΩ feedback resistor is called for. This resistance can, however, be reduced using the circuit in Figure 26. A divider with a ratio of 100 to 1 (R_3 and R_4) is added to the output of the amplifier: Unity-gain feedback is applied from the output of the divider, giving an overall gain of 100 using only 2 MΩ resistors.

This circuit does increase the offset voltage somewhat. The output offset voltage is given by

$$V_{OUT} = \left(\frac{R_1 + R_2}{R_2}\right) A_V\, V_{os}.$$

The offset voltage is only multiplied by $A_V + 1$ in a conventional inverter. Therefore, the circuit in Figure 26 multiplies the offset by 200, instead of 101. This multiplication factor can be reduced to 110 by increasing R_2 to 20 MΩ and R_3 to 5.55k.

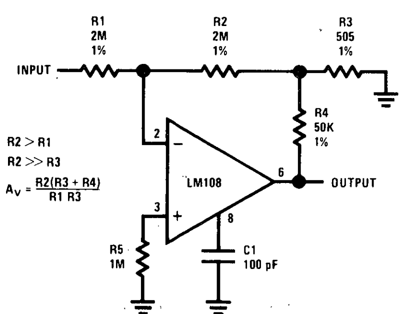


FIGURE 26. Inverting Amplifier With High Input Resistance

Another disadvantage of the circuit is that four resistors determine the gain, instead of two. Hence, for a given resistor tolerance, the worst-case gain deviation is greater, although this is probably more than offset by the ease of getting better tolerances in the low resistor values.

CURRENT SOURCES

Although there are numerous ways to make current sources with op amps, most have limitations as far as their application is concerned. Figure 27, however, shows a current source which is fairly flexible and has few restrictions as far as its use is concerned. It supplies a current that is proportional to the input voltage and drives a load referred to ground or any voltage within the output-swing capability of the amplifier.

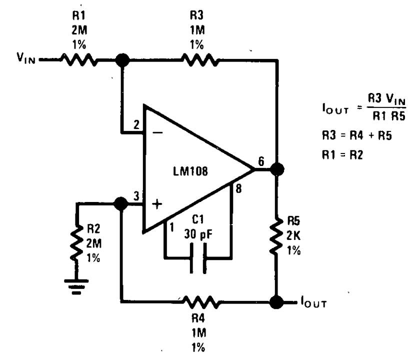


FIGURE 27. Bilateral Current Source

With the output grounded, it is relatively obvious that the output current will be determined by R_5 and the gain setting of the op amp, yielding

$$I_{OUT} = -\frac{R_3\, V_{IN}}{R_1\, R_5}.$$

When the output is not at zero, it would seem that the current through R_2 and R_4 would reduce accuracy. Nonetheless, if $R_1 = R_2$ and $R_3 = R_4 + R_5$, the output current will be independent of the output voltage. For $R_1 + R_3 >> R_5$, the output resistance of the circuit is given by

$$R_{OUT} \cong R_5 \left(\frac{R}{\Delta R}\right)$$

where R is any one of the feedback resistors (R_1, R_2, R_3 or R_4) and ΔR is the incremental change in the resistor value from design center. Hence, for the circuit in Figure 27, a 1 percent deviation in one of the resistor values will drop the output resistance of 200 kΩ. Such errors can be trimmed out by adjusting one of the feedback resistors. In design, it is advisable to make the feedback resistors as large as possible. Otherwise, resistor tolerances become even more critical.

The circuit must be driven from a source resistance which is low by comparison to R_1, since this resistance will imbalance the circuit and affect both gain and output resistance. As shown, the circuit gives a negative output current for a positive input voltage. This can be reversed by grounding the input and driving the ground end of R_2. The magnitude of the scale factor will be unchanged as long as $R_4 >> R_5$.

VOLTAGE COMPARATORS

Like most op amps, it is possible to use the LM108 as a voltage comparator. Figure 28 shows the device used as a simple zero-crossing detector. The inputs of the IC are protected internally by back-

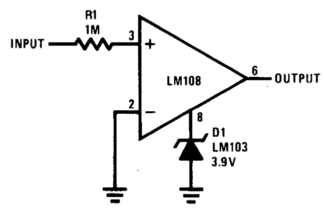


FIGURE 28. Zero Crossing Detector

to-back diodes connected between them, therefore, voltages in excess of 1V cannot be impressed directly across the inputs. This problem is taken care of by R_1 which limits the current so that input voltages in excess of 1 kV can be tolerated. If absolute accuracy is required or if R_1 is made much larger than 1 MΩ, a compensating resistor of equal value should be inserted in series with the other input.

In Figure 28, the output of the op amp is clamped so that it can drive DTL or TTL directly. This is accomplished with a clamp diode on pin 8. When the output swings positive, it is clamped at the breakdown voltage of the zener. When it swings negative, it is clamped at a diode drop below ground. If the 5V logic supply is used as a positive supply for the amplifier, the zener can be replaced with an ordinary silicon diode. The maximum fan out that can be handled by the device is one for standard DTL or TTL under worst case conditions.

As might be expected, the LM108 is not very fast when used as a comparator. The response time is up in the tens of microseconds. An LM103[11] is recommended for D_1, rather than a conventional alloy zener, because it has lower capacitance and will not slow the circuit further. The sharp breakdown of the LM103 at low currents is also an advantage as the current through the diode in clamp is only 10 μA.

Figure 29 shows a comparator for voltages of opposite polarity. The output changes state when the voltage on the junction of R_1 and R_2 is equal to V_{TH}. Mathematically, this is expressed by

$$V_{TH} = V_2 + \frac{R_2 (V_1 - V_2)}{R_1 + R_2}.$$

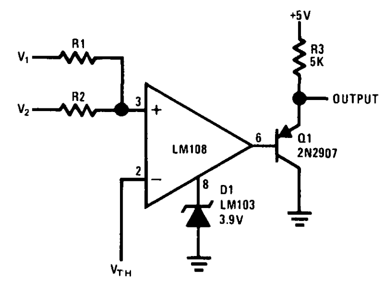


FIGURE 29. Voltage Comparator With Output Buffer

The LM108 can also be used as a differential comparator, going through a transition when two input voltages are equal. However, resistors must be inserted in series with the inputs to limit current and minimize loading on the signal sources when the input-protection diodes conduct. Figure 29 also shows how a PNP transistor can be added on the output to increase the fan out to about 20 with standard DTL or TTL.

POWER BOOSTER

The LM108, which was designed for low power consumption, is not able to drive heavy loads. However, a relatively simple booster can be added to the output to increase the output current to ±50 mA. This circuit, shown in Figure 30, has the added advantage that it swings the output up to the supplies, within a fraction of a volt. The increased voltage swing is particularly helpful in low voltage circuits.

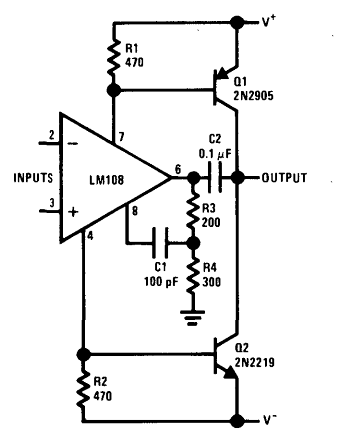


FIGURE 30. Power Booster

In Figure 30, the output transistors are driven from the supply leads of the op amp. It is important that R_1 and R_2 be made low enough so Q_1 and Q_2 are not turned on by the *worst case* quiescent current of the amplifier. The output of the op amp is loaded heavily to ground with R_3 and R_4.

When the output swings about 0.5V positive, the increasing positive supply current will turn on Q_1 which pulls up the load. A similar situation occurs with Q_2 for negative output swings.

The bootstrapped shunt compensation shown in the figure is the only one that seems to work for all loading conditions. This capacitor, C_1, can be made inversely proportional to the closed loop gain to optimize frequency response. The value given is for a unity-gain follower connection. C_2 is also required for loop stability.

The circuit does have a dead zone in the open loop transfer characteristic. However, the low frequency gain is high enough so that it can be neglected. Around 1 kHz, though, the dead zone becomes quite noticeable.

Current limiting can be incorporated into the circuit by adding resistors in series with the emitters of Q_1 and Q_2 because the short circuit protection of the LM108 limits the maximum voltage drop across R_1 and R_2.

BOARD CONSTRUCTION

As indicated previously, certain precautions must be observed when building circuits that are sensitive to very low currents. If proper care is not taken, board leakage currents can easily become much larger than the error currents of the op amp. To prevent this, it is necessary to thoroughly clean printed circuit boards. Even experimental breadboards must be cleaned with trichloroethlene or alcohol to remove solder fluxes, and blown dry with compressed air. These fluxes may be insulators at low impedance levels—like in electric motors—but they certainly are not in high impedance circuits. In addition to causing gross errors, their presence can make the circuit behave erratically, especially as the temperature is changed.

At elevated temperatures, even the leakage of clean boards can be a headache. At 125°C the leakage resistance between adjacent runs on a printed circuit board is about $10^{11}\,\Omega$ (0.05-inch separation parallel for 1 inch) for high quality epoxy-glass boards that have been properly cleaned. Therefore, the boards can easily produce error currents in the order of 200 pA and much more if they become contaminated. Conservative practice dictates that the boards be coated with epoxy or silicone rubber after cleaning to prevent contamination. Silicone rubber is the easiest to use. However, if the better durability of epoxy is needed, care must be taken to make sure that it gets thoroughly cured. Otherwise, the epoxy will make high temperature leakage much worse.

Care must also be exercised to insure that the circuit board is protected from condensed water vapor when operating in the vicinity of 0°C. This can usually be accomplished by coating the board as mentioned above.

GUARDING

Even with properly cleaned and coated boards, leakage currents are on the verge of causing trouble at 125°C. The standard pin configuration of most IC op amps has the input pins adjacent to pins which are at the supply potentials. Therefore, it is advisable to employ guarding to reduce the voltage difference between the inputs and adjacent metal runs.

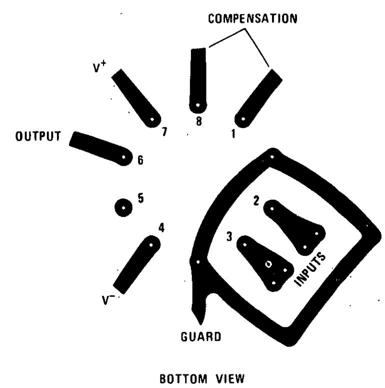
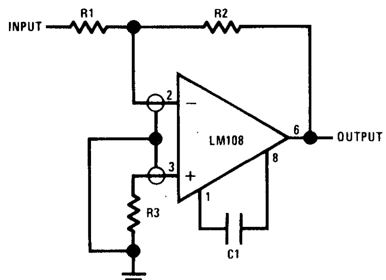


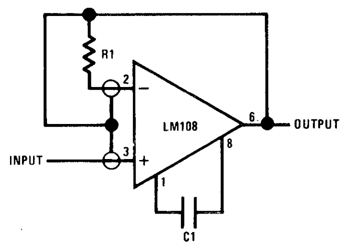
FIGURE 31. Printed Circuit Layout For Input Guarding With TO-5 Package

A board layout that includes input guarding is shown in Figure 31 for the eight lead TO-5 package. A ten-lead pin circle is used, and the leads of the IC are formed so that the holes adjacent to the inputs are vacant when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is then connected to a low impedance point that is at the same potential as the inputs. The leakage currents from the pins at the supply potentials are absorbed by the guard. The voltage difference between the guard and the inputs can be made approximately equal to the offset voltage, reducing the effective leakage by more than three orders of magnitude. If the leads of the integrated circuit, or other components connected to the input, go through the board, it may be necessary to guard both sides.

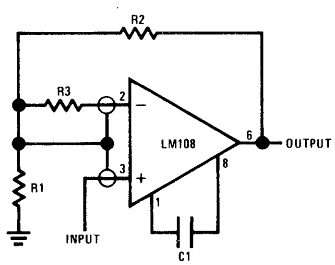
Figure 32 shows how the guard is committed on the more-common op amp circuits. With an integrator or inverting amplifier, where the inputs are close to ground potential, the guard is simply grounded. With the voltage follower, the guard is bootstrapped to the output. If it is desirable to put a resistor in the inverting input to compensate for the source resistance, it is connected as shown in Figure 32b.



a. Inverting Amplifier



b. Follower



c. Non-Inverting Amplifier

FIGURE 32. Connection Of Input Guards

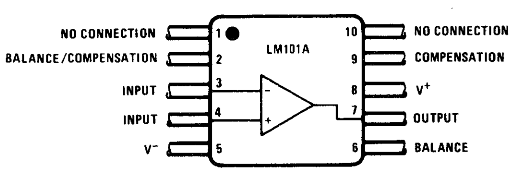
Guarding a non-inverting amplifier is a little more complicated. A low impedance point must be created by using relatively low value feedback resistors to determine the gain (R_1 and R_2 in Figure 32c). The guard is then connected to the junction of the feedback resistors. A resistor, R_3, can be connected as shown in the figure to compensate for large source resistances.

With the dual-in-line and flat packages, it is far more difficult to guard the inputs, if the standard pin configuration of the LM709 or LM101A is used, because the pin spacings on these packages are fixed. Therefore, the pin configuration of the LM108 was changed, as shown in Figure 33.

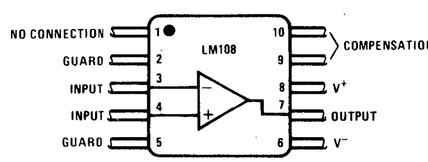
CONCLUSIONS

IC op amps are now available that equal the input current specifications of FET amplifiers in all but the most restricted temperature range applications. At operating temperatures above 85°C, the IC is clearly superior as it uses bipolar transistors that make it possible to eliminate the leakage currents that plague FETs. Additionally, bipolar transistors match better than FETs, so low offset voltage and drifts can be obtained without expensive adjustments or selection. Further, the bipolar devices lend themselves more readily to low-cost monolithic construction.

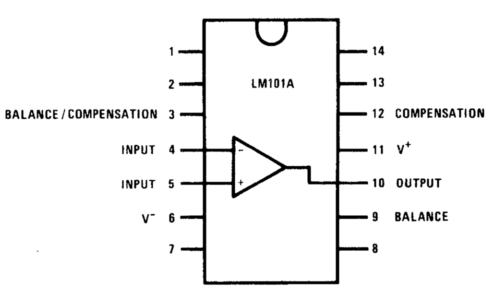
These amplifiers open up new application areas and vastly improve performance in others. For example, in analog memories, holding intervals can be extended to minutes, even where −55°C to 125°C operation is involved. Instrumentation amplifiers and low frequency waveform generators also benefit from the low error currents.



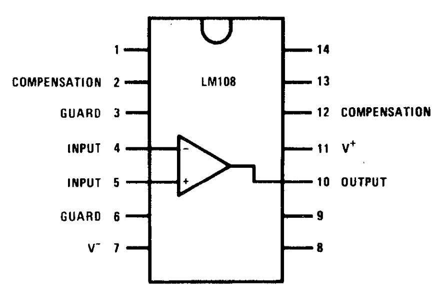
NOTE: Pin 5 Connected to bottom of package.
TOP VIEW



NOTE: Pin 6 connected to bottom of package
TOP VIEW



NOTE: Pin 6 connected to bottom of package.
TOP VIEW



NOTE: Pin 7 connected to bottom of package
TOP VIEW

FIGURE 33. Comparing Connection Diagrams Of The LM101A And LM108, Showing Addition Of Guarding

When operating above 85°C, overall performance is frequently limited by components other than the op amp, unless certain precautions are observed. It is generally necessary to redesign circuits using semiconductor switches to reduce the effect of their leakage currents. Further, high quality capacitors must be used, and care must be exercised in selecting large value resistors. Printed circuit board leakages can also be troublesome unless the boards are properly treated. And above 100°C, it is almost mandatory to employ guarding on the boards to protect the inputs, if the full potential of the amplifier is to be realized.

APPENDIX

A complete schematic of the LM108 is given in Figure A1. A description of the basic circuit is presented along with a simplified schematic earlier in the text. The purpose of this Appendix is to explain some of the more subtle features of the design.

The current source supplying the input transistors is Q_{29}. It is designed to supply a total input stage current of 6 μA at 25°C. This current drops to 3 μA at −55°C but increases to only 7.5 μA at 125°C. This temperature characteristic tends to compensate for the current gain falloff of the input transistors at low temperatures without creating stability problems at high temperatures.

The biasing circuitry for the input current source is nearly identical to that in the LM101A, and a complete description is given in Reference 4. However, a brief explanation follows.

A collector FET,[6] Q_{23}, which has a saturation current of about 30 μA, establishes the collector current of Q_{24}. This FET provides the initial turn-on current for the circuit and insures starting under all conditions. The purpose of R_{14} is to compensate for production and temperature variations in the FET current. It is a collector resistor (indicated by the T through it) made of the same semiconductor material as the FET channel. As the FET current varies, the drop across R_{14} tends to compensate for changes in the emitter base voltage of Q_{24}.

The collector-emitter voltage of Q_{24} is equal to the emitter base voltage of Q_{24} plus that of Q_{25}. This voltage is delivered to Q_{26} and Q_{29}. Q_{25} and Q_{24} are operated at substantially higher currents than Q_{26} and Q_{29}. Hence, there is a differential in

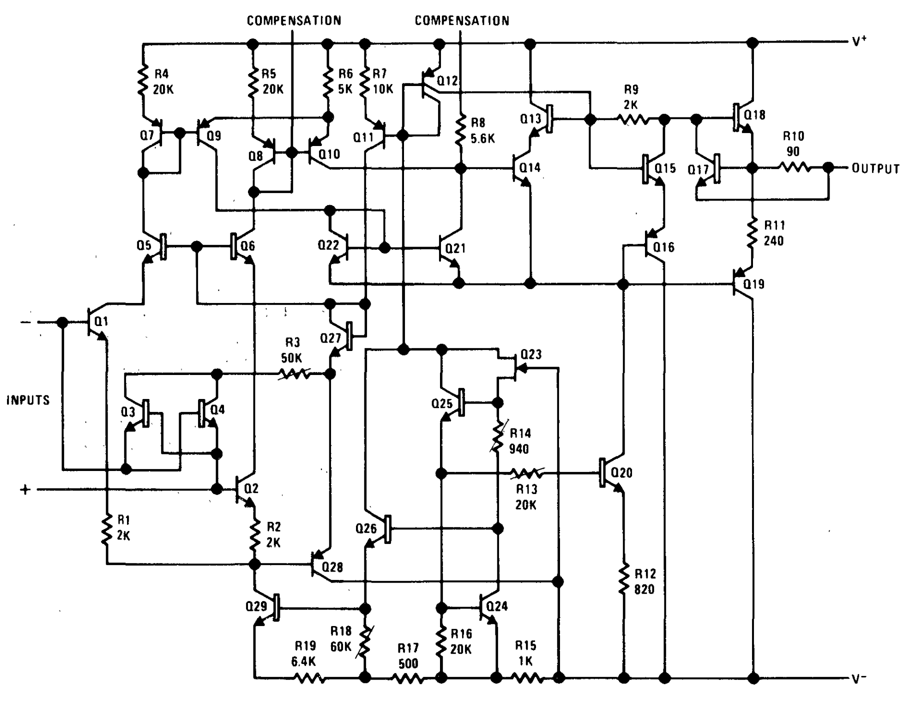


FIGURE A1. Complete Schematic Of The LM108

their emitter base voltages that is dropped across R_{19} to determine the input stage current. R_{18} is a pinched base resistor, as is indicated by the slash bar through it. This resistor, which has a large positive temperature coefficient, operates in conjunction with R_{17} to help shape the temperature characteristics of the input stage current source.

The output currents of Q_{26}, Q_{25} and Q_{23} are fed to Q_{12}, which is a controlled-gain lateral PNP.[6] It delivers one-half of the combined currents to the output stage. Q_{11} is also connected to Q_{12}, with its output current set at approximately 15 μA by R_7. Since this type of current source makes use of the emitter-base voltage differential between similar transistors operating at different collector currents, the output of Q_{11} is relatively independent of the current delivered to Q_{12}.[12] This current is used for the input stage bootstrapping circuitry.

Q_{20} also supplies current to the class-B output stage. Its output current is determined by the ratio of R_{15} to R_{12} and the current through R_{12}. R_{13} is included so that the biasing circuitry is not upset when Q_{20} saturates.

One major departure from the simplified schematic is the bootstrapping of the second stage active loads, Q_{21} and Q_{22}, to the output. This makes the second stage gain dependent only on how well Q_9 and Q_{10} match with variations in output voltage. Hence, the second stage gain is quite high. In fact, the overall gain of the amplifier is typically in excess of 10^6 at dc.

The second stage active loads drive Q_{14}. A high-gain primary transistor is used to prevent loading of the second stage. Its collector is bootstrapped by Q_{13} to operate it at zero collector-base voltage. The class-B output stage is actually driven by the emitter of Q_{14}.

A dead zone in the output stage is prevented by biasing Q_{18} and Q_{19} on the verge of conduction with Q_{15} and Q_{16}. R_9 is used to compensate for the transconductance of Q_{15} and Q_{16}, making the output stage quiescent current relatively independent of the output current of Q_{12}. The drop across this resistor also reduces quiescent current.

For positive-going outputs, short circuit protection is provided by R_{10} and Q_{17}. When the voltage drop across R_{10} turns on Q_{17}, it removes base drive from Q_{18}. For negative-going outputs, current limiting is initiated when the voltage drop across R_{11} becomes large enough for the collector base junction of Q_{17} to become forward biased. When this happens, the base of Q_{19} is clamped so the output current cannot increase further.

Input protection is provided by Q_3 and Q_4 which act as clamp diodes between the inputs. The collectors of these transistors are bootstrapped to the emitter of Q_{28} through R_3. This keeps the collector-isolation leakage of the transistors from showing up on the inputs. R_3 is included so that the bootstrapping is not disrupted when Q_3 or Q_4 saturate with an input overload. Current-limiting resistors were not connected in series with the inputs, since diffused resistors cannot be employed such that they work effectively, without causing high temperature leakages.

Table I. Typical Performance of the LM108 Operational Amplifier ($T_A = 25°C$ and $V_S = \pm15V$).

Input Offset Voltage	0.7 mV
Input Offset Current	50 pA
Input Bias Current	0.8 nA
Input Resistance	70 MΩ
Input Common Mode Range	±14V
Common Mode Rejection	100 dB
Offset Voltage Drift	3 μV/°C
Offset Current Drift	0.5 pA/°C
Voltage Gain	300V/mV
Small Signal Bandwidth	1.0 MHz
Slew Rate	0.3V/μs
Output Swing	±14V
Supply Current	300 μA
Power Supply Rejection	100 dB
Operating Voltage Range	±2V to ±20V

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November 1969

LOGARITHMIC CONVERTERS

One of the most predictable non-linear elements commonly available is the bipolar transistor. The relationship between collector current and emitter base voltage is precisely logarithmic from currents below one picoamp to currents above one milliamp. Using a matched pair of transistors and integrated circuit operational amplifiers, it is relatively easy to construct a linear to logarithmic converter with a dynamic range in excess of five decades.

The circuit in Figure 1 generates a logarithmic output voltage for a linear input current. Transistor Q_1 is used as the non-linear feedback element around an LM108 operational amplifier. Negative feedback is applied to the emitter of Q_1 through divider, R_1 and R_2, and the emitter base junction of Q_2. This forces the collector current of Q_1 to be exactly equal to the current through the input resistor. Transistor Q_2 is used as the feedback element of an LM101A operational amplifier. Negative feedback forces the collector current of Q_2 to equal the current through R_3. For the values shown, this current is 10 μA. Since the collector current of Q_2 remains constant, the emitter base voltage also remains constant. Therefore, only the V_{BE} of Q_1 varies with a change of input current. However, the output voltage is a function of the difference in emitter base voltages of Q_1 and Q_2:

$$E_{OUT} = \frac{R_1 + R_2}{R_2} (V_{BE_2} - V_{BE_1}). \qquad (1)$$

For matched transistors operating at different collector currents, the emitter base differential is given by

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C_1}}{I_{C_2}} \qquad (2)$$

where k is Boltzmann's constant, T is temperature in degrees Kelvin and q is the charge of an electron. Combining these two equations and writing the expression for the output voltage gives

$$E_{OUT} = \frac{-kT}{q} \left[\frac{R_1 + R_2}{R_2}\right] \log_e \left[\frac{E_{IN}\, R_3}{E_{REF}\, R_{IN}}\right] \qquad (3)$$

for $E_{IN} \geq 0$. This shows that the output is proportional to the logarithm of the input voltage. The coefficient of the log term is directly proportional to absolute temperature. Without compensation, the scale factor will also vary directly with temperature. However, by making R_2 directly proportional to temperature, constant gain is obtained. The temperature compensation is typically 1% over a temperature range of −25°C to 100°C for the resistor specified. For limited temperature range applications, such as 0°C to 50°C, a 430Ω sensistor in series with a 570Ω resistor may be substituted for the 1K resistor, also with 1% accuracy. The divider, R_1 and R_2, sets the gain while the current through R_3 sets the zero. With the values given, the scale factor is 1V/decade and

$$E_{OUT} = -\left[\log_{10} \left|\frac{E_{IN}}{R_{IN}}\right| + 5\right] \qquad (4)$$

where the absolute value sign indicates that the dimensions of the quantity inside are to be ignored.

Log generator circuits are not limited to inverting operation. In fact, a feature of this circuit is the ease with which non-inverting operation is obtained. Supplying the input signal to A_2 and the reference current to A_1 results in a log output that is not inverted from the input. To achieve the same 100 dB dynamic range in the non-inverting configuration, an LM108 should be used for A_2, and an LM101A for A_1. Since the LM108 cannot use feedforward compensation, it is frequency compensated with the standard 30 pF capacitor.

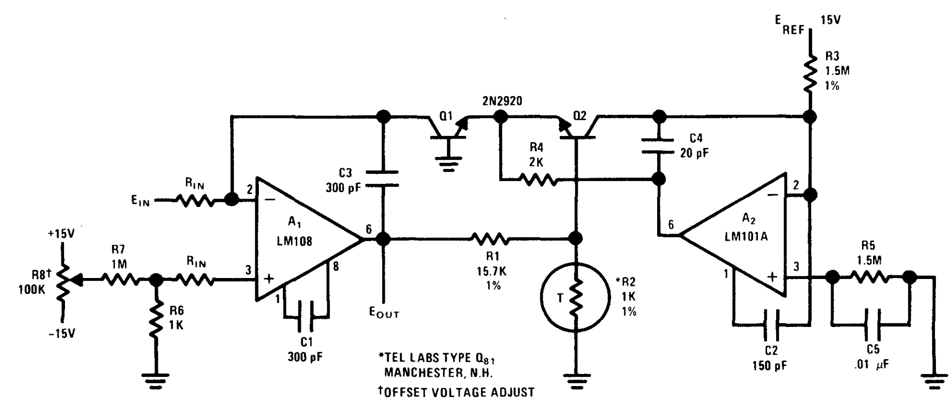

FIGURE 1. Log Generator with 100 dB Dynamic Range

The only other change is the addition of a clamp diode connected from the emitter of Q_1 to ground. This prevents damage to the logging transistors if the input signal should go negative.

The log output is accurate to 1% for any current between 10 nA and 1 mA. This is equivalent to about 3% referred to the input. At currents over 500 μA the transistors used deviate from log characteristics due to resistance in the emitter, while at low currents, the offset current of the LM108 is the major source of error. These errors occur at the ends of the dynamic range, and from 40 nA to 400 μA the log converter is 1% accurate referred to the input. Both of the transistors are used in the grounded base connection, rather than the diode connection, to eliminate errors due to base current. Unfortunately, the grounded base connection increases the loop gain. More frequency compensation is necessary to prevent oscillation, and the log converter is necessarily slow. It may take 1 to 5 ms for the output to settle to 1% of its final value. This is especially true at low currents.

the transfer function. With the values shown the scale factor is 1V/decade and

$$E_{OUT} = -\left[\log_{10}\left|\frac{E_{IN}}{R_{IN}}\right| + 4\right] \qquad (5)$$

from less than 100 nA to 1 mA.

Anti-log or exponential generation is simply a matter of rearranging the circuitry. Figure 3 shows the circuitry of the log converter connected to generate an exponential output from a linear input. Amplifier A_1 in conjunction with transistor Q_1 drives the emitter of Q_2 in proportion to the input voltage. The collector current of Q_2 varies exponentially with the emitter-base voltage. This current is converted to a voltage by amplifier A_2. With the values given

$$E_{OUT} = 10^{-[E_{IN}]} \qquad (6)$$

Many non-linear functions such as $X^{1/2}$, X^2, X^3, $1/X$, XY, and X/Y are easily generated with the use of logs. Multiplication becomes addition, division

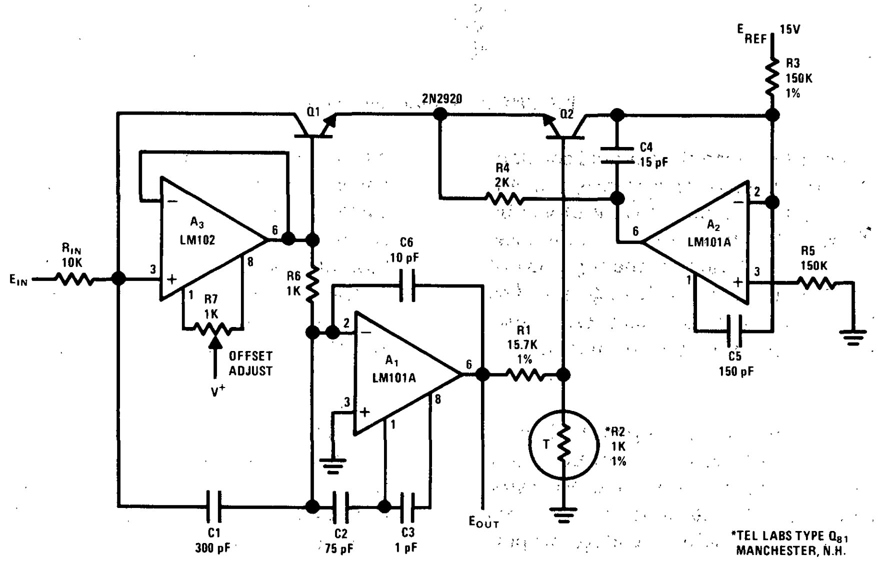

FIGURE 2. Fast Log Generator

The circuit shown in Figure 2 is two orders of magnitude faster than the previous circuit and has a dynamic range of 80 dB. Operation is the same as the circuit in Figure 1, except the configuration optimizes speed rather than dynamic range. Transistor Q_1 is diode connected to allow the use of feedforward compensation[1] on an LM101A operational amplifier. This compensation extends the bandwidth to 10 MHz and increases the slew rate. To prevent errors due to the finite h_{FE} of Q_1 and the bias current of the LM101A, an LM102 voltage follower buffers the base current and input current. Although the log circuit will operate without the LM102, accuracy will degrade at low input currents. Amplifier A_2 is also compensated for maximum bandwidth. As with the previous log converter, R_1 and R_2 control the sensitivity; and R_3 controls the zero crossing of

becomes subtraction and powers become gain coefficients of log terms. Figure 4 shows a circuit whose output is the cube of the input. Actually, any power function is available from this circuit by changing the values of R_9 and R_{10} in accordance with the expression:

$$E_{OUT} = E_{IN}^{\frac{16.7\,R_9}{R_9 + R_{10}}} \qquad (7)$$

Note that when log and anti-log circuits are used to perform an operation with a linear output, no temperature compensating resistors at all are needed. If the log and anti-log transistors are at the same temperature, gain changes with temperature cancel. It is a good idea to use a heat sink which couples the two transistors to minimize thermal gradients. A 1°C temperature difference between the log and anti-log transistors results in a 0.3% error. Also, in the log converters, a 1°C difference between the log transistors and the compensating resistor results in a 0.3% error.

Either of the circuits in Figures 1 or 2 may be used as dividers or reciprocal generators. Equation 3 shows the outputs of the log generators are actually the ratio of two currents: the input current and the current through R_3. When used as a log generator, the current through R_3 was held constant by connecting R_3 to a fixed voltage. Hence, the output was just the log of the input. If R_3 is driven by an input voltage, rather than the 15V reference, the output of the log generator is the log ratio of the input current to the current through R_3. The anti-log of this voltage is the quotient. Of course, if the divisor is constant, the output is the reciprocal.

A complete one quadrant multiplier/divider is shown in Figure 5. It is basically the log generator shown in Figure 1 driving the anti-log generator shown in Figure 3. The log generator output from A_1 drives the base of Q_3 with a voltage proportional to the log of E_1/E_2. Transistor Q_3 adds a voltage proportional to the log of E_3 and drives the anti-log transistor, Q_4. The collector current of Q_4 is converted to an output voltage by A_4 and R_7, with the scale factor set by R_7 at $E_1 E_3/10E_2$.

Measurement of transistor current gains over a wide range of operating currents is an application particularly suited to log multiplier/dividers. Using the circuit in Figure 5, PNP current gains can be measured at currents from 0.4 μA to 1 mA. The collector current is the input signal to A_1, the base current is the input signal to A_2, and a fixed voltage to R_5 sets the scale factor. Since A_2 holds the base at ground, a single resistor from the emitter to the positive supply is all that is needed to establish the operating current. The output is proportional to collector current divided by base current, or h_{FE}.

In addition to their application in performing functional operations, log generators can provide a significant increase in the dynamic range of signal processing systems. Also, unlike a linear system, there is no loss in accuracy or resolution when the

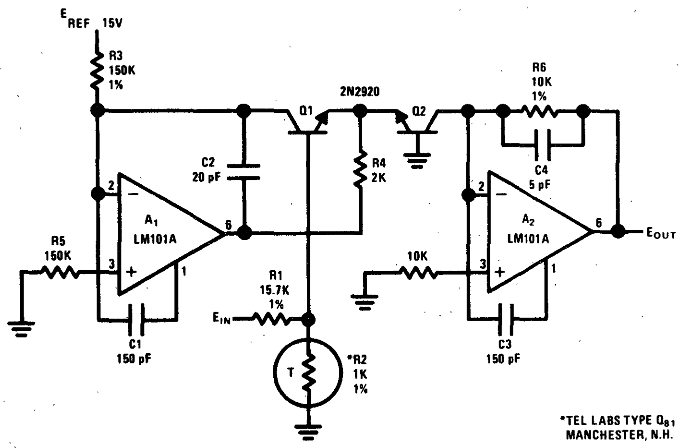

FIGURE 3. Anti-log Generator

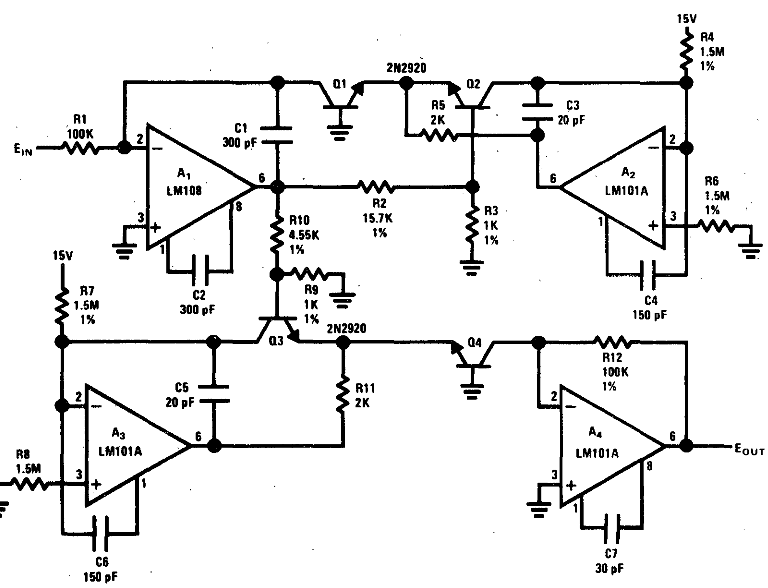

FIGURE 4. Cube Generator

input signal is small compared to full scale. Over most of the dynamic range, the accuracy is a percent-of-signal rather than a percent-of-full-scale. For example, using log generators, a simple meter can display signals with 100 dB dynamic range or an oscilloscope can display a 10 mV and 10V pulse simultaneously. Obviously, without the log generator, the low level signals are completely lost.

To achieve wide dynamic range with high accuracy, the input operational amplifier necessarily must have low offset voltage, bias current and offset current. The LM108 has a maximum bias current of *3 nA* and offset current of *400 pA* over a −55°C to 125°C temperature range. By using equal source resistors, only the offset current of the LM108 causes an error. The offset current of the LM108 is as low as many FET amplifiers. Further, it has a low and constant temperature coefficient rather than doubling every 10°C. This results in greater accuracy over temperature than can be achieved with FET amplifiers. The offset voltage may be zeroed, if necessary, to improve accuracy with low input voltages.

The log converters are low level circuits and some care should be taken during construction. The input leads should be as short as possible and the input circuitry guarded against leakage currents. Solder residues can easily conduct leakage currents, therefore circuit boards should be cleaned before use. High quality glass or mica capacitors should be used on the inputs to minimize leakage currents. Also, when the +15V supply is used as a reference, it must be well regulated.

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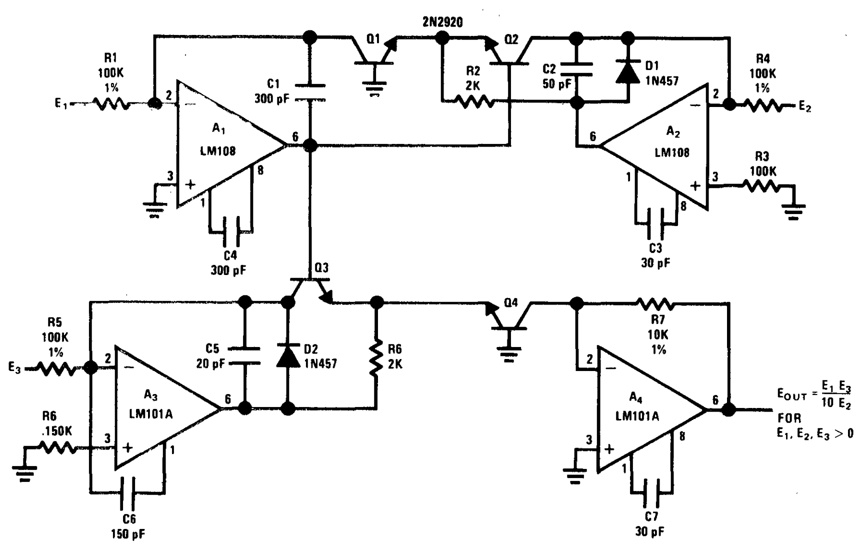
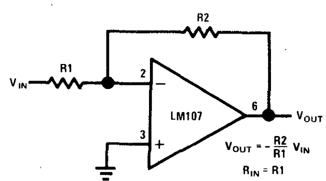


FIGURE 5. Multiplier/Divider

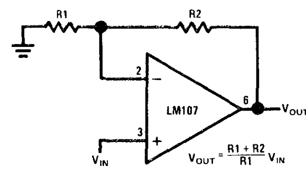
February 1970

op amp circuit collection

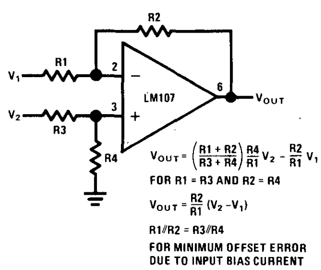
section 1 — basic circuits



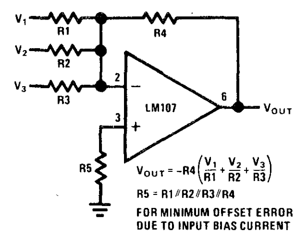
Inverting Amplifier



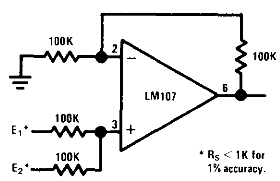
Non-Inverting Amplifier



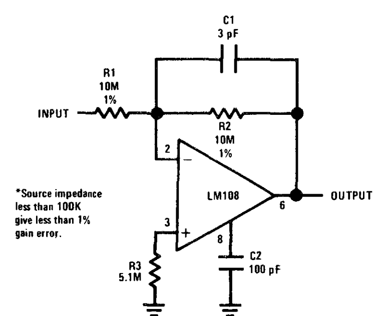
Difference Amplifier



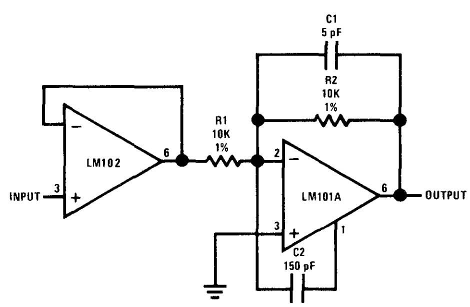
Inverting Summing Amplifier



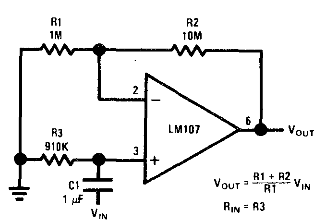
Non-Inverting Summing Amplifier



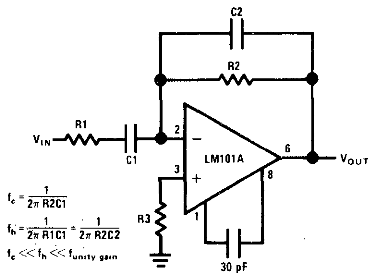
Inverting Amplifier with High Input Impedance



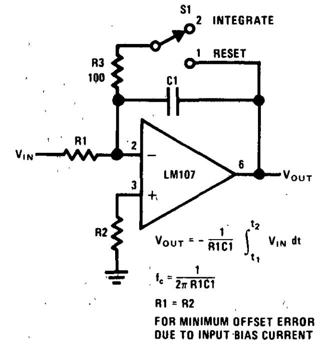
Fast Inverting Amplifier With High Input Impedance



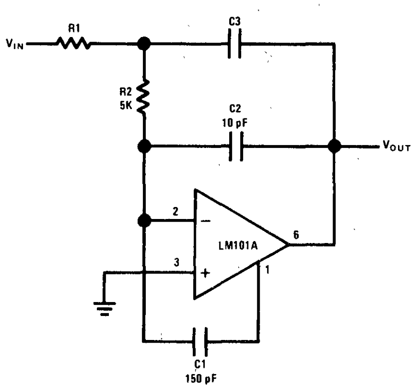
Non-Inverting AC Amplifier



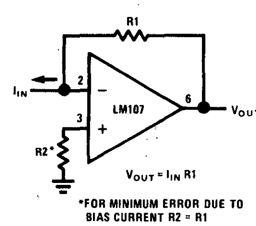
Practical Differentiator



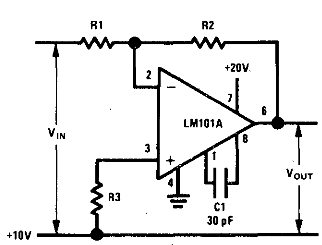
Integrator



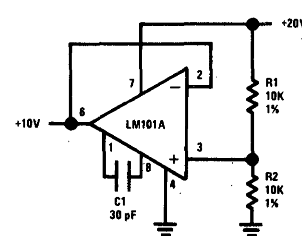
Fast Integrator



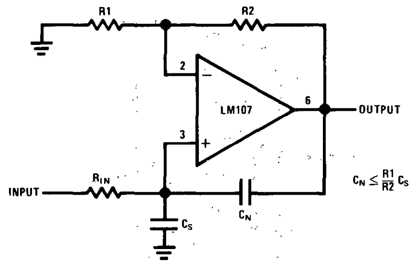
Current to Voltage Converter



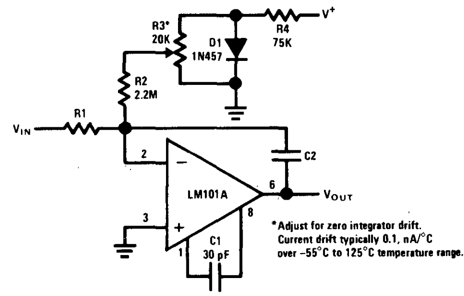
Circuit for Operating the LM101 without a Negative Supply



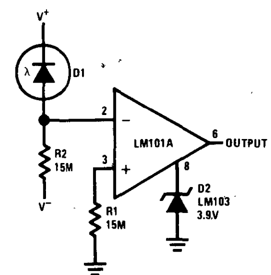
Circuit for Generating the Second Positive Voltage



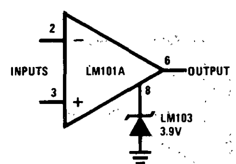
Neutralizing Input Capacitance to Optimize Response Time



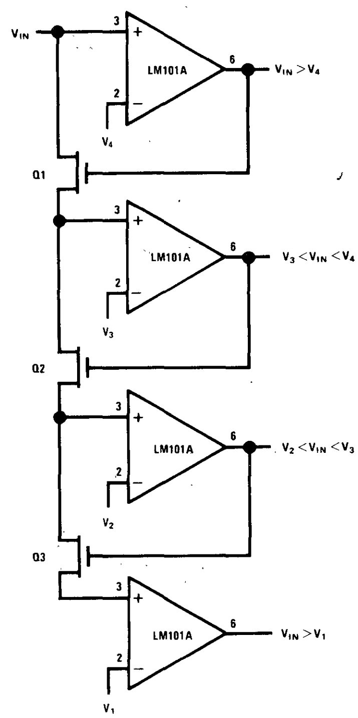
Integrator with Bias Current Compensation



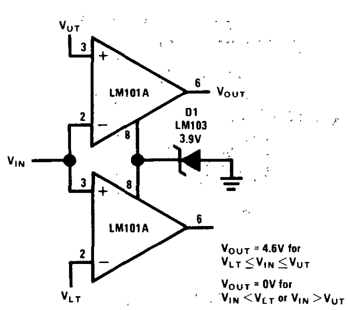
Threshold Detector for Photodiodes



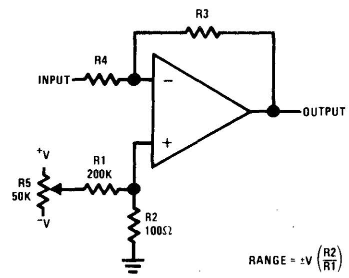
Voltage Comparator for Driving DTL or TTL Integrated Circuits



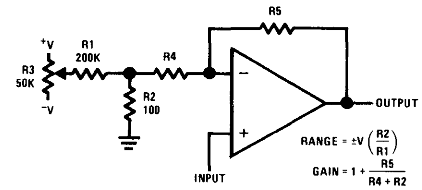
Multiple Aperture Window Discriminator



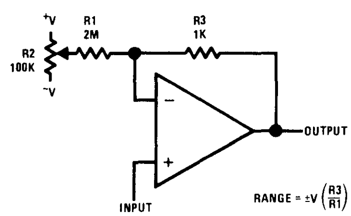
Double-Ended Limit Detector



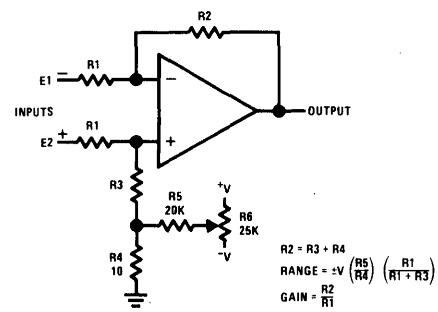
Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element



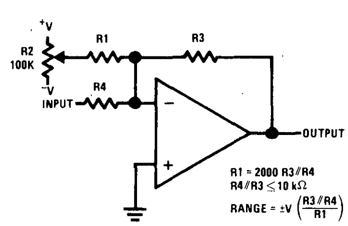
Offset Voltage Adjustment for Non-Inverting Amplifiers



Offset Voltage Adjustment for Voltage Followers

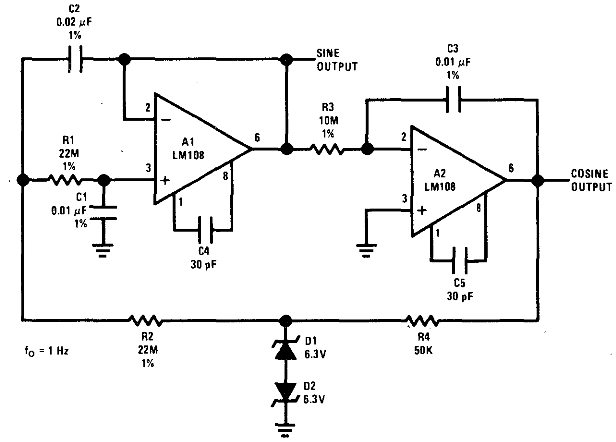


Offset Voltage Adjustment for Differential Amplifiers

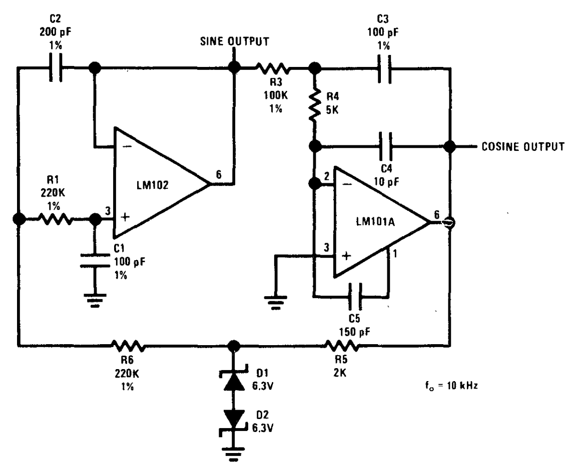


Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less

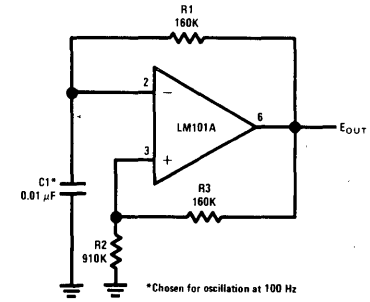
section 2 — signal generation



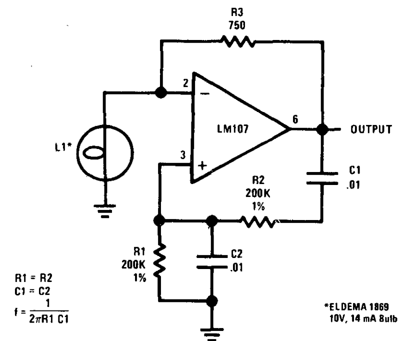
Low Frequency Sine Wave Generator with Quadrature Output



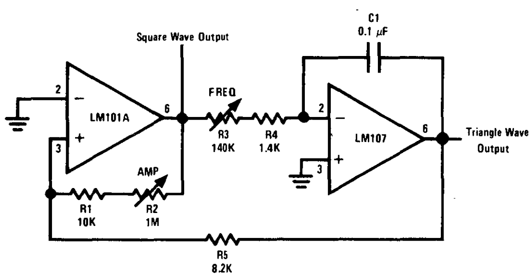
High Frequency Sine Wave Generator with Quadrature Output



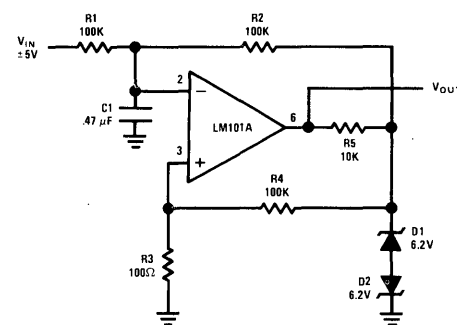
Free-Running Multivibrator



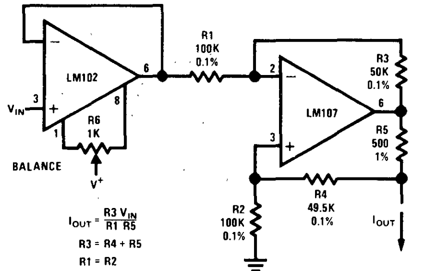
Wein Bridge Sine Wave Oscillator



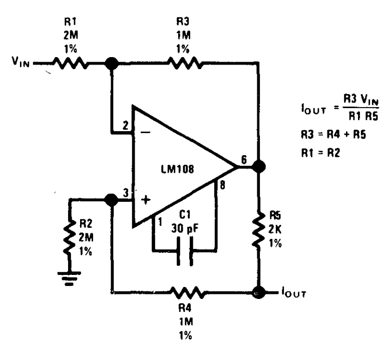
Function Generator



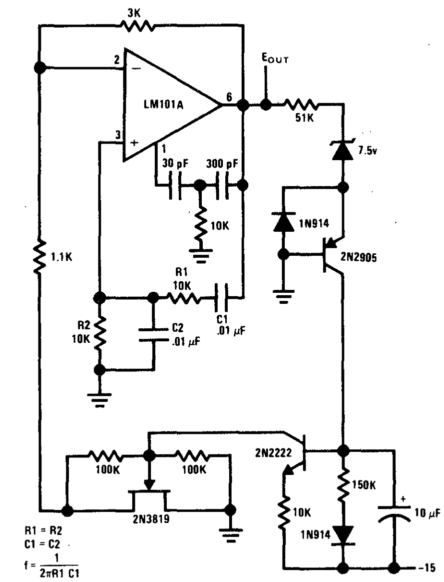
Pulse Width Modulator



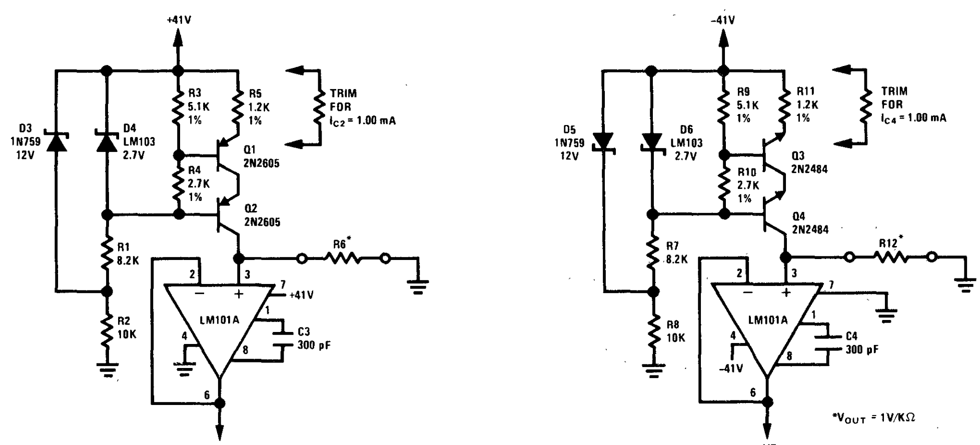
Bilateral Current Source



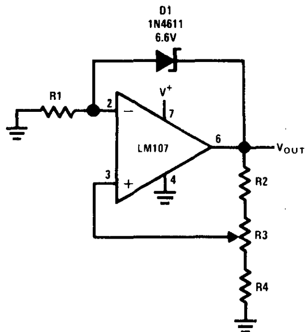
Bilateral Current Source



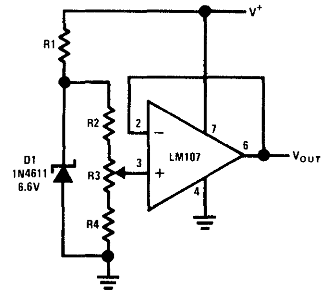
Wein Bridge Oscillator with FET Amplitude Stabilization



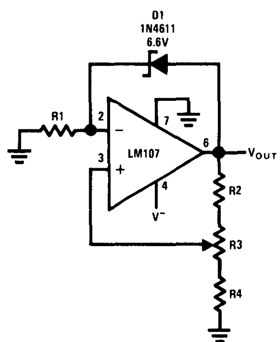
Low Power Supply for Integrated Circuit Testing



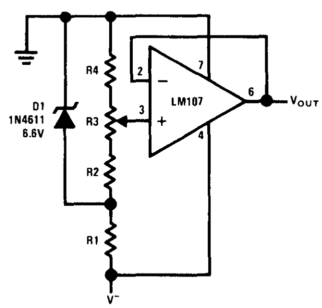
Positive Voltage Reference



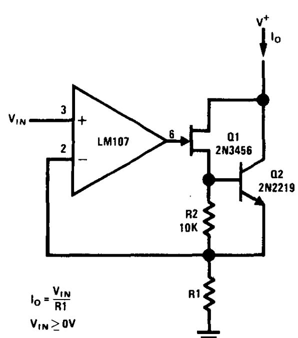
Positive Voltage Reference



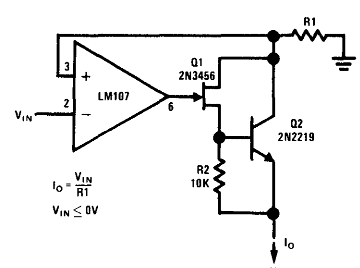
Negative Voltage Reference



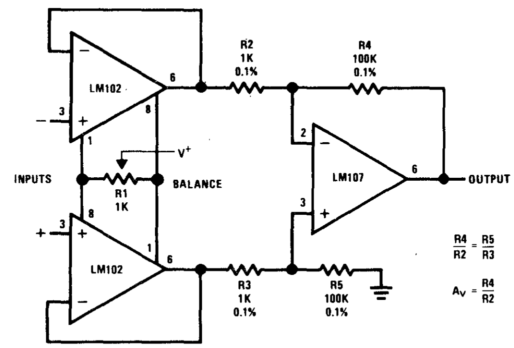
Negative Voltage Reference



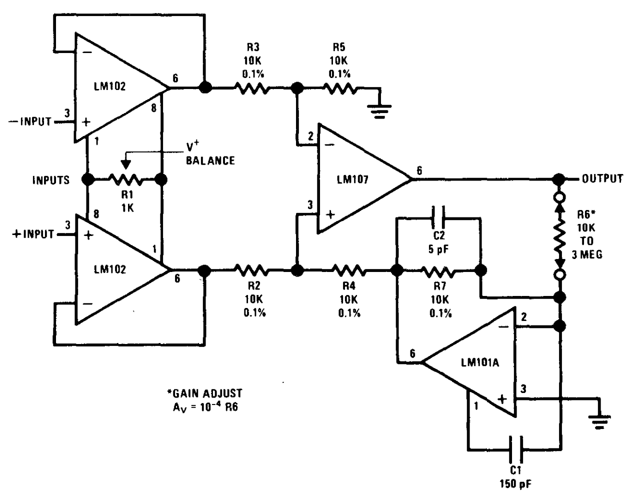
Precision Current Sink



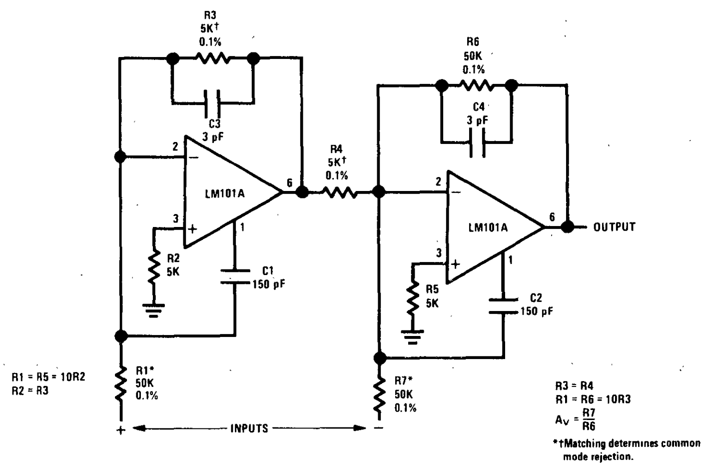
Precision Current Source



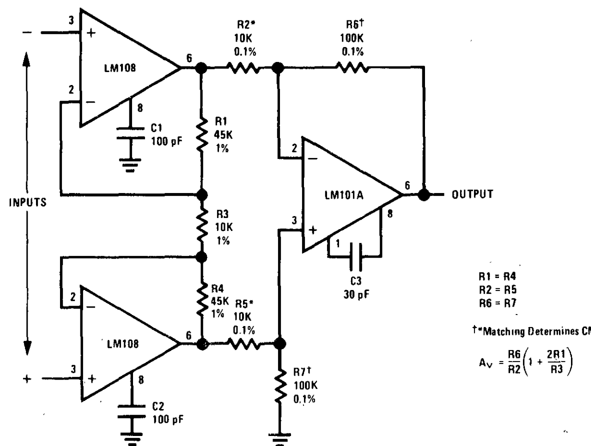
Differential-Input Instrumentation Amplifier



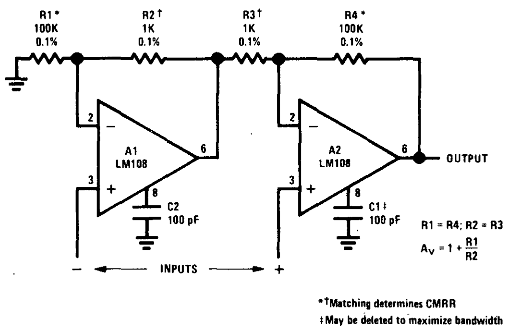
Variable Gain, Differential-Input Instrumentation Amplifier



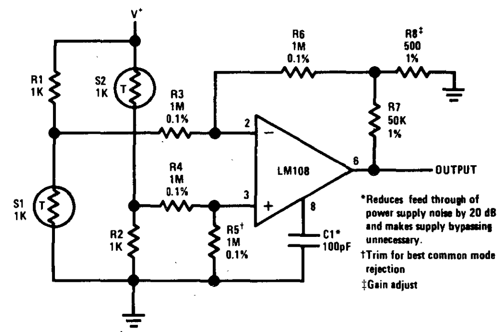
Instrumentation Amplifier with ±100 Volt Common Mode Range



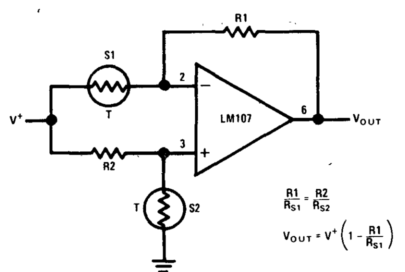
Differential Input Instrumentation Amplifier with High Common Mode Rejection



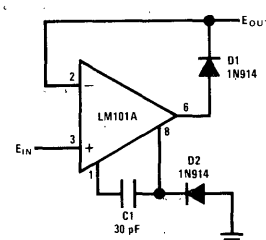
High Input Impedance Instrumentation Amplifier



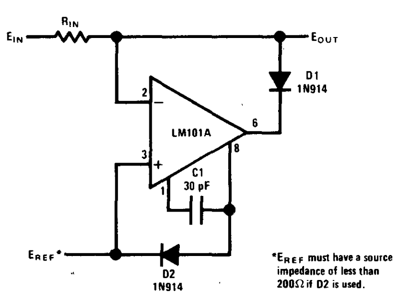
Bridge Amplifier with Low Noise Compensation



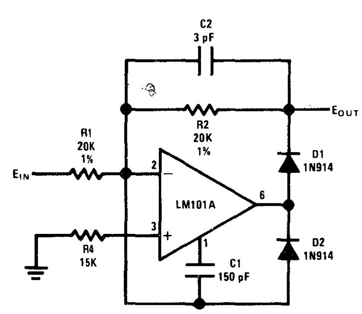
Bridge Amplifier



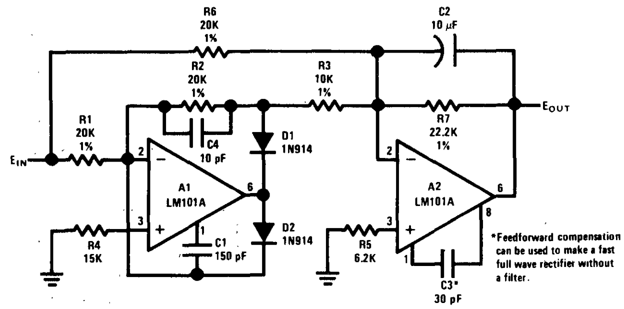
Precision Diode



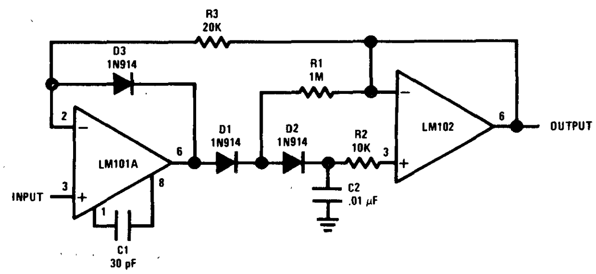
Precision Clamp



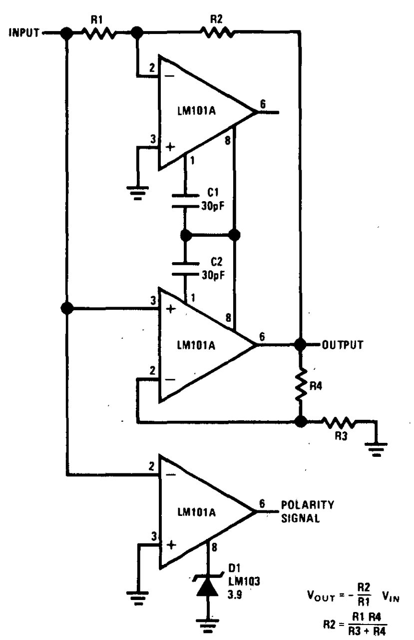
Fast Half Wave Rectifier



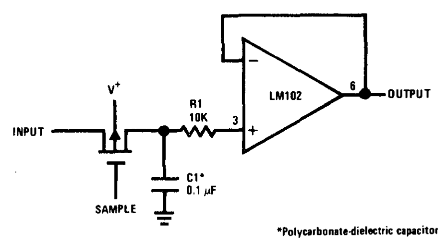
Precision AC to DC Converter



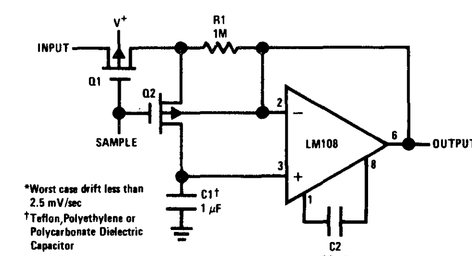
Low Drift Peak Detector



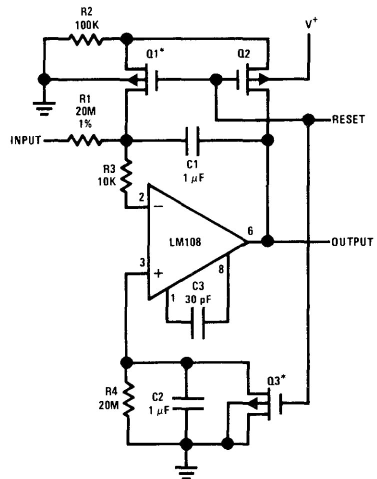
Absolute Value Amplifier with Polarity Detector



Sample and Hold



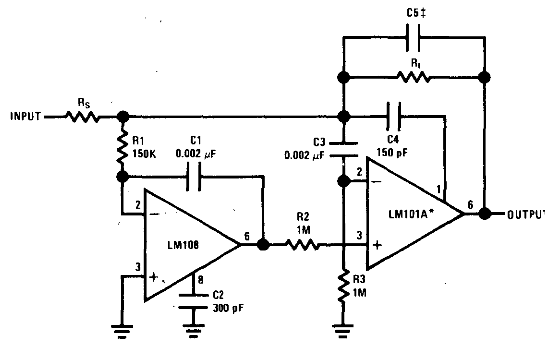
Sample and Hold



*Q1 and Q3 should not have internal gate-protection diodes.

Worst case drift less than 500 μV/sec over −55°C to +125°C.

Low Drift Integrator

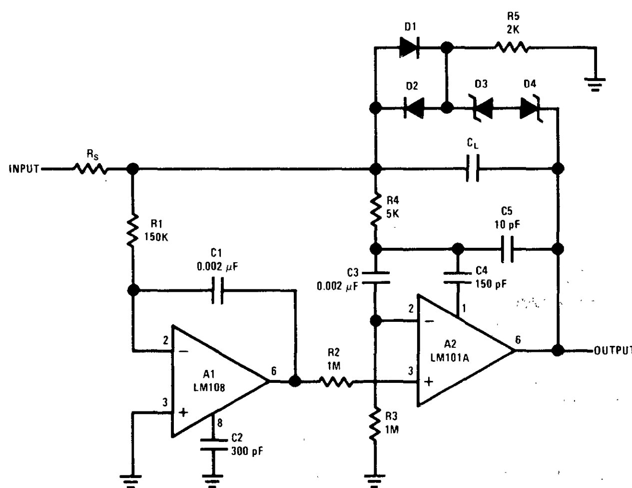


* In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

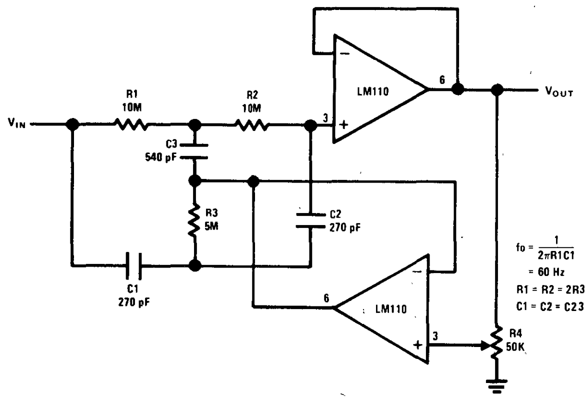
† Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

‡ $C5 = \frac{6 \times 10^{-8}}{R_f}$

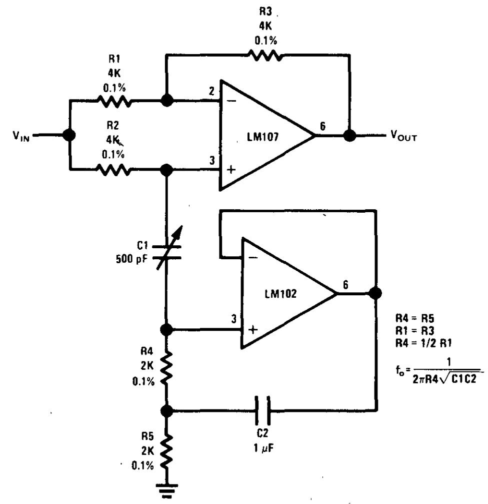
Fast† Summing Amplifier with Low Input Current



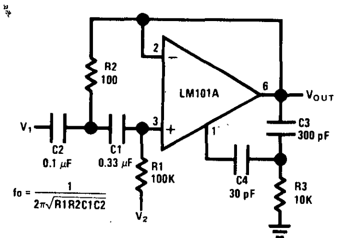
Fast Integrator with Low Input Current



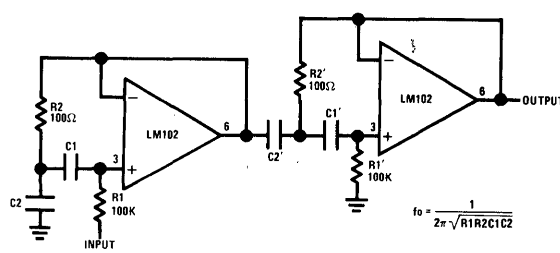
Adjustable Q Notch Filter



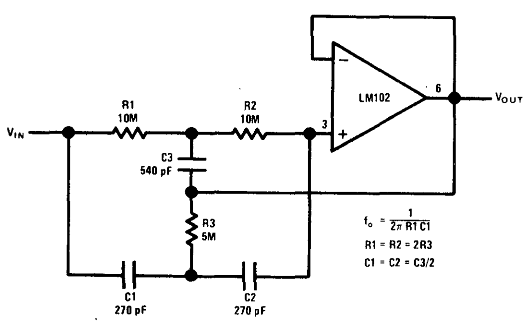
Easily Tuned Notch Filter



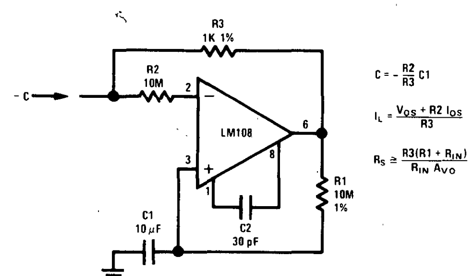
Tuned Circuit



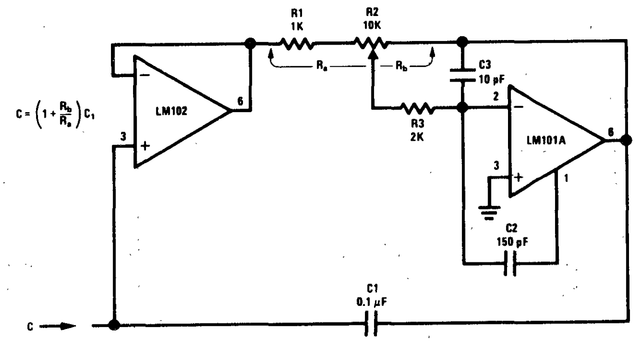
Two-Stage Tuned Circuit



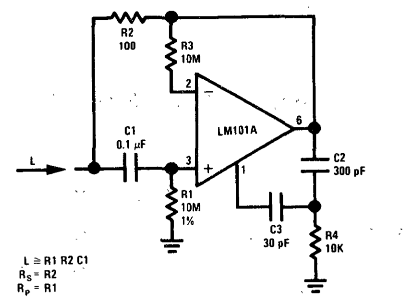
High Q Notch Filter



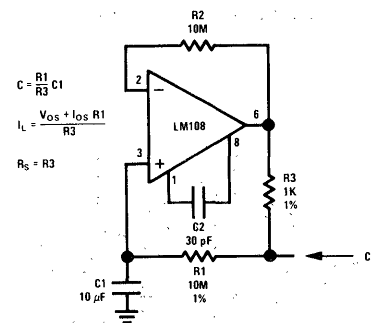
Negative Capacitance Multiplier



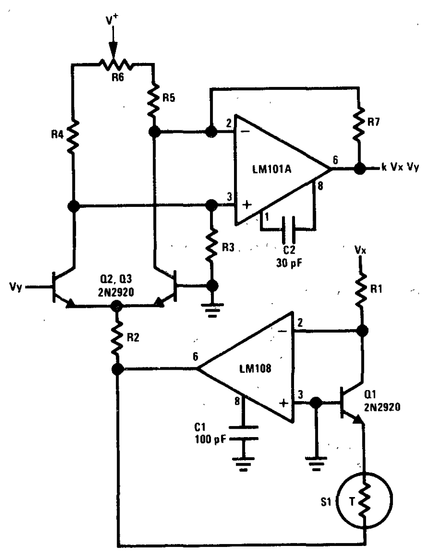
Variable Capacitance Multiplier



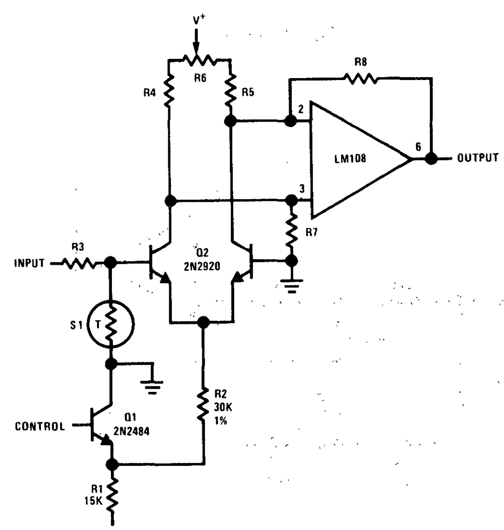
Simulated Inductor



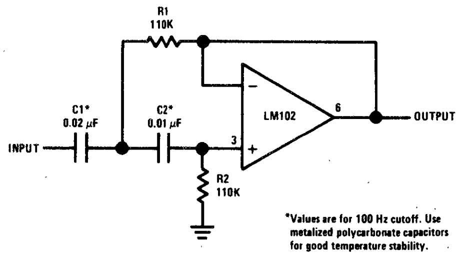
Capacitance Multiplier



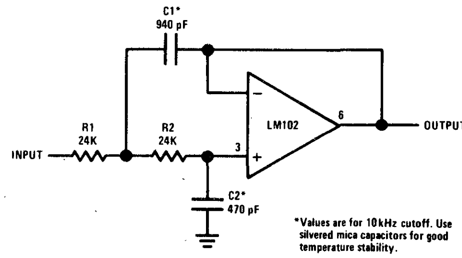
Two Quadrant Multiplier



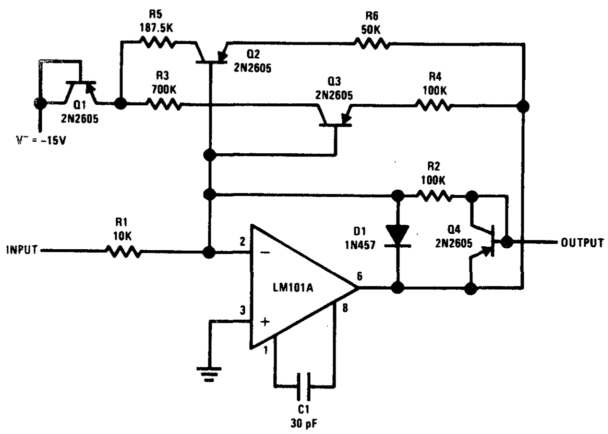
Voltage Controlled Gain Circuit



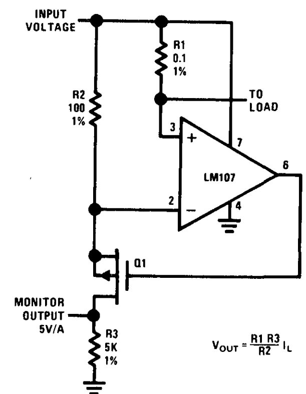
High Pass Active Filter



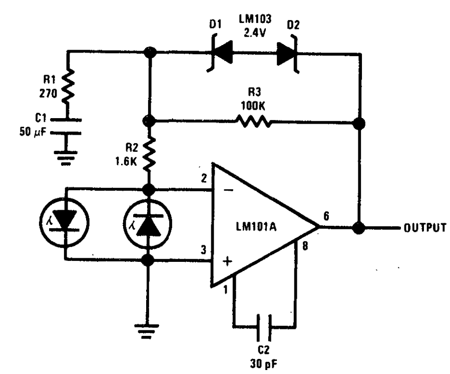
Low Pass Active Filter



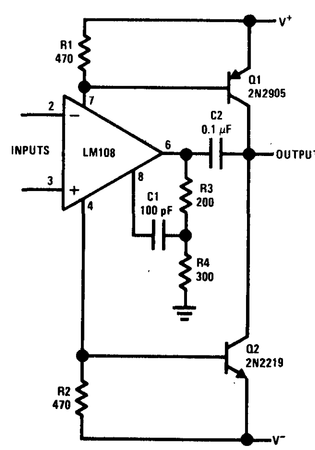
Nonlinear Operational Amplifier with Temperature Compensated Breakpoints



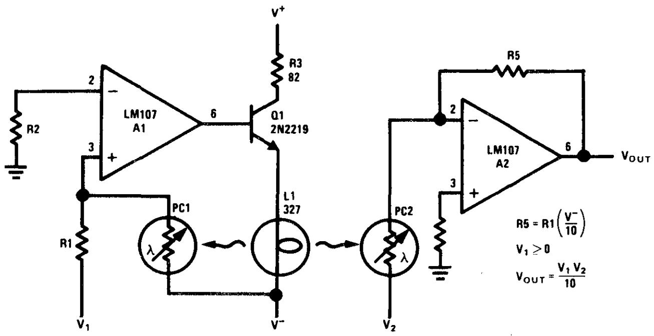
Current Monitor



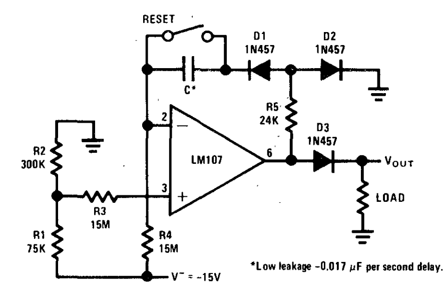
Saturating Servo Preamplifier with Rate Feedback



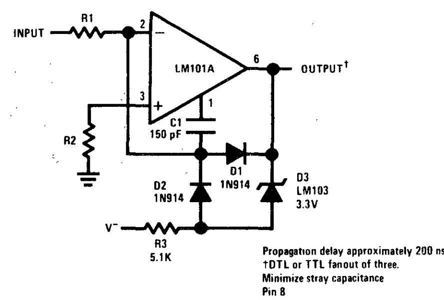
Power Booster



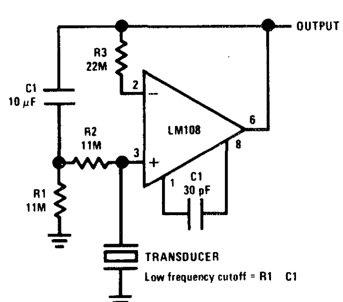
Analog Multiplier



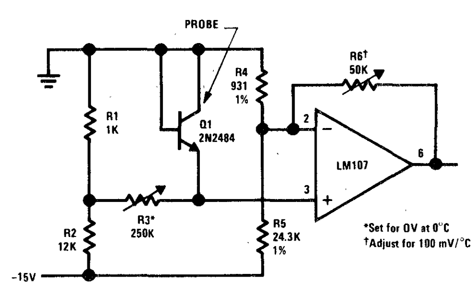
Long Interval Timer



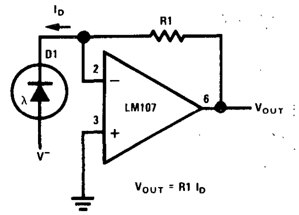
Fast Zero Crossing Detector



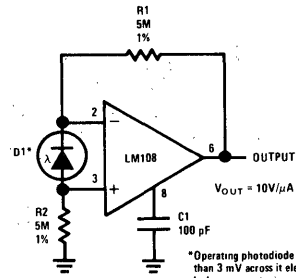
Amplifier for Piezoelectric Transducer



Temperature Probe

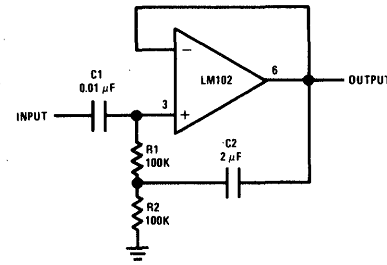


Photodiode Amplifier

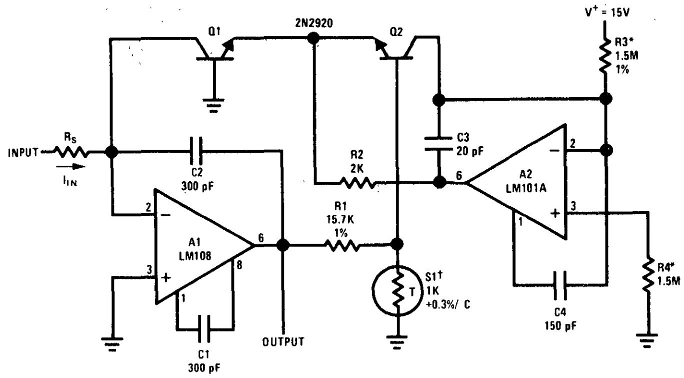


*Operating photodiode with less than 3 mV across it eleminates leakage currents.

Photodiode Amplifier



High Input Impedance AC Follower

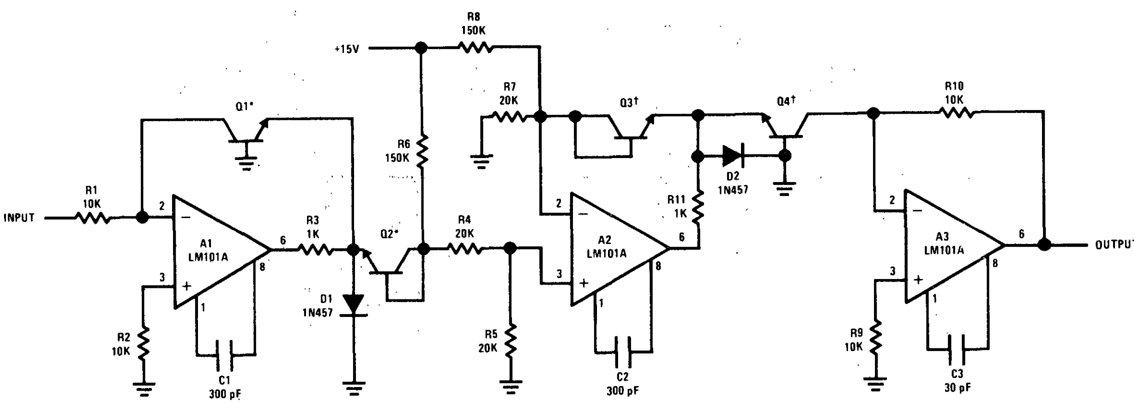


$10\ nA < I_{IN} < 1\ mA$
Sensitivity is 1V per decade.

†Available from Tel Labs, Inc., Manchester, N.H., Type Q81.

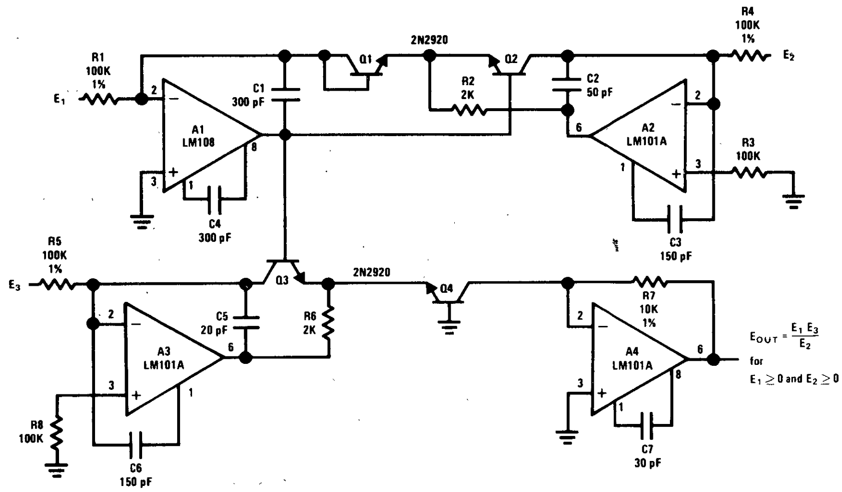
*Determines current for zero crossing on output: 10 μA as shown.

Temperature Compensated Logrithmic Converter

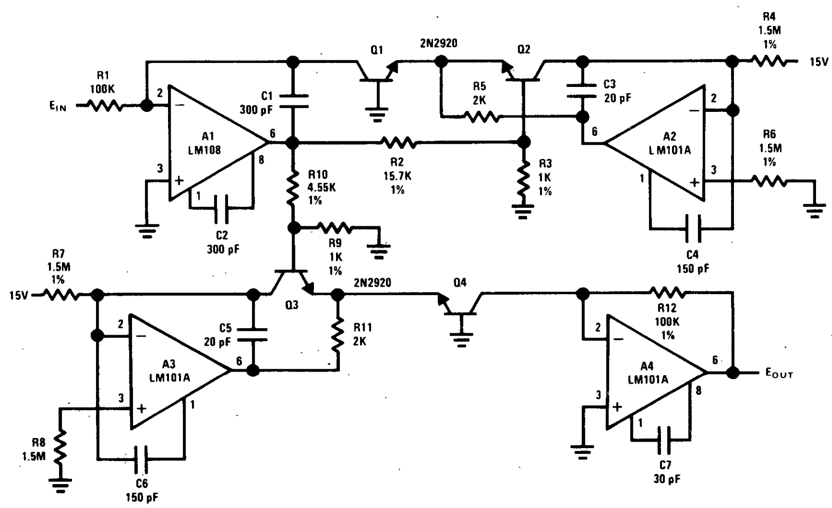


* †2N3728 matched pairs

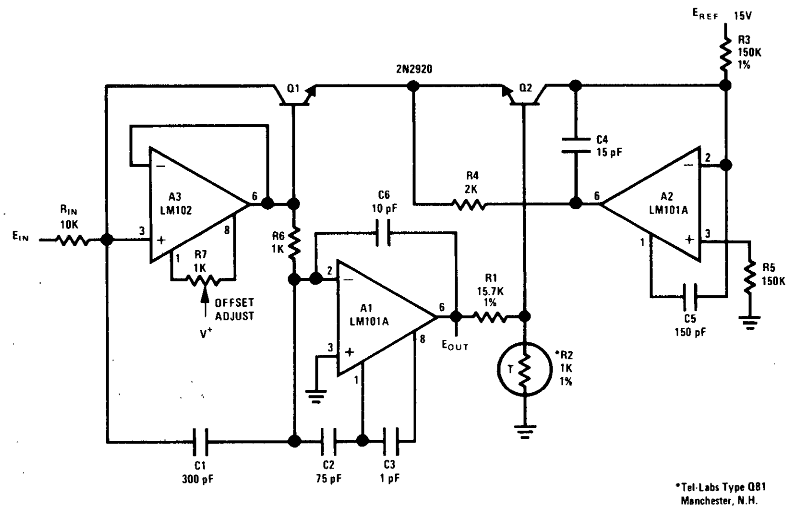
Root Extractor



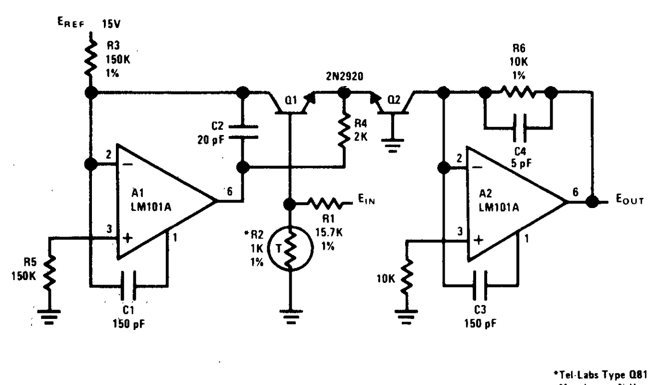
Multiplier/Divider



Cube Generator



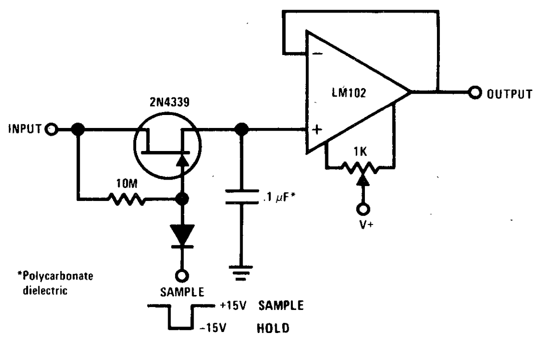
Fast Log Generator



Anti-log Generator

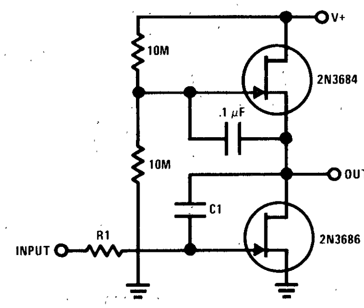
February 1970

FET circuit applications



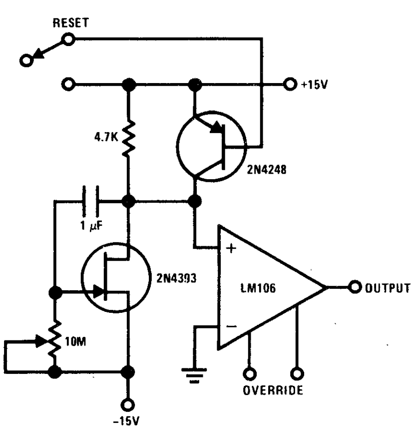
Sample and Hold With Offset Adjustment

The 2N4339 JFET was selected because of its low I_{GSS} (<100 pA), very-low $I_{D(OFF)}$ (<50 pA) and low pinchoff voltage. Leakages of this level put the burden of circuit performance on clean, solder-resin free, low leakage circuit layout.



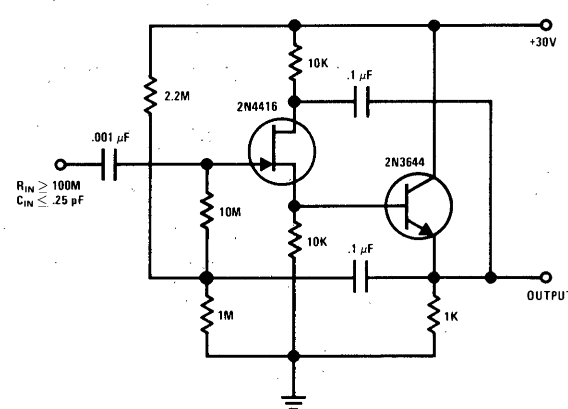
JFET AC Coupled Integrator

This circuit utilizes the "μ-amp" technique to achieve very high voltage gain. Using C_1 in the circuit as a Miller integrator, or capacitance multiplier, allows this simple circuit to handle very long time constants.



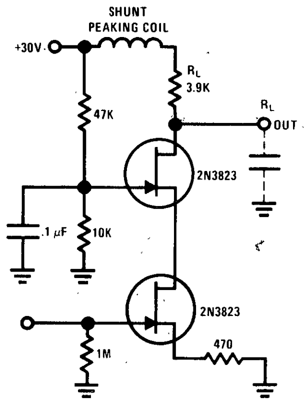
Long Time Comparator

The 2N4393 is operated as a Miller integrator. The high Y_{fs} of the 2N4393 (over 12,000 μmhos @ 5 mA) yields a stage gain of about 60. Since the equivalent capacitance looking into the gate is C times gain and the gate source resistance can be as high as 10 MΩ, time constants as long as a minute can be achieved.

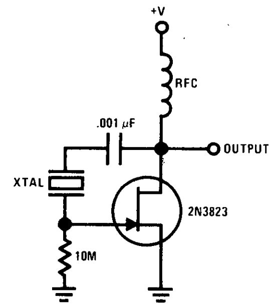


Ultra-High Z_{IN} AC Unity Gain Amplifier

Nothing is left to chance in reducing input capacitance. The 2N4416, which has low capacitance in the first place, is operated as a source follower with bootstrapped gate bias resistor and drain. Any input capacitance you get with this circuit is due to poor layout techniques.



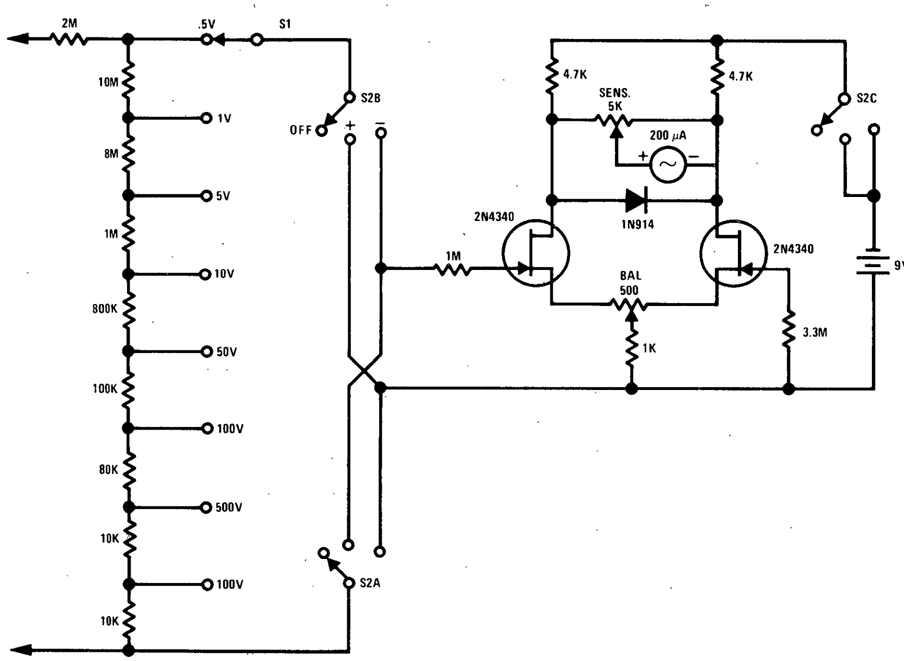
FET Cascode Video Amplifier



JFET Pierce Crystal Oscillator

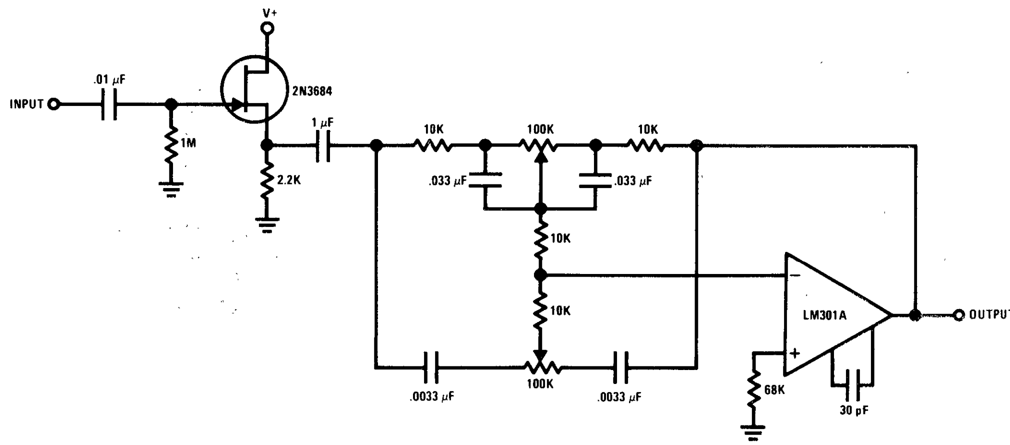
The FET cascode video amplifier features very low input loading and reduction of feedback to almost zero. The 2N3823 is used because of its low capacitance and high Y_{fs}. Bandwidth of this amplifier is limited by R_L and load capacitance.

The JFET Pierce crystal oscillator allows a wide frequency range of crystals to be used without circuit modification. Since the JFET gate does not load the crystal, good Q is maintained thus insuring good frequency stability.



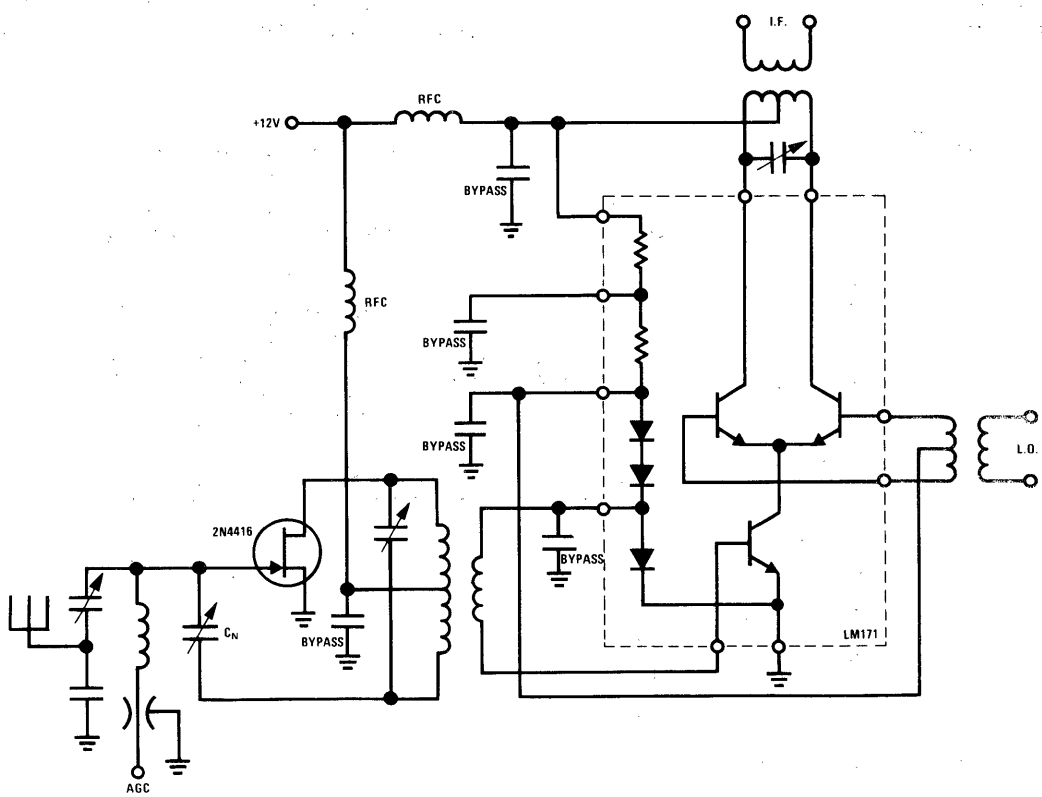
FETVM—FET Voltmeter

This FETVM replaces the function of the VTVM while at the same time ridding the instrument of the usual line cord. In addition, drift rates are far superior to vacuum tube circuits allowing a 0.5 volt full scale range which is impractical with most vacuum tubes. The low-leakage, low-noise 2N4340 is an ideal device for this application.



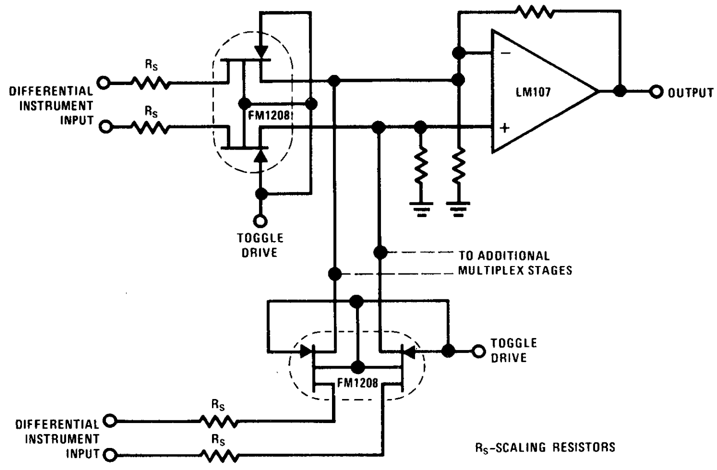
HI-FI Tone Control Circuit (High Z Input)

The 2N3684 JFET provides the function of a high input impedance and low noise characteristics to buffer an op amp-operated feedback type tone control circuit.



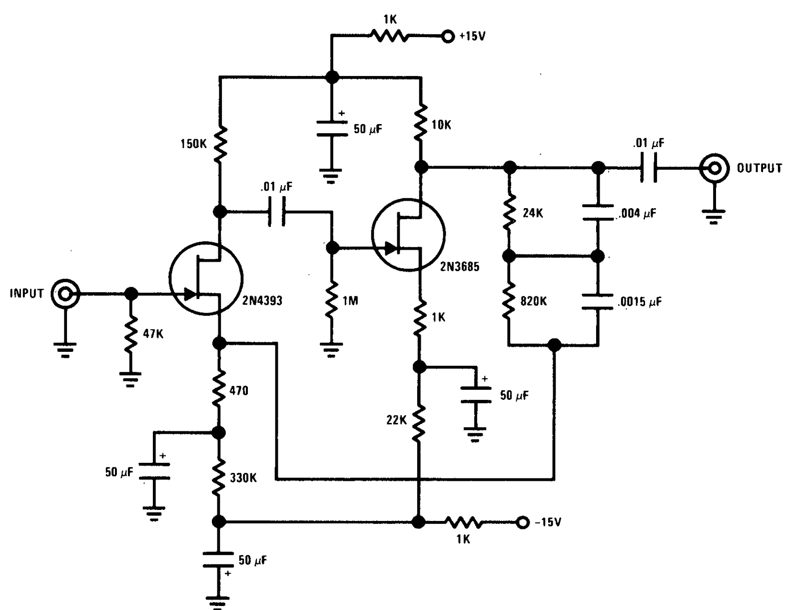
100 MHz Converter

The 2N4416 JFET will provide noise figures of less than 3 dB and power gain of greater than 20 dB. The JFETs outstanding low crossmodulation and low intermodulation distortion provides an ideal characteristic for an input stage. The output feeds into an LM171 used as a balanced mixer. This configuration greatly reduces L.O. radiation both into the antenna and into the I.F. strip and also reduces RF signal feedthrough.



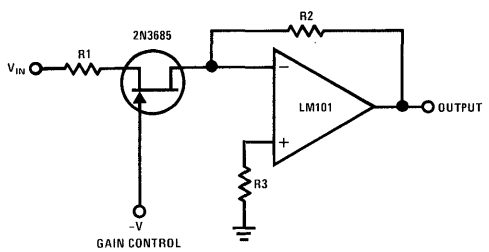
Differential Analog Switch

The FM1208 monolithic dual is used in a differential multiplexer application where $R_{DS(ON)}$ should be closely matched. Since $R_{DS(ON)}$ for the monolithic dual tracks at better than ±1% over wide temperature ranges (–25 to +125°C), this makes it an unusual but ideal choice for an accurate multiplexer. This close tracking greatly reduces errors due to common mode signals.



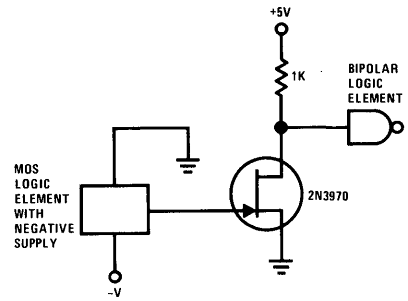
Magnetic-Pickup Phono Preamplifier

This preamplifier provides proper loading to a reluctance phono cartridge. It provides approximately 35 dB of gain at 1 kHz (2.2 mV input for 100 mV output), it features S + N/N ratio of better than –70 dB (referenced to 10 mV input at 1 kHz) and has a dynamic range of 84 dB (referenced to 1 kHz). The feedback provides for RIAA equalization.



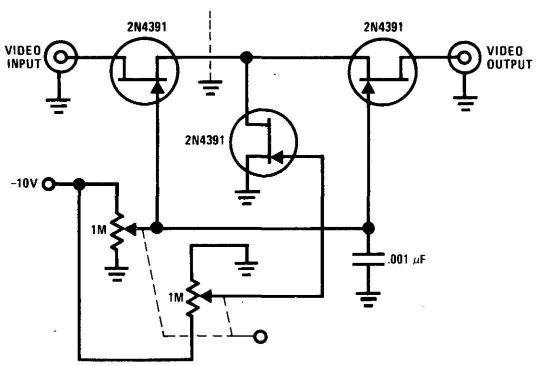
Variable Attenuator

The 2N3685 acts as a voltage variable resistor with an $R_{DS(ON)}$ of 800Ω max. The 2N3685 JFET will have linear resistance over several decades of resistance providing an excellent electronic gain control.



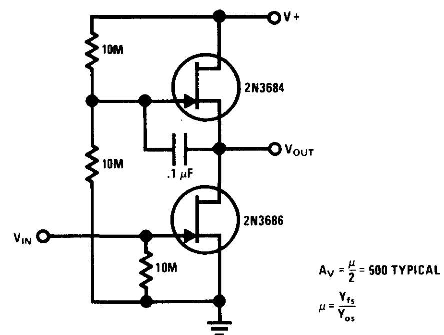
Negative to Positive Supply Logic Level Shifter

This simple circuit provides for level shifting from any logic function (such as MOS) operating from minus to ground supply to any logic level (such as TTL) operating from a plus to ground supply. The 2N3970 provides a low $r_{ds(ON)}$ and fast switching times.



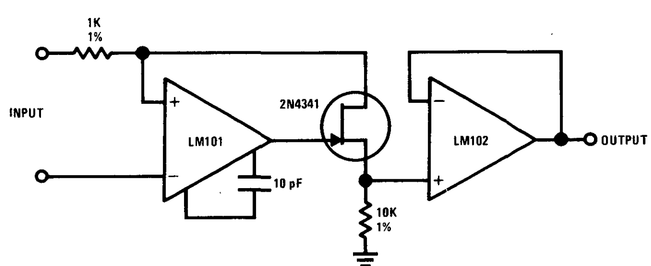
Voltage Controlled Variable Gain Amplifier

The 2N4391 provides a low $R_{DS(ON)}$ (less than 30Ω). The tee attenuator provides for optimum dynamic linear range for attenuation and if complete turnoff is desired, attenuation of greater than 100 dB can be obtained at 10 MHz providing proper RF construction techniques are employed.



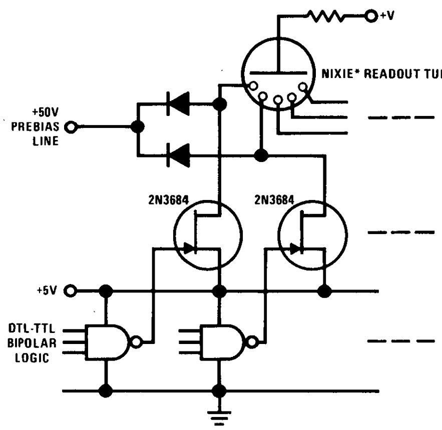
Ultra-High Gain Audio Amplifier

Sometimes called the "JFET μ amp," this circuit provides a very low power, high gain amplifying function. Since μ of a JFET increases as drain current decreases, the lower drain current is, the more gain you get. You do sacrifice input dynamic range with increasing gain, however.



Level-Shifting-Isolation Amplifier

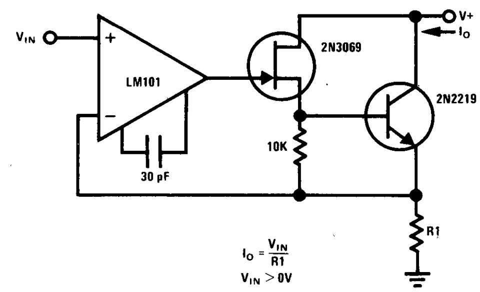
The 2N4341 JFET is used as a level shifter between two op amps operated at different power supply voltages. The JFET is ideally suited for this type of application because $I_D = I_S$.



*Trademark of the Burroughs Corp.

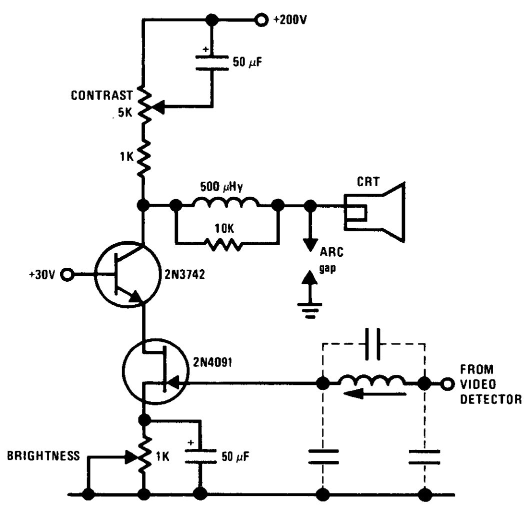
FET Nixie* Drivers

The 2N3684 JFETs are used as Nixie tube drivers. Their V_P of 2-5 volts ideally matches DTL-TTL logic levels. Diodes are used to a +50 volt prebias line to prevent breakdown of the JFETs. Since the 2N3684 is in a TO-72 (4 lead TO-18) package, none of the circuit voltages appear on the can. The JFET is immune to almost all of the failure mechanisms found in bipolar transistors used for this application.



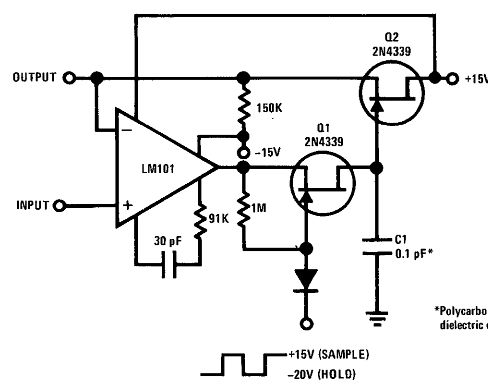
Precision Current Sink

The 2N3069 JFET and 2N2219 bipolar have inherently high output impedance. Using R_1 as a current sensing resistor to provide feedback to the LM101 op amp provides a large amount of loop gain for negative feedback to enhance the true current sink nature of this circuit. For small current values, the 10k resistor and 2N2219 may be eliminated if the source of the JFET is connected to R_1.



JFET–Bipolar Cascode Circuit

The JFET-Bipolar cascode circuit will provide full video output for the CRT cathode drive. Gain is about 90. The cascode configuration eliminates Miller capacitance problems with the 2N4091 JFET, thus allowing direct drive from the video detector. An m derived filter using stray capacitance and a variable inductor prevents 4.5 MHz sound frequency from being amplified by the video amplifier.



*Polycarbonate dielectric capacitor

Low Drift Sample and Hold

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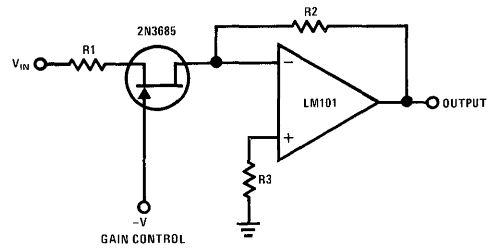

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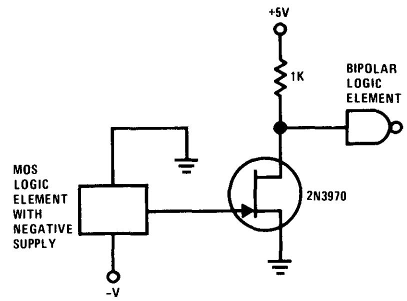

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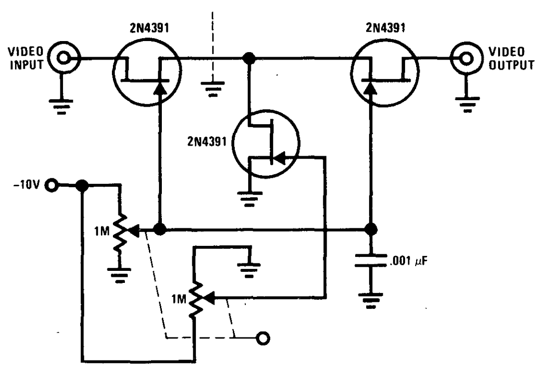

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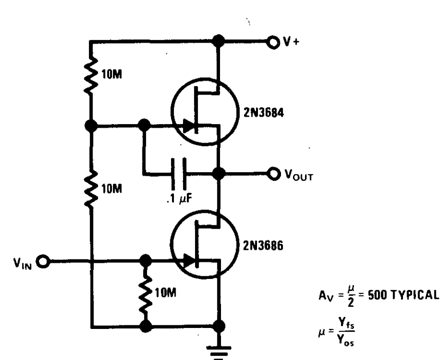

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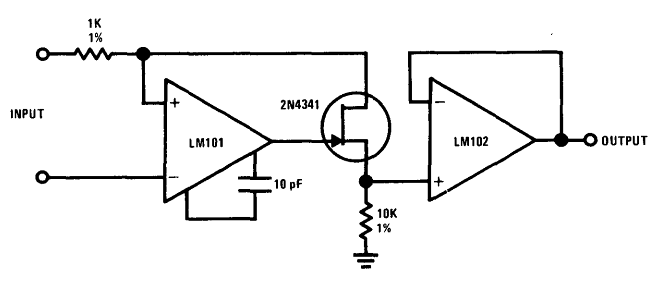

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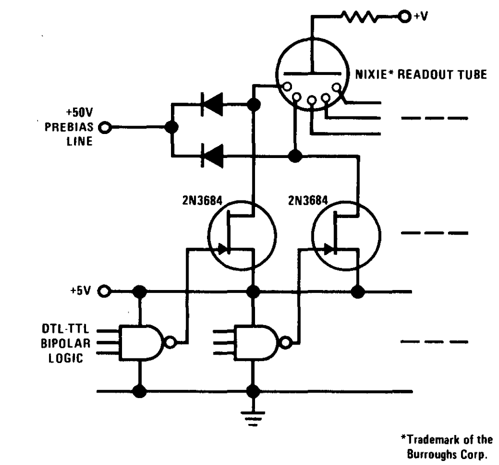

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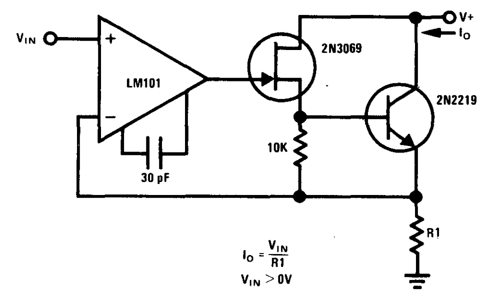

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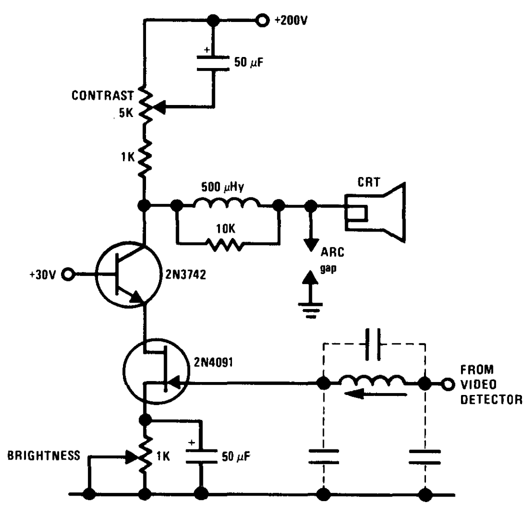

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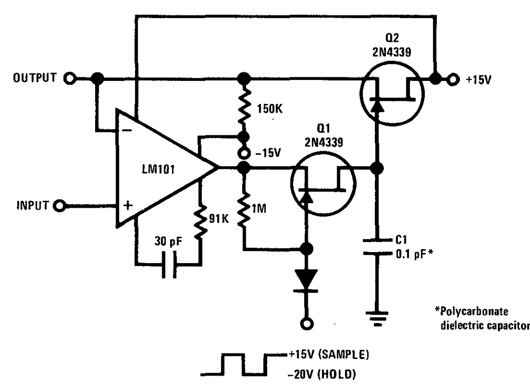

Low Drift Sample and Hold

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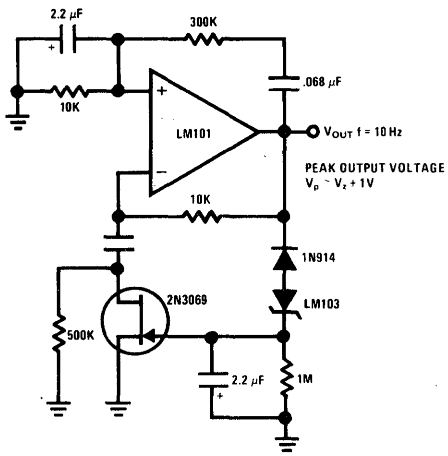
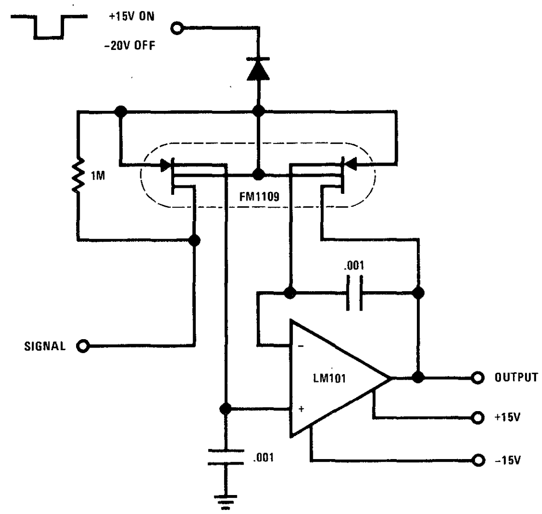


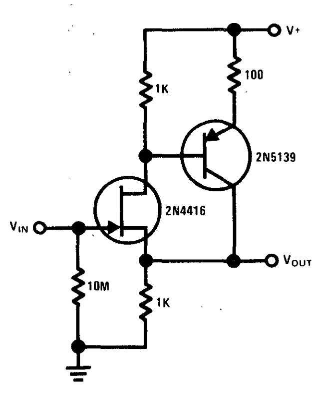
Wien Bridge Sine Wave Oscillator



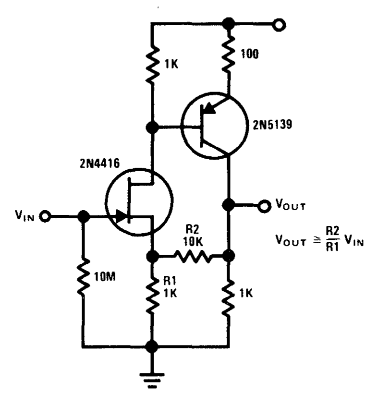
JFET Sample and Hold Circuit

The major problem in producing a low distortion, constant amplitude sine wave is getting the amplifier loop gain just right. By using the 2N3069 JFET as a voltage variable resistor in the amplifier feedback loop, this can be easily achieved. The LM103 zener diode provides the voltage reference for the peak sine wave amplitude; this is rectified and fed to the gate of the 2N3069, thus varying its channel resistance and, hence, loop gain.

The logic voltage is applied simultaneously to the sample and hold JFETs. By matching input impedance and feedback resistance and capacitance, errors due to $r_{ds(ON)}$ of the JFETs is minimized. The inherent matched $r_{ds(ON)}$ and matched leakage currents of the FM1109 monolithic dual greatly improve circuit performance.



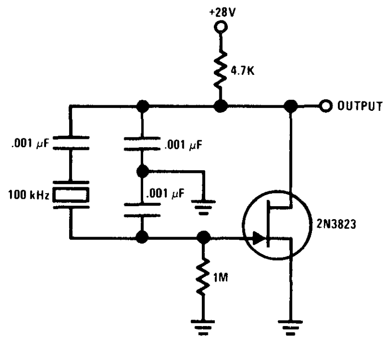
High Impedance Low Capacitance Wideband Buffer



High Impedance Low Capacitance Amplifier

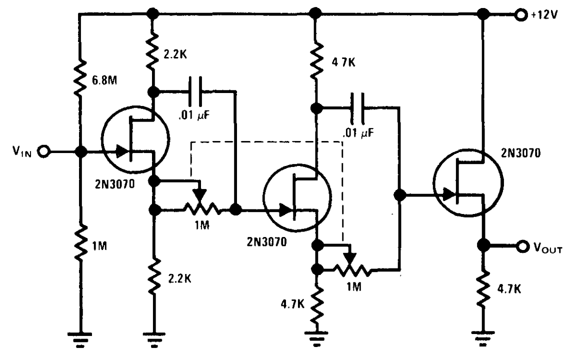
The 2N4416 features low input capacitance which makes this compound-series feedback buffer a wide-band unity gain amplifier.

This compound series-feedback circuit provides high input impedance and stable, wide-band gain for general purpose video amplifier applications.



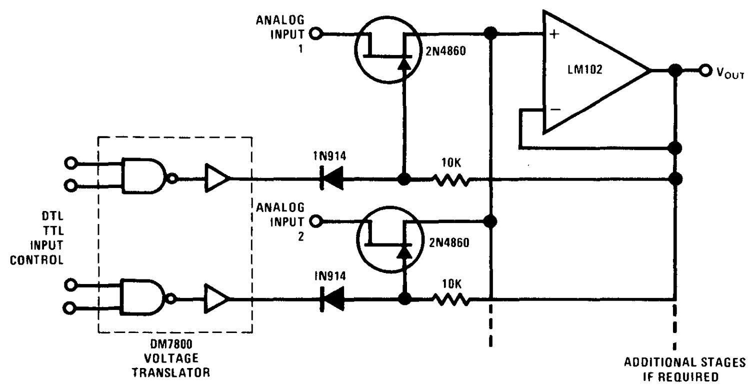
Stable Low Frequency Crystal Oscillator

This Colpitts-Crystal oscillator is ideal for low frequency crystal oscillator circuits. Excellent stability is assured because the 2N3823 JFET circuit loading does not vary with temperature.



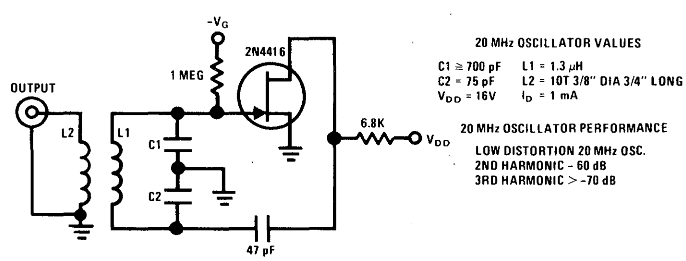
0 to 360° Phase Shifter

Each stage provides 0° to 180° phase shift. By ganging the two stages, 0° to 360° phase shift is achieved. The 2N3070 JFETs are ideal since they do not load the phase shift networks.



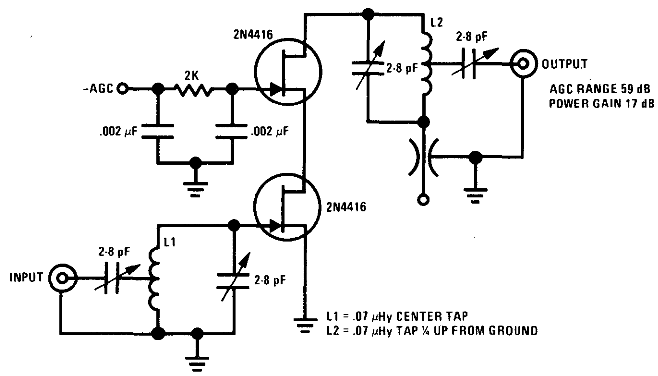
DTL-TTL Controlled Buffered Analog Switch

This analog switch uses the 2N4860 JFET for its 25 ohm r_{ON} and low leakage. The LM102 serves as a voltage buffer. This circuit can be adapted to a dual trace oscilloscope chopper. The DM7800 monolithic I.C. provides adequate switch drive controlled by DTL-TTL logic levels.



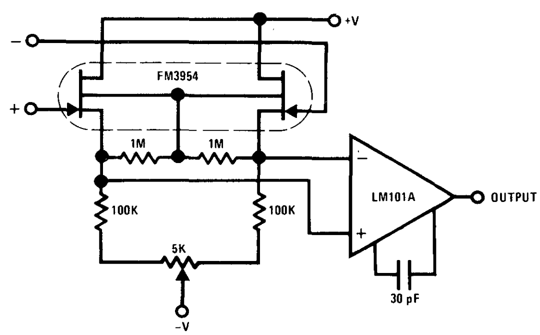
Low Distortion Oscillator

The 2N4416 JFET is capable of oscillating in a circuit where harmonic distortion is very low. The JFET local oscillator is excellent when a low harmonic content is required for a good mixer circuit.



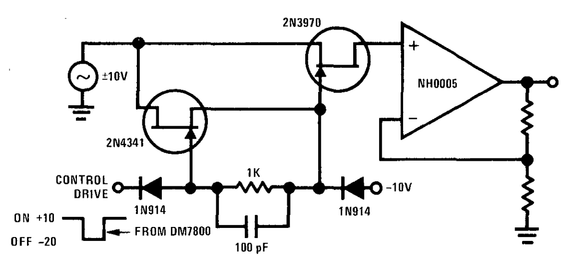
200 MHz Cascode Amplifier

This 200 MHz JFET cascode circuit features low crossmodulation, large-signal handling ability, no neutralization, and AGC controlled by biasing the upper cascode JFET. The only special requirement of this circuit is that I_{DSS} of the upper unit must be greater than that of the lower unit.



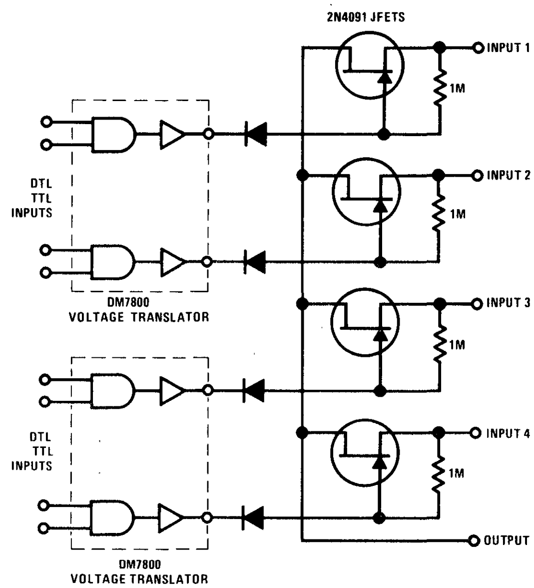
FET Op Amp

The FM3954 monolithic-dual provides an ideal low-offset, low-drift buffer function for the LM101A op amp. The excellent matching characteristics of the FM3954 track well over its bias current range thus improving common mode rejection.



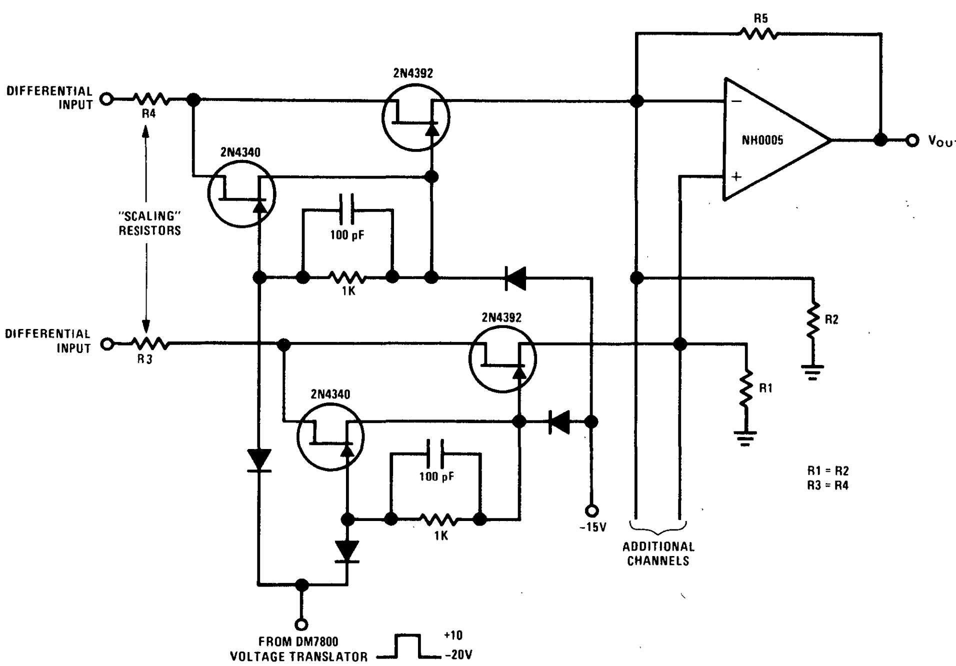
High Toggle Rate High Frequency Analog Switch

This commutator circuit provides low impedance gate drive to the 2N3970 analog switch for both on and off drive conditions. This circuit also approaches the ideal gate drive conditions for high frequency signal handling by providing a low ac impedance for off drive and high ac impedance for on drive to the 2N3970. The NH0005 op amp does the job of amplifying megahertz signals.



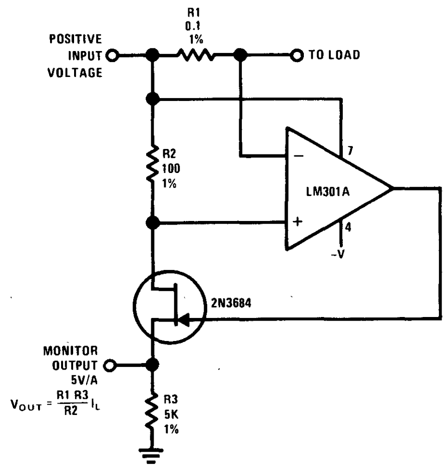
4-Channel Commutator

This 4-channel commutator uses the 2N4091 to achieve low channel ON resistance (<30Ω) and low OFF current leakage. The DM7800 voltage translator is a monolithic device which provides from +10V to −20V gate drive to the JFETs while at the same time providing DTL-TTL logic compatability.



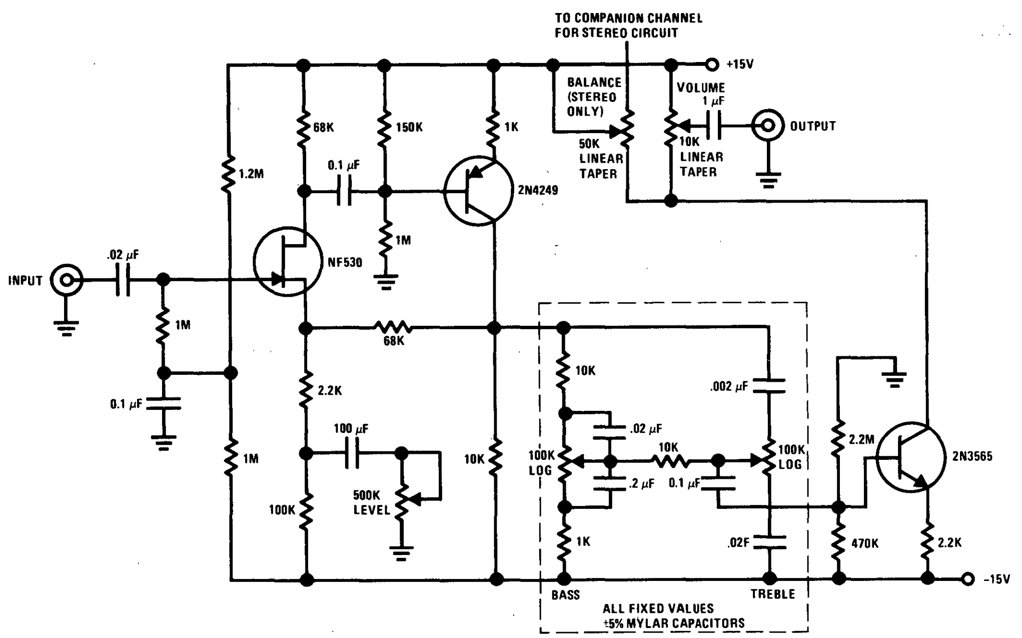
Wide Band Differential Multiplexer

This design allows high frequency signal handling and high toggle rates simultaneously. Toggle rates up to 1 MHz and MHz signals are possible with this circuit.



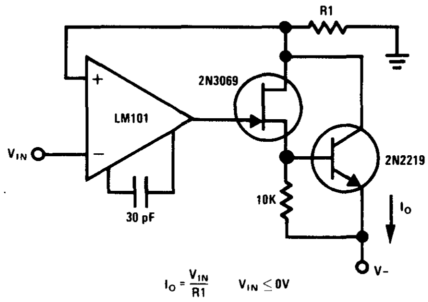
Current Monitor

R_1 senses current flow of a power supply. The JFET is used as a buffer because $I_D = I_S$, therefore the output monitor voltage accurately reflects the power supply current flow.



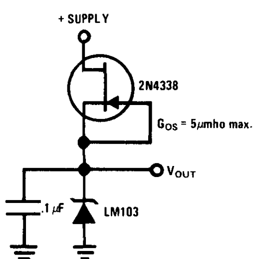
Low Cost High Level Preamp and Tone Control Circuit

This preamp and tone control uses the JFET to its best advantage; as a low noise high input impedance device. All device parameters are non-critical yet the circuit achieves harmonic distortion levels of less than .05% with a S/N ratio of over 85 dB. The tone controls allow 18 dB of cut and boost; the amplifier has a 1 volt output for 100 mV input at maximum level.



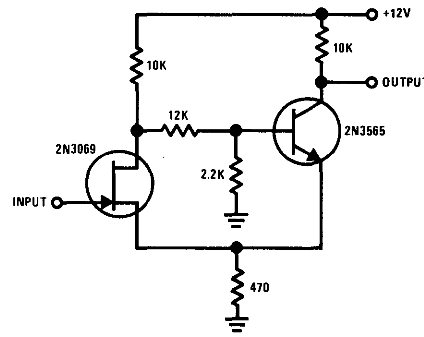
Precision Current Source

The 2N3069 JFET and 2N2219 bipolar serve as voltage isolation devices between the output and the current sensing resistor, R_1. The LM101 provides a large amount of loop gain to assure that the circuit acts as a current source. For small values of current, the 2N2219 and 10k resistor may be eliminated with the output appearing at the source of the 2N3069.



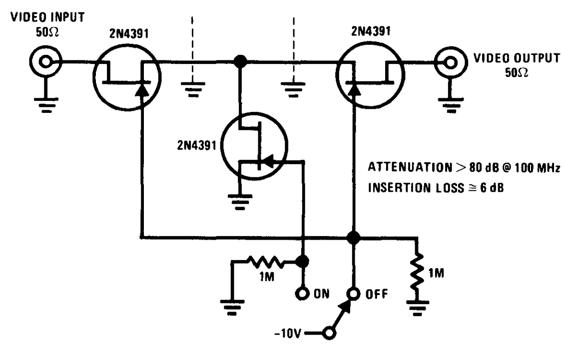
Low Power Regulator Reference

This simple reference circuit provides a stable voltage reference almost totally free of supply voltage hash. Typical power supply rejection exceeds 100 dB.



Schmitt Trigger

This Schmitt trigger circuit is "emitter coupled" and provides a simple comparator action. The 2N3069 JFET places very little loading on the measured input. The 2N3565 bipolar is a high h_{FE} transistor so the circuit has fast transition action and a distinct hysteresis loop.



High Frequency Switch

The 2N4391 provides a low on-resistance of 30 ohms and a high off-impedance (<.2 pF) when off. With proper layout and an "ideal" switch, the performance stated above can be readily achieved.

February 1970

ANALOG-SIGNAL COMMUTATION

INTRODUCTION

Telemetry and other data-acquisition systems have become very compact and efficient, particularly when built with integrated circuits. To keep in step, small, low-power commutators are needed to multiplex large numbers of analog signals. Metal-oxide-semiconductor field-effect transistors do the job well.

MOS IC's containing several MOSFET switching channels are presently available in production quantities and perform excellently as low-level analog commutators if the system designer understands their limitations and exploits their advantages. This report will describe the DC characteristics involved in switching analog signals when the signal input range varies between −10V and +10V.

MOSFET's size up very well against earlier switching devices when their overall characteristics are considered (see Table 1 and the discussion of competitive devices). In addition to being fabricated easily as multichannel IC's—in some cases, complete with switching-control circuitry on the chip—MOSFET's have several significant electrical advantages:

- Power dissipation is essentially zero in most applications. No DC power is consumed in the control gate, and practically no signal power is dissipated in the switch.
- Offset voltage is zero in a well-designed switch.
- Resistance is reasonably low when the channel is conducting.
- Resistance of an OFF channel is practically open-circuit (R_{OFF} is on the order of 10^{12} ohms and leakage currents are very small, about 100 pA).
- Analog signals are well isolated from the switch-control signals.

With all of these things in their favor, MOS analog-switching IC's will come into much wider use, especially in large, multichannel instrumentation and data-transmission systems.

	Mechanical Switch	Bipolar Transistor	Photocell	N Junction FET	P MOS FET
"On" Resistance	$10^{-2}\Omega$	10Ω	1 KΩ	30Ω	100Ω
"Off" Leakage	10 pA	100 pA	10 nA	100 pA	100 pA
Offset Voltage	0	10^{-2}V	0	0	0
Commutation Rate	1 KHz	100 KHz	100 Hz	10 MHz	50 MHz

Table 1

Comparison of Switches

MOS IC STRUCTURE

MOS IC's generally provide four or more channels in a monolithic chip, but two are enough to illustrate the basic construction that governs switch operation. The cutaway view of Figure 1 shows two complete MOSFET's, one of which may be on while the other is off. Figure 2 is the schematic.

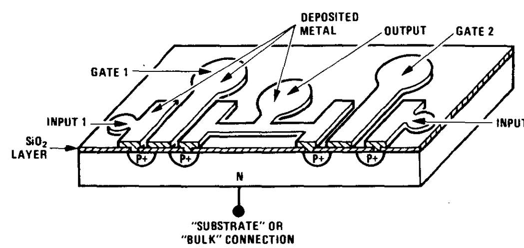


FIGURE 1. Cross-section of Two MOSFET's in an Integrated Circuit.

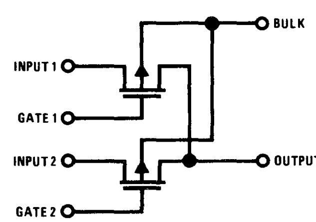
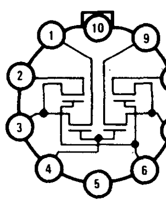


FIGURE 2. Schematic Diagram of Two-Channel Analog Switch.

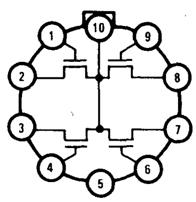
Both MOSFET's have a common substrate, the "bulk" consisting of lightly doped N type silicon. Thermally grown silicon oxide covers the entire chip surface, except where the oxide was etched away to allow ohmic connections of input and output electrodes to stripes diffused with P+ dopants. These stripes are the MOSFET drain and source regions. Each gate is defined by the gate electrode, which lies over a channel region and is isolated from it by the oxide (hence, MOSFET's are sometimes called insulated-gate FET's or IGFET's).

All electrodes are etched from a thin film of deposited aluminum. Each MOSFET has separate input and gate electrodes, but the output electrodes may be paired as shown, connected to a common output pin, or connected to separate output pins on the package. The same basic MOSFET structure can be used, whether the circuit is a differential switch, a multiplexer, or independent switches in a single package (see Figure 3).



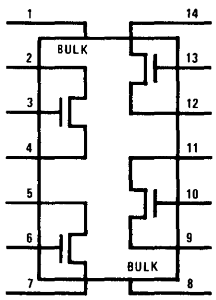
BULK

NOTE: Pin 5 connected to case and device bulk.
MM450, MM550



BULK

NOTE: Pin 5 connected to case and device bulk.
MM451, MM551



NOTE: Pins 1 and 8 connected to case and device bulk.
MM452, MM552

FIGURE 3. Connection Diagrams of Dual Differential Switch, Four-Channel Switch and Quad MOS Transistor.

MOSFET's are, for practical purposes, bilaterally symmetrical. The drain (or source) can be either the input or output. By strict definition, the drain is the electrode to which majority-carrier current flows. The majority carriers are "holes" in the channel of P-channel MOSFET's (N-channel MOSFET's are not commonly used in MOS IC's). In most analog switching applications, the signal contains AC components, so the direction of current flow frequently alternates.

SWITCHING AND ISOLATION

A P-channel MOSFET turns on when negative voltage is applied between gate and source. The gate is biased negative with respect to the bulk. Electrons accumulate on the gate, creating positive charges in the channel region. This inverts the electric charge thus creating an "enhanced" P type channel in the n-type semiconductor. When the gate is several volts more negative than threshold, a conducting channel is formed, allowing majority carrier current (holes) to flow freely between source and drain. The channel is said to be "enhanced," so these MOSFET's are called P-channel enhancement MOSFET's.

Operating voltages in a typical switching channel are illustrated in Figure 4. In most schematics, the bulk connection would not be shown.

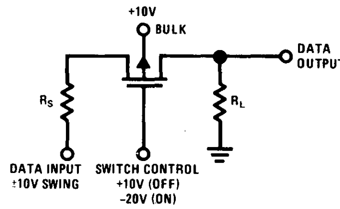


FIGURE 4. Biases on Single MOS Channel at Maximum Signal Range of ±10V.

The applied biases are those that would be used at an analog signal range of ±10V. At any signal range, the following guidelines apply:

1. Bulk bias V_{BB} must equal or be more positive than the most positive excursion of the analog signal. This bias must be maintained at all times, so is taken from a DC supply.
2. To turn the switch ON and make R_{ON} low, the voltage applied to the gate should be *at least* 5V more negative than the most negative excursion of the analog signal (10V is desirable). The actual gate voltage is V_{GG} and the gate bias is $-V_{GB}$.
3. To ensure that the switch turns OFF fully, V_{GG} should be as positive as V_{BB} making $V_{GB} = 0$.

The first rule must be followed to get good performance from the switch. With V_{BB} most positive, the p-n junctions are kept reverse-biased. When the channel is OFF, this condition isolates the drain from the source. When the switch is turned ON and the P-channel is enhanced, the drain-channel-source region is isolated by the p-n junction from the substrate because the substrate is "reverse biased" from all of these regions at all times.

The voltage across the switch, from drain to source, is caused by IR drop whether the switch is on or off. The MOS analog switch does not have any inherent offset voltage. To get $V_{out} = V_{in}$ in a MOSFET switch merely requires that load resistance R_L be much larger than the resistance in the conducting channel, R_{ON}. Since R_L is generally about 100 kilohms in most high-accuracy analog commutator applications, the requirement is easily met.

Figure 5 helps clarify rules (2) and (3). This curve shows how the gate-source threshold voltage changes with bulk-source bias voltage. Channel resistance is high and current flow at the output can only be a few microamperes. A forward bias higher than threshold is needed to enhance the channel. Making gate bias much more negative than V_{TH} at turn-ON does this. Then, at turn-OFF, the gate bias becomes more positive than V_{TH} when $V_{GG} = V_{BB}$. The channel must revert to N-type silicon thus preventing majority carrier current flow.

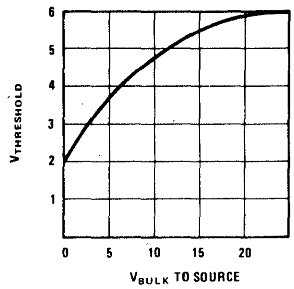
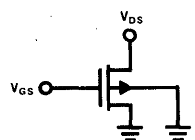
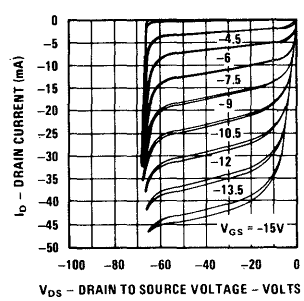


FIGURE 5. Variation in Switching-Threshold Voltage with Changes in Bulk-to-Source Bias Voltage.

The circuit designer must use biases that prevent the drain from having a positive potential when the switch is OFF. For example, V_{in} = +10V and V_{BB} = +9V should not be allowed. Operating with V_{DS} = +1V won't harm the MOSFET, but some of the signal will appear at the output. Effects of improper biasing can be seen in Figure 6. With the source and bulk grounded while V_{DS} varies, output currents at different gate biases are measured to produce the "drain family of curves." The normal family looks like Figure 6b (the drain

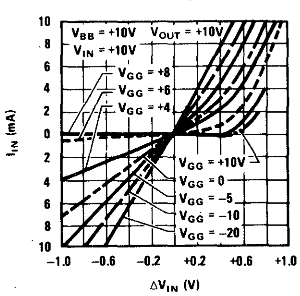


6a



6b

Dynamic R_{ON}



6c

FIGURE 6. Drain-Current Measuring Circuit, Normal Drain Family of Curves, and "Bipolar" Drain Family of Curves.

family of National Semiconductor's MM450/MM550 MOS switching IC's). The "bipolar" family in Figure 6c shows what happens when V_{DS} is allowed to go positive.

During small excursions of V_{DS}, the MOSFET acts as a voltage-variable resistor. But when V_{DS} rises to about +0.6V, there is an abrupt increase in drain current. At this point, the diode drop is exceeded and the drain-bulk junction becomes forward biased. Minority carriers are injected into the n-type channel region, causing grounded-base pnp bipolar transistor action (note in Figure 1 that a MOSFET resembles a lateral pnp transistor in the OFF condition). Output current will be α times the input current. In most MOS devices, the amplification factor will be 0.5 to 0.9.

It is absolutely mandatory that the $V_{DS} \geq +0.6V$ be avoided. Otherwise the effective R_{OFF} will be poor and the channel will seem to have abnormally high leakage current.

Only the upper right corner of the graph in Figure 6b, detailed in the third quadrant of Figure 6c, is useful in practical circuit designs. The useful characteristics are to the right of $-V_{DS}$ = –1 and above a load line at about I_D = 0.5 mA.

ON AND OFF RESISTANCE

Both R_{ON} and R_{OFF} normally vary with signal voltage and operating temperature. A positive signal voltage improves channel enhancement by making the gate more negative with respect to drain and source.

R_{ON} is minimum at the most positive signal level. It will increase slowly with temperature, since high temperatures reduce the mobility of majority carriers. Neverthless, R_{ON} will have little effect on signal quality if R_L is much larger. R_{ON} does vary nonlinearly, though, so we investigated its effect upon signal quality. Figure 7 proves that the effect

Total Harmonic Distortion vs V_{DS}

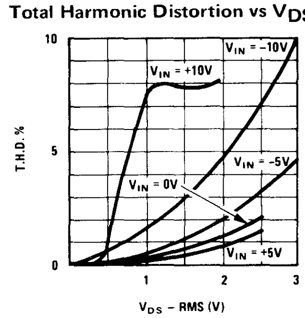


FIGURE 7. Small-Signal Harmonic Distortion (Measured with Only About 100 Ohms Load Resistance).

is negligible provided that the biasing rules are observed.

The curves of small-signal harmonic distortion in Figure 7 were measured with practically no load resistance. AC signals at various voltages were applied to the MOSFET input and the current flow was measured at the output with the help of a 100-ohm current-sensing resistor. Distortion levels less than 0.1% could not be measured with available instruments. The anomaly in the +10V curve is due to diode distortion of the type illustrated in Figure 6c. The input signal's AC plus DC components exceeded the bulk voltage, V_{BB} = +10V, by more than the +0.6V diode drop.

The harmonic distortion is amply low for practical applications. With a 1-kilohm load, the small-signal distortion typically would be less than 0.5%, with V_{in} = ±10V and V_{DS} almost ±1V. A load of 1 kilohm is unusually small. Small signal distortion would be almost unmeasurable with a 10-kilohm load. When signal accuracy must be very high, 100 kilohms are used by some designers.

Worst-case R_{ON} can be expected at a −10V input. Figure 8 gives the change in R_{ON} of the MM450/MM550 series devices when the analog input is at +10V, 0V and −10V. If lower impedance is essential, the gate can be biased more negative. For instance, at V_{BB} = +10V, V_{GG} can be made −25V or −30V instead of −20V, increasing $-V_{GB}$ to -35V or −40V. Don't go over the specificed maximum bias, which is usually −45V, because excessive bias could reduce the device operating life.

Conversely, all biases can be reduced if the signal voltage range is less than ±10V. The gate-drive circuit will not have to swing as far, the switch can be operated faster, and switching transients will be smaller. Or, the bulk bias can be reduced and the gate bias maintained at the previous ON level. This

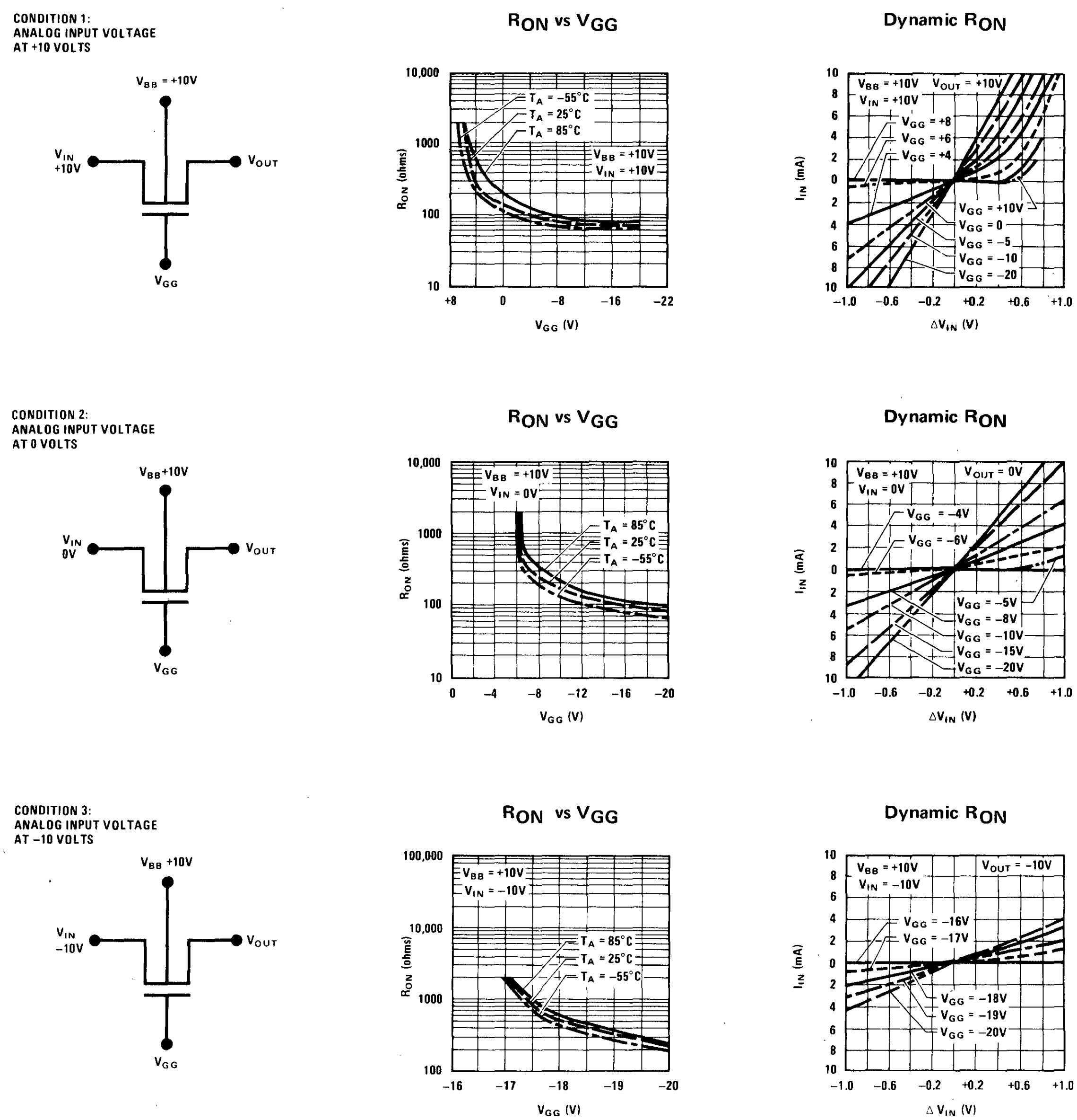


FIGURE 8. Typical R_{ON} Characteristics of MM450/MM550 MOS Devices at Most Positive, Zero and Most Negative Signal Voltages.

will give the effect shown in Figure 9—an improvement in channel enhancement and reductions in R_{ON} at the various signal levels.

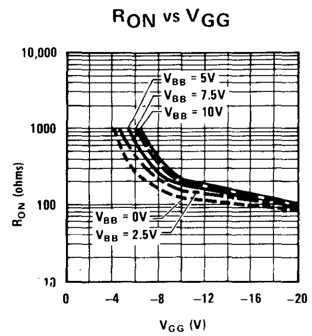


FIGURE 9. Bulk Bias Effect on R_{ON}.

When the gate is turned OFF, impedance between source and drain becomes very high ($R_{OFF} \approx 10^{12}$ ohms). A MOSFET's only significant DC conduction is leakage current. Total leakage in MM450/MM550 devices is typically less than 100 pA at 25°C. It rises more rapidly than R_{ON} with increasing temperature, approximately doubling with every 10°C rise in temperature. However, the MM450 devices are low-leakage types that are specified for use to 125°C. At the maximum temperature, leakage will usually be less than 100 nA. (At very high signal frequencies, another conduction mechanism may occur—analog signal feedthrough in the device capacitances, which can be prevented by making the gate-driver impedance low when the switch is OFF.)

The two significant forms of DC leakage are leakage from source and drain to bulk, and leakage through the channel from input to output. When all channels in the multiplexer are OFF, and the outputs of each MOSFET are connected to a common package pin, total leakage will be the sum of the bulk and channel leakages.

Worst-case leakage is measured with the circuit in Figure 10. The pin at which the leakage current is measured is biased to −25V and all other pins are grounded. This is equivalent to the bulk being biased at +10V, all gates at +10V, and all analog-signal inputs at +10V, with the output at −15V.

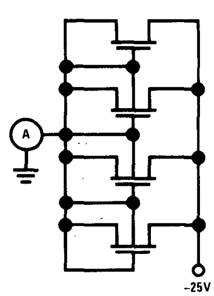


FIGURE 10. Worst-Case Leakage Test Circuit and Typical Worst-Case Total Leakage of MM451 at 25°C.

Channel leakage is measured with the test circuit in Figure 11a. At V_{in} = +10V, the leakage at the output is at its maximum positive value. As V_{in} goes more negative than +10V, channel leakage decreases, goes through zero, and becomes negative, as in Figure 11b.

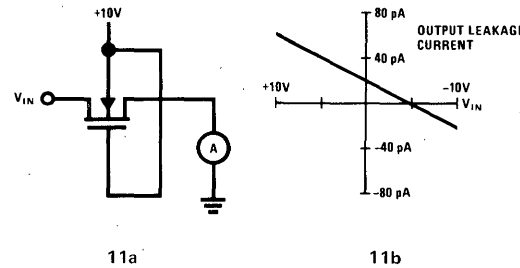


FIGURE 11. Channel-Leakage Test Circuit and Variation in Leakage with Signal Voltage.

The designer of switching systems that require very high R_{OFF} values under all signal conditions should anticipate the possibility of worst-case leakage. But average leakage will generally be considerably less than worst case. First, leakage currents in each switch are voltage-sensitive, and will be less than maximum at signal voltages less than +10V. Secondly, when the analog signals on some channels are positive and those on other channels are negative, the negative currents will subtract from the positive currents, further reducing the total leakage at the output. Also, when a switch is ON, it would not be contributing to the leakage. Assuming signal voltages vary randomly between +10 and −10V, total leakage will run about half that of worst case. Of course, leakage will be still less if the analog signal limits are less than ±10V.

CONCLUSION

Integrated MOSFET switching circuits make excellent low-level analog commutators. Power dissipation is essentially zero, capacitance is reasonably low (typically 8 pF at the analog input), the R_{OFF}/R_{ON} ratio is high, and the control signal is isolated from the input. MOS IC's with four or more switching channels are readily available in production quantities.

Conventional bipolar drive circuitry can control channel switching at rates in the megahertz range. Hybrid integrated circuits containing monolithic MOS multiplexers and bipolar drivers are being manufactured for medium-speed applications (NH0014 and NH0019). Level-changing circuits in these devices allow external TTL or DTL IC's to control the commutator at analog signal levels to ±10V. MOS commutator systems can be built with building-block circuits such as the MM454F in Figure 12. This monolithic IC can commutate at rates to 1 MHz, depending on the range of signal voltages. The control logic on the chip includes a clock-countdown chain that facilitates submultiplexing.

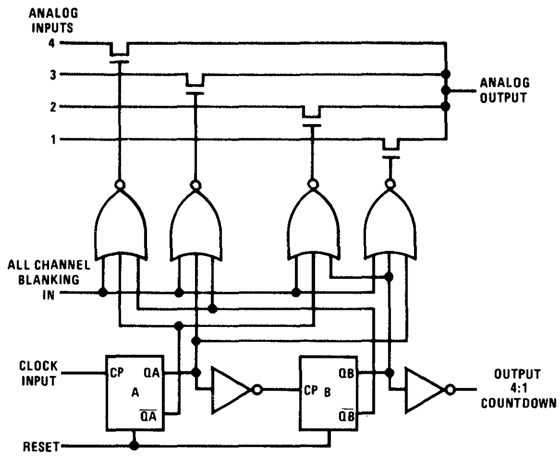


FIGURE 12. Logic Diagram of MM454F Four-Channel MOS Multiplexer. Switches and Control Circuitry Are Fabricated in the Same Monolithic Chip.

MOSFET switches are generally used to commutate low-frequency analog signals. Today, the preferred device for RF-signal multiplexing is the N-channel junction FET, which can handle signal frequencies in the VHF range. MOS IC's have operated successfully, however, in some RF application. The high-frequency capabilities of MOS IC's are being investigated by the author and will be the subject of a future report.

Although the most outstanding feature of MOSFET's is the ease with which they can be fabricated as multichannel monolithic IC's, their electrical characteristics compare quite favorably with those of other switching components. An "order of magnitude" comparison of MOSFET's and other devices that could be used for low-level analog switching is given by Table 1. Better characteristics might be obtained in each case, but these values are typical.

Each type of analog switch has advantages and limitations that must be considered for practical use. No switch is perfect. If a switch were perfect, it would have zero resistance when ON, infinite resistance when OFF, and be 100% efficient—that is, it would consume no power.

Electrically, the mechanical switch comes close to this ideal. It has the highest R_{OFF}/R_{ON} ratio and totally isolates the analog signal from the switching-control function. However, it has mechanical drawbacks that make it noisy and unsuitable for low-level commutation: contact bounce, contact pitting, susceptibility to vibration, and the necessity to move a physical mass to turn the switch on or off. It cannot commutate very fast and consumes more power than a solid-state switch, as a rule.

Bipolar transistors make excellent digital switches, the fastest ever developed, but they are usually a poor choice for multiplexing low-level analog signals. Their main disadvantages are an inherent offset voltage and the impossibility of isolating the switching control signal from the analog signal being switched. Furthermore, analog switching rates are slower than FET's. Their R_{on} is low, though—typically 10 ohms in analog switches (versus milliohms in power transistors). Bipolar transistors fare much better in high-level switching, where DC offset is not a problem.

Photocells make fairly good analog switches. Because light is used as the control signal, the control is completely isolated from the analog electrical signal. However, R_{ON} is high and the R_{OFF}/R_{ON} ratio is relatively poor. Even at moderate R_{OFF}/R_{ON} ratios, photocells cannot commutate much faster than 100 Hz. After exposure to intense light, a photocell made with a semiconductor such as cadmium sulfide or cadmium selenide exhibits a long turn-off decay time. Photocell turn-off time constants may stretch out for many seconds before R_{OFF} reaches an acceptable level. Faster switches can be made with combinations of electroluminescent diodes and phototransistors, but these devices are still very expensive.

Some N-channel junction FET's come close to being ideal switches. Offset voltage is zero, and the admittance-to-input capacitance ratio Y_{fs}/C_{iss} is the highest of any contemporary device. These two parameters govern commutation rate, which can be very high if the impedances of the signal source and the load are made very low. Theoretically, the high majority-carrier mobility in an N-channel J-FET enables it to operate at a frequency higher than any other type of FET. A good example is the 2N4391: R_{OFF}/R_{ON} is about 10^9, $R_{ds\ (on)}$ is a maximum of 30 ohms, and maximum leakage at 25°C is 100 pA. The one major disadvantage of N-channel J-FET's is that they are extremely difficult to make in the form of multichannel IC's. For high-frequency commutation, the P-channel type of J-FET is a poor choice because its majority carrier mobility is lower than N channel J-FET's.

March 1970

HOW TO BIAS THE MONOLITHIC JFET DUAL

The National Semiconductor monolithic JFET dual is a unique device. Its unusual intertwined geometry results in a very good matching characteristic and exceptional thermal tracking characteristic plus the fact that its drain currents may be biased over a broad range without seriously affecting matching and tracking. FM1100 through FM1111, FM1200 through FM1211, and FM3954 through FM3958 (similar to 2N3954 through 2N3958) are the device numbers for the monolithic JFET dual.

A typical National monolithic JFET dual's differential gate matching (ΔV_{GS}) is less than 10 mV and temperature drift is typically less than 10 μV/°C. What drain current you use for biasing is not critical, so you needn't even bother biasing the unit to its zero T.C. drain current, as far as ΔV_{GS} matching and tracking are concerned. $R_{DS(on)}$, Y_{fs}, and I_{DSS} track better than 1% over the full specified temperature range (−55°C to +125°C). The FM1100, FM1105, FM1200, and FM1205 are specified at 2 mV(max) ΔV_{GS} with a drift of 5 μV/°C(max). There are specs available which are less stringent than these, but many of the devices exceed this tough spec.

In order to obtain this performance advantage over separate matched JFET die, the two JFETs must be made such that there is one diffused "top" gate for each of the devices and a "bulk" gate which is common to both of the devices. (See Figure 1.) Normally, single triode JFETs have the diffused top gates internally connected to the bulk and this bulk is used as the gate connection. There are a few tetrode JFETs available with both the diffused gate and substrate gate brought out separately. The National monolithic JFET dual could be called a "siamese tetrode". This unique configuration presents several alternatives for proper biasing.

BIAS SCHEMES

If the bulk were ohmically connected to each gate, all gates would be common. The dual would turn into a differential switch, like the one in Figure 2,

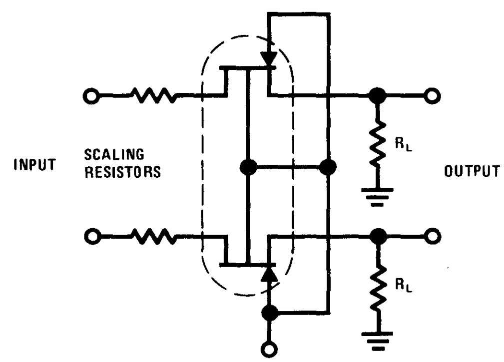


FIGURE 2. Dual Differential Analog Switch.

and would not be a true dual. This switch, incidentally, is an excellent application of the FM1100, FM1200, and FM3954 series. When the gates are tied externally, the near-perfect match of the JFETs assures precision in analog switching and multiplexing.

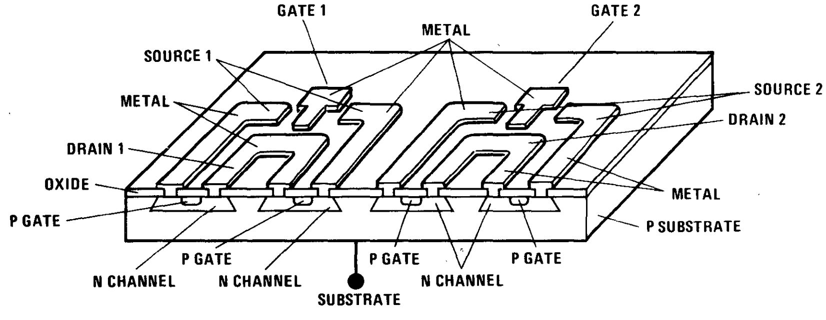


FIGURE 1. Simplified Section of Monolithic JFET Dual

AGC CONTROL

One of the most obvious uses of the bulk gate is AGC control because it is almost completely isolated from the signal path. The bulk bias voltage affects I_D, $V_{GS(off)}$, and Y_{fs}, but it does not significantly affect V_{GS} matching and tracking. The diffused gates (G_1 and G_2) could be called the differential mode gates and the bulk could be called a common mode gate.

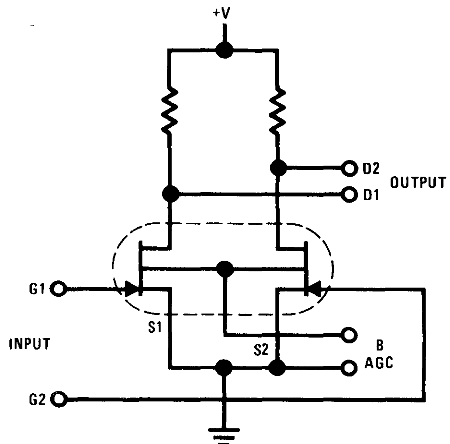


FIGURE 3. Automatic Gain Control.

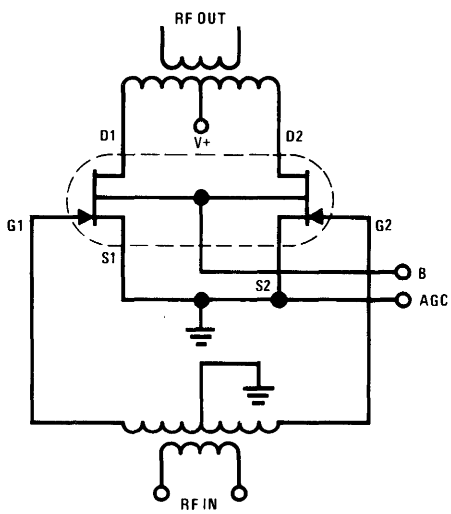


FIGURE 4. AGC Connections for Frequencies to 30 MHz.

OPERATIONAL AMPLIFIER BIASING

In operational amplifier applications which do not require any common mode rejection, biasing is fairly simple. The most straightforward biasing method is to simply ground the bulk as shown in Figure 5. Common mode rejection is very poor since the bulk gate is degenerative; it could become forward biased on positive common mode swings and cut off both channels on negative common mode swings.

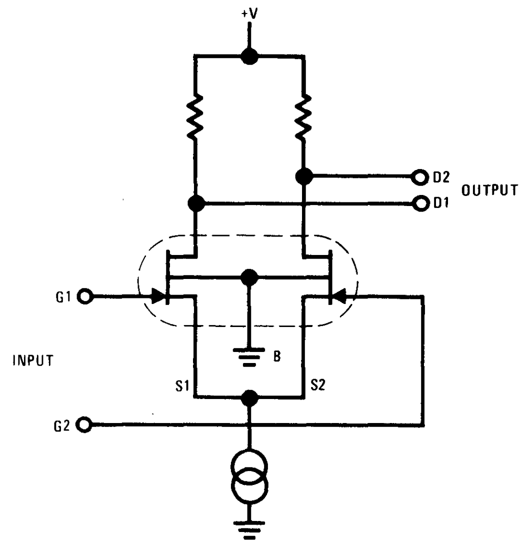


FIGURE 5. Substrate Bias, No Common-Mode Range.

For comparator applications, the bulk terminal may be connected to the comparison voltage along with gate 2. If the input varies over many volts (in excess of $V_{GS(off)}$), a 1M ohm resistor in series with gate 1 will prevent excessive gate current in the positive gate source forward bias situation or the negative gate-bulk reachthrough breakdown mode. Reachthrough breakdown will be covered later.

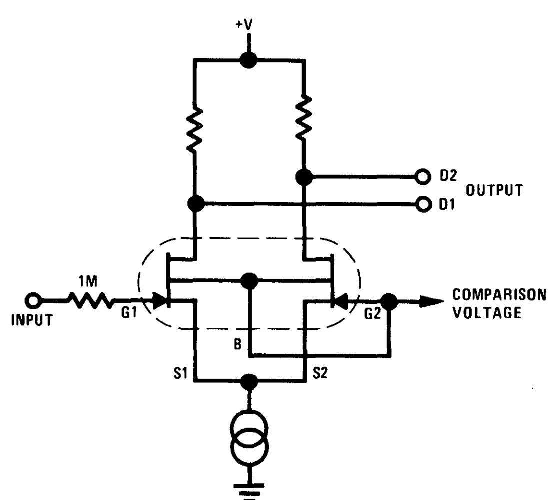


FIGURE 6. Biasing for Comparator Applications.

For special applications where very low leakage is desirable, drain-gate voltage should be kept as low as possible but in excess of pinchoff and drain current should be at 100 μA or less. Figure 7 uses the bulk to bias the monolithic JFET dual so that gate-source voltage is zero, thus eliminating that leakage component. The gates must be operated at or very close to ground potential; the LM101A is used for feedback biasing to force the source voltage to ground, using the bulk gate to control source voltage.

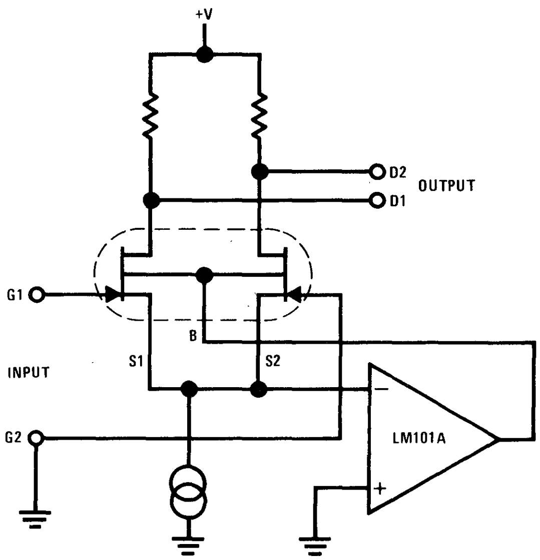


FIGURE 7. Low-Leakage Substrate Biasing Method.

BIASING OP AMPS FOR LARGE COMMON MODE RANGE

The simplest bias method to accommodate large common mode signals is shown in Figure 8, simply connect the bulk to the sources for the common source amplifier configuration.

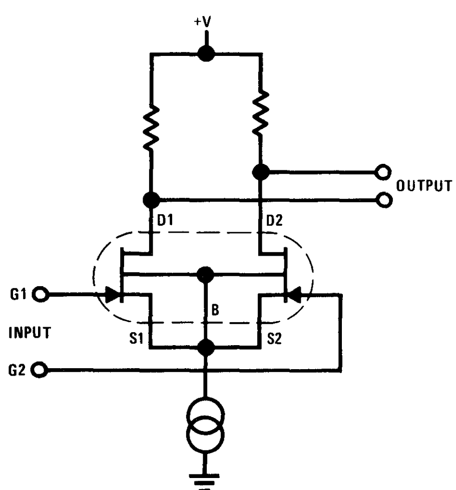


FIGURE 8. Large Common Mode Range Biasing, Common Source.

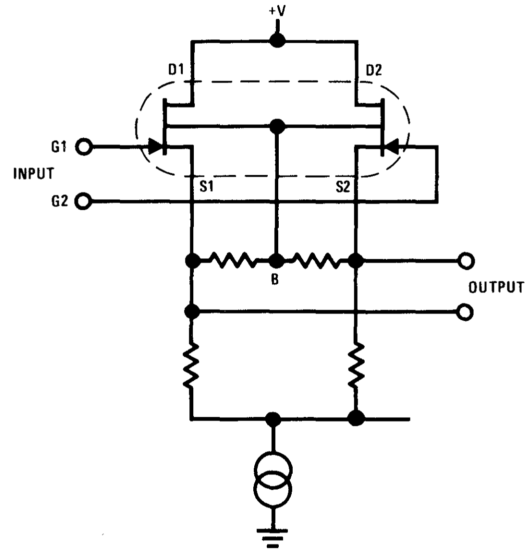


FIGURE 9. Large Common Mode Range Biasing, Common Drain.

If the common drain amplifier configuration is preferred, Figure 9 shows how to bias the bulk, just use a resistor from each of the sources, they should be the same value of course.

If large differential voltages are to be encountered (in excess of $V_{GS(off)}$) Figure 10 shows how to increase gate-bulk reachthrough voltage.

The circuit in Figure 10 has a static bias of zero volts from gate to bulk, regardless of drain current bias. The amplifiers in Figure 8 and 9 will have a finite static bias voltage from gate to bulk thus reducing the amount of input voltage required to cause reachthrough voltage from gate to bulk. Figure 10 shows optimum biasing for large differential signals. Reachthrough breakdown is only increased, not eliminated; the 10 MΩ bias resistors will prevent excessive gate to bulk current in the reachthrough breakdown mode.

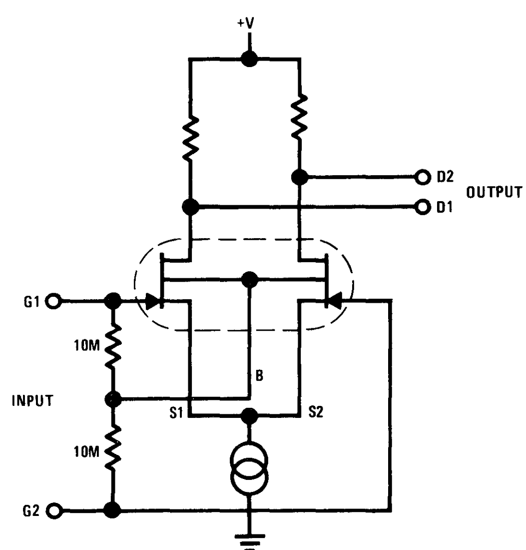


FIGURE 10. Best Biasing for Large Input Signals.

Additional series gate resistance must be used if gate source forward bias voltage is likely. These resistors will prevent excessive gate source forward current.

REACHTHROUGH VOLTAGE

Figure 11 is a simplified cross section of Figure 1. If $V_{bs} = 0$ and one of the gates is biased toward cutoff, channel current will decrease to the picoamp range. If the gate is driven past cutoff, the depletion region will reach the bulk and "reachthrough" voltage from gate to bulk will be encountered. Figure 12 shows reachthrough is greater than $V_{GS(off)}$ and varies from one unit to another just as $V_{GS(off)}$ does. Electrically, reachthrough breakdown is similar to a zener diode breakdown, i.e., the gate impedance will rapidly change from a very high to a very low value. As long as the current is 0.1 mA or less, the device will not be damaged.

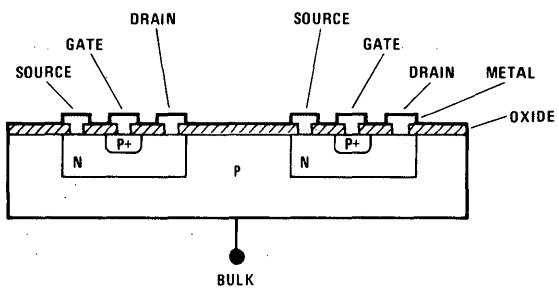
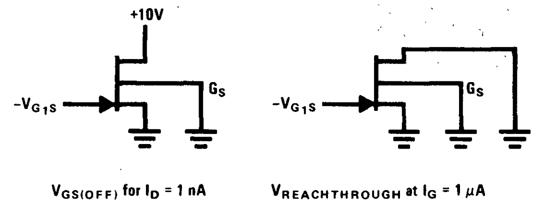


FIGURE 11. Simplified Cross Section of Monolithic JFET Dual.



GATE 1 $V_{REACHTHROUGH} \cong |V_{G_1S(OFF)}| + V_{G_SS(FORWARD)}$

$V_{G_SS(FORWARD)} \cong 0.6V$

FIGURE 12. Reachthrough in One Half of Dual JFET.

The circuit designer must also bear in mind reachthrough voltage when using large signal AC voltages. If instantaneous voltages from gate to bulk are too great, reachthrough breakdown will occur.

CONCLUSION

National Semiconductor's monolithic JFET duals (FM1100 series, FM1200 series, and FM3954 series) can be used in a wide variety of applications. The bulk gate can be put to advantageous use for reducing input gate leakage, AGC operation, RF balanced mixer applications, or even differential analog switch usage. All in all, the seven terminal monolithic JFET dual is more flexible, useful, and economical than a six terminal two chip dual. The monolithic dual now allows performance levels which were heretofore impossible to achieve.

May 1970

APPLICATIONS OF MOS ANALOG SWITCHES

ABSTRACT

This discussion begins with some basic commutation circuits, then describes some uses in linear amplifier applications such as reset functions and chopper applications. The use of MOS switches as a suppressed carrier double-sideband modulator and a double-sideband demodulator is then covered; followed by a circuit proposal for a phase-locked loop AM-FM detector without tuned circuits.

THE MOS DIFFERENTIAL SWITCH—DC TO RF

The dual differential switch is a particular switch connection scheme which at first glance prompts one to say—so what? It is, however, one of those simple circuit configurations which can find a wide variety of uses in electronic circuits. The dual differential switch could also be called a DPDT switch or two SPDT switches—depending on how they are toggled.

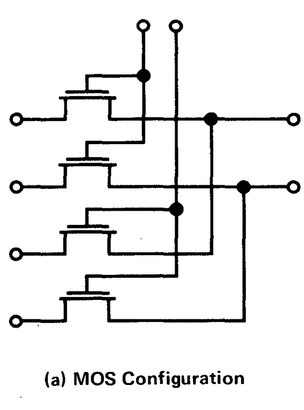
MOS switches have some unique features which make them very useful for data switching[1,2,3]: no offset voltage, high R_{OFF}/R_{ON} ratios, low leakage, fast operation, and matched "on" resistance. Within definite bounds, MOS switches exhibit good isolation between the switching drive and signal path.

MOS switches do have somewhat unique driving requirements. In order to solve this problem, National manufactures a hybrid integrated circuit which provides DTL-TTL drive compatibility with the dual differential switch. These devices use the DM7801 chip with an MM450 chip for the NH0014 and the DM7800 chip with an MM450 chip for the NH0019. The NH0014 is basically a DPDT switch while the NH0019 is two SPDT switches in the same package. Each connection has its particular advantages and disadvantages.

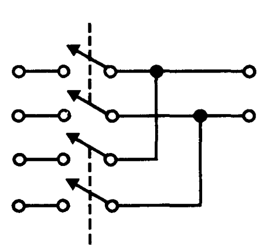
COMMUTATION CIRCUITS

The NH0014 may be used as a two channel commutator only, because two of its four channels are always on. The NH0019 may be used for systems with any number of channels since it can shut all channels off on command.

Figure 3 shows a six channel commutator which may be easily expanded. Data sampling may be done on any format which the user chooses. Sampling format is easily controlled by DTL or TTL logic design independent of the NH0019. Since each buffer-driver of the NH0019 has a dual input gate, all channel blanking is readily achieved. If desired, the format shown in Figure 3 may be



(a) MOS Configuration

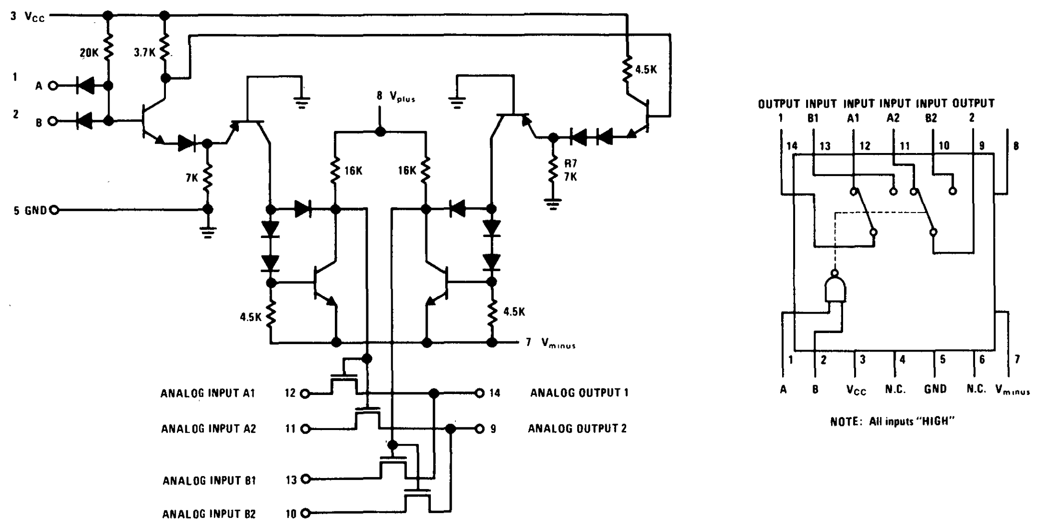


(b) Schematic Configuration

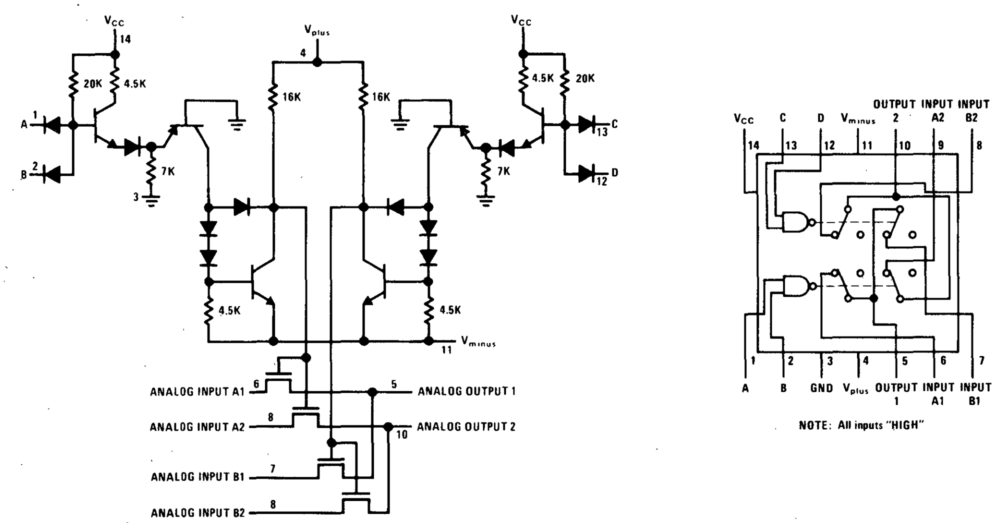
FIGURE 1. MM450/MM550 MOS Dual Differential Switch

modified so as to use the NH0019 logic inputs as binary gates which can reduce the command logic complexity if the blanking function is not required.

Since the multiplexed information is in differential form, common mode noise is greatly reduced. Also, the MOS gate drive spiking is drastically reduced because of the differential channel configuration. Demultiplexing may be accomplished by using a circuit identical to the multiplexer because the MOS device is a true bilateral switch. In hard-wired systems where the multiplex "outputs" are electrically connected as in Figure 4, the signal may be transmitted in either direction. For non-hardwired systems, the modulation-demodulation sequence is still bilateral, but provisions must be made for transmit/receive function control.



(a) NH0014



(b) NH0019

FIGURE 2. NH0014 and NH0019 DTL-TTL Compatible MOS Analog Switches

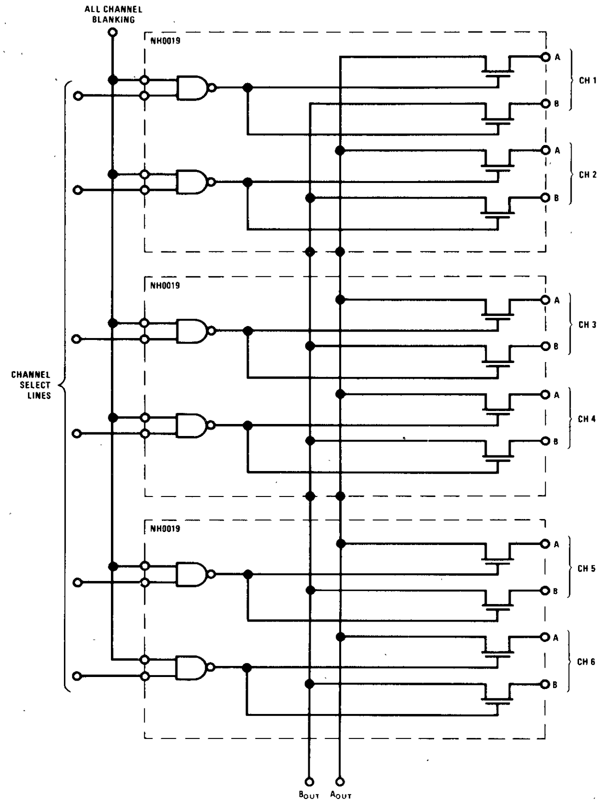


FIGURE 3. Differential Signal Commutator—NH0019

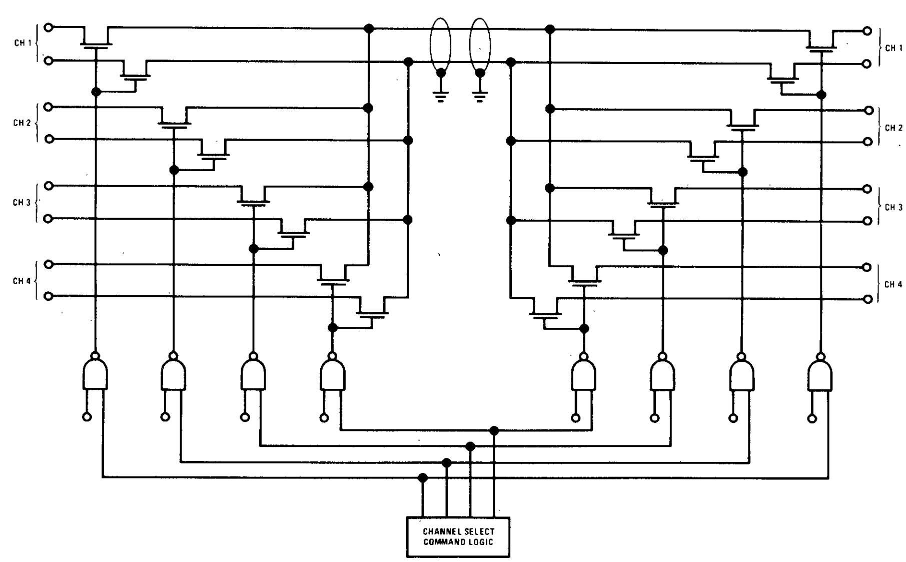


FIGURE 4. Commutation-Modulation and Demodulation

USAGE IN LINEAR AMPLIFIER CIRCUITS

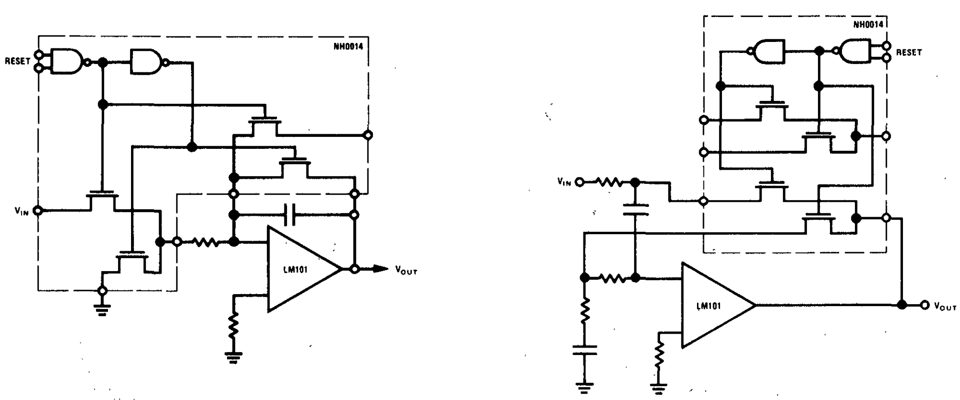
The NH0014 and NH0019 devices are useful for switching functions in linear circuit applications because of high off/on resistance ratio and ease of switching control using logic elements. Sample and hold circuits, integrator reset switching, and reset stabilized amplifiers are a few examples (Figure 5). More detailed information on this type of circuitry is available in National Semiconductor applications notes AN-4, AN-5, AN-20, and AN-29[4-7]

An obvious use of the NH0014 and NH0019 are in chopper stabilized amplifiers (Figure 6). One of the better forms of chopper stabilized amplifiers is the series shunt chopper with sample and hold type of output. The NH0014 does a good job at this because it contains the complete set of switches plus proper drive for the switches. The NH0014 can greatly reduce component count for chopper stabilized amplifiers.

DOUBLE SIDEBAND MODULATOR

The NH0019 can be used as a double sideband modulator. In modulator applications, the NH0019 functions as a DPDT switch which alternately reverses the polarity of the modulating signal at the chopper frequency. MOS switches work quite well at this application because of zero offset voltage and large signal handling ability.

In order to build a double sideband balanced modulator[8,9], one of the two modulating inputs must be applied as a balanced input. For the circuit shown in Figure 7, an LM102 and LM107 were used for an audio phase splitter.



(a) Integrator

(b) Reset Stabilized Amplifier

FIGURE 5. Switching Applications With Linear Circuits

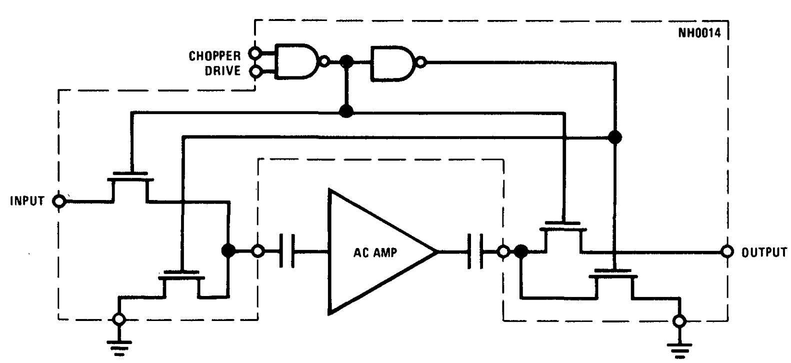


FIGURE 6. Series-Shunt Chopper Stabilized Amplifier

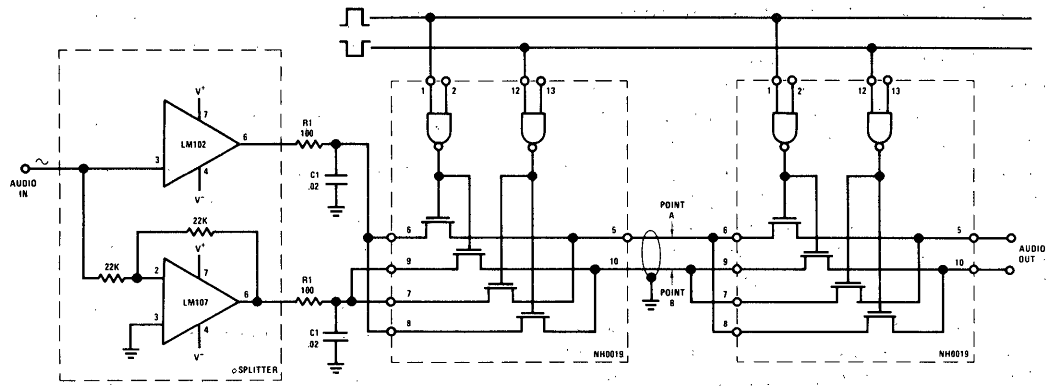


FIGURE 7. Double Sideband Modulator-Demodulator

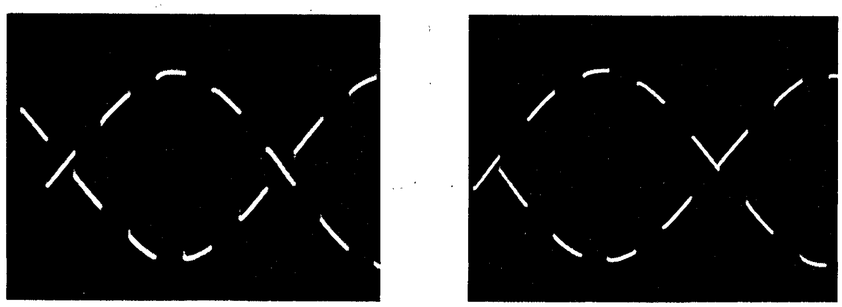
Both point A and point B in Figure 7 are DSB modulated outputs; so, technically, you could get by with only one. The waveform at point A is illustrated in Figure 8a for a carrier frequency of 100 kHz and an audio frequency of 12.5 kHz. Point B is equal and out of phase.

One type of spurious response encountered with MOS switching devices is output spikes caused by a charge being dumped into the channel by the gate drive through gate-channel capacitance. By adding C1, part of the charge can be absorbed, the switching transients are an "in phase" or "common mode" error.

To better illustrate the improvement by using a balanced output, the audio signal was reduced to zero volts and the points A, B, and A-B were measured as shown in Figure 9. The improvement operating in the differential mode is obvious.

The circuit drive requirements for Figure 7 may be simplified by using the NH0014 since it provides an inverting function internally. Only one phase of toggle drive to the NH0014 is required.

Horiz. 10 ns/cm
Vert. 1V/cm



(a) V_a (b) V_a-V_b

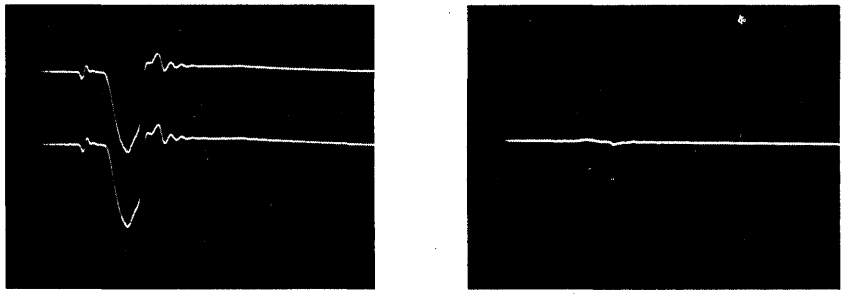
FIGURE 8. Double Sideband Signal

thus reducing the voltage amplitude of the spikes. The R1C1 combination has its 3 dB point at about 80 kc, so output from the phase splitter was not attenuated in the audio range.

The astute observer will notice switching transients on the waveform in Figure 8a. By taking the output in differential form at points A and B, these transients are greatly reduced because the desired signals are equal but of opposite polarity, while

The modulation will be distorted more due to the phase lag created by the internal inverter of the NH0014. Figure 10a shows the switching performance of the NH0019 while Figure 10b shows the switching performance of the NH0014. In applications which do not require high carrier frequencies, the NH0014 is adequate, but for carrier frequencies above 100 kHz, the NH0019 provides improved performance because of its symmetrical switching behavior.

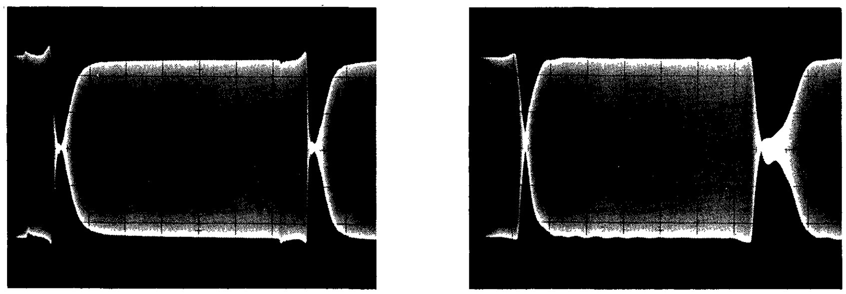
Horiz. 50 ns/cm
Vert. 0.1V/cm



(a) Upper Trace - V_a
Lower Trace - V_b

(b) V_a-V_b

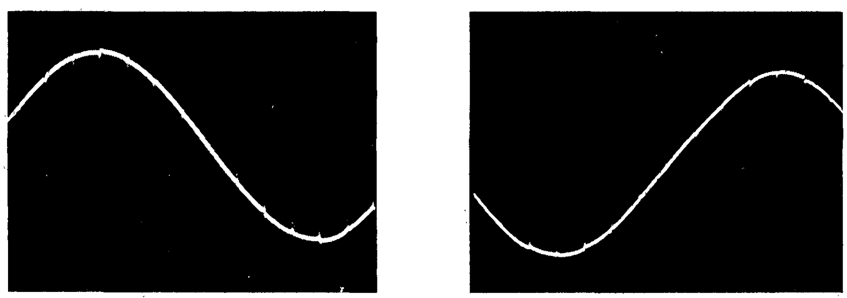
FIGURE 9. MOS Switching Transients



(a) NH0019 50 ns/cm

(b) NH0014 50 ns/cm

FIGURE 10. Channel Switching—NH0019 vs NH0014



(a) Single Ended Output

(b) Differential Output

FIGURE 11. Demodulator Recovered Output

DOUBLE SIDEBAND DEMODULATOR

The major requirement of double sideband signal demodulation is proper carrier reinsertion. For maximum output, the carrier must be reinserted exactly in phase or exactly 180° out of phase with respect to the signal. Any departure from this optimum phase relationship will reduce the recovered signal amplitude. By applying the double sideband signal to a second NH0019, as shown in Figure 7, the original modulating waveform may be recovered, along with some switching transients (Figure 11).

These switching transients may be filtered out quite easily. It is, however, instructive to compare the recovered audio signal with the original. The modulating signal had less than 0.1% distortion at 1 kHz. Figure 12 shows the distortion of the recovered signal vs. signal amplitude.

Carrier frequency was 100 Hz for the upper curve and 10 kHz for the lower. These curves indicate that most of the distortion is due to switching transients, especially at low modulation levels. Output filtering will significantly reduce the recovered signal distortion.

Figure 13 emphasizes the affect that switching transients have on harmonic distortion. At carrier frequencies below 10 kHz, the RMS value of the transients is reduced to a point where distortion of the MOS switches themselves can be seen.

The NH0014 and NH0019 data sheet suggests a V plus supply value of 10 volts and a V minus supply value of −20 volts. However, switching transients may be reduced by using different power supply voltages. Figure 14 and Figure 15 show what happens to harmonic distortion caused by spiking versus power supply level. Figure 14 is plotted for V minus with V plus at 10 volts. Figure 15 shows what happens as V plus is varied. All of the previous data was taken at V plus at 14 volts and V minus at −12 volts.

AM-FM DEMODULATOR

Although an AM-FM demodulator was not physically constructed, the previously discussed "double sideband demodulator" performance implies that a very interesting phase detector can be built. The interesting features of this type of a detector are large dynamic range, recovery of both in-phase (amplitude modulated) and quadrature-phase (frequency modulated) signals plus the feasibility of not using any inductors for tuning.

Figure 16 shows the proposed circuit block diagram which uses a phase-locked loop for phase reference signal. The voltage controlled oscillator (VCO) is operated at 4 f_o. Flip Flop #1 provides a two phase output which is fed into FF #2 and FF #3. The outputs of FF #2 and FF #3 are exactly 90° out of phase regardless of the frequency of the VCO. This kind of performance is awfully hard to achieve using tuned circuits. For a 455 kHz detector, the VCO would operate at 1820 kHz. TTL flip flops will operate quite nicely at that frequency and should hold phase shift errors to practically zero. The LM107 provides DC gain to close the phase-locked loop, it forces the VCO to a frequency and phase angle which causes the "FM out" port to zero volts DC; this port is then operating exactly in quadrature with the applied signal. This part of the detector is then insensitive to amplitude modulation and sensitive to frequency modulation. Since the AM detector portion is operating exactly 90° out of phase with the FM portion, its output is insensitive to FM and sensitive to AM.

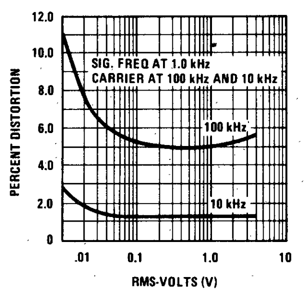


FIGURE 12. Recovered Signal Harmonic Distortion vs Audio Modulation Level

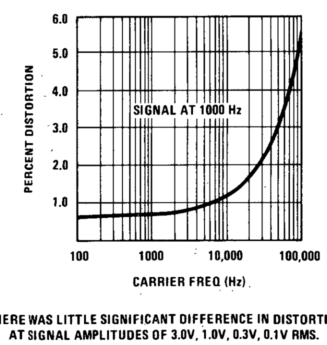


FIGURE 13. Recovered Signal Harmonic Distortion vs Carrier Frequency

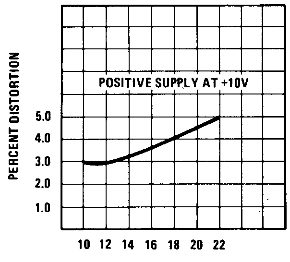


FIGURE 14. Harmonic Distortion vs Negative Power Supply Voltage

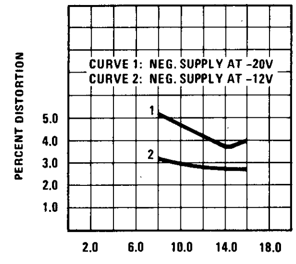


FIGURE 15. Harmonic Distortion vs Positive Supply Voltage

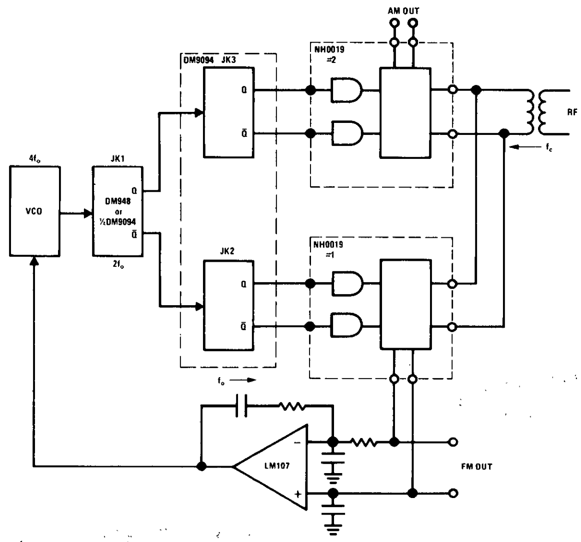


FIGURE 16. AM-FM Demodulator

CONCLUSION

The most obvious use of the NH0014 and NH0019 is in commutator applications, and it indeed is a very useful device for that purpose. The use of these switches in linear circuit applications is also very attractive because of DTL-TTL control compatibility. There are many more uses of these switches possible than the few examples described here.

The unusual application of these devices as suppressed carrier double-sideband modulators and demodulators suggests applications in servo systems and even communications systems due to their high speed operation. The final circuit suggestion, a phase-locked loop AM-FM demodulator without tuned circuits should be very useful in communications systems. The NH0019 will operate quite well at an IF frequency of 455 kHz or less.

These basic capabilities of the MOS dual differential switch should encourage much greater usage of this type of device in new product designs.

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October 1970

PRECISION IC COMPARATOR RUNS FROM 5V LOGIC SUPPLY

INTRODUCTION

In digital systems, it is sometimes necessary to convert low level analog signals into digital information. An example of this might be a detector for the illumination level of a photodiode. Another would be a zero crossing detector for a magnetic transducer such as a magnetometer or a shaft-position pickoff. These transducers have low-level outputs, with currents in the low microamperes or voltages in the low millivolts. Therefore, low level circuitry is required to condition these signals before they can drive logic circuits.

A voltage comparator can perform many of these precision functions. A comparator is essentially a high-gain op amp designed for open loop operation. The function of a comparator is to produce a logic "one" on the output with a positive signal between its two inputs or a logic "zero" with a negative signal between the inputs. Threshold detection is accomplished by putting a reference voltage on one input and the signal on the other. Clearly, an op amp can be used as a comparator, except that its response time is in the tens of microseconds which is often too slow for many applications.

A unique comparator design will be described here along with some of its applications in digital systems. Unlike older IC comparators or op amps, it will operate from the same 5V supply as DTL or TTL logic circuits. It will also operate with the single negative supply used with MOS logic. Hence, low level functions can be performed without the extra supply voltages previously required.

The versatility of the comparator along with the minimal circuit loading and considerable precision recommend it for many uses, in digital systems, other than the detection of low level signals. It can be used as an oscillator or multivibrator, in digital interface circuitry and even for low voltage analog circuitry. Some of these applications will also be discussed.

CIRCUIT DESCRIPTION

In order to understand how to use this comparator, it is necessary to look briefly at the circuit configuration. Figure 1 shows a simplified schematic of the device. PNP transistors buffer the

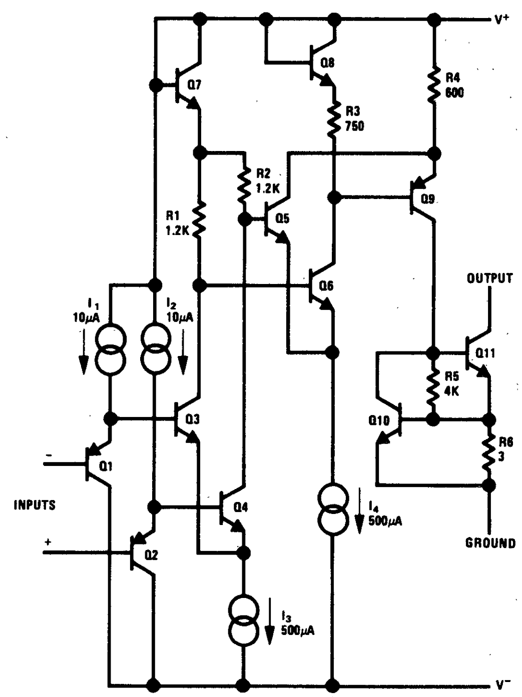

FIGURE 1. Simplified Schematic of the Comparator

differential input stage to get low input currents without sacrificing speed. The PNP's drive a standard NPN differential stage, Q_3 and Q_4. The output of this stage is further amplified by the Q_5–Q_6 pair. This feeds Q_9 which provides additional gain and drives the output stage. Current sources are used to determine the bias currents, so that performance is not greatly affected by supply voltages.

The output transistor is Q_{11}, and it is protected by Q_{10} and R_6 which limit the peak output current. The output lead, since it is not connected to any other point in the circuit, can either be returned to the positive supply through a pull-up resistor or switch loads that are connected to a voltage higher than the positive supply voltage. The circuit will operate from a single supply if the negative supply lead is connected to ground. However, if a negative supply is available, it can be used to increase the input common mode range.

Table 1 summarizes the performance of the comparator when operating from a 5V supply. The circuit will work with supply voltages up to ±15V

Table 1. Important Electrical Characteristics of the LM111 Comparator when Operating from Single, 5V Supply (T_A = 25°C).

Parameter	Limits			Units
	Min	Typ	Max	
Input Offset Voltage		0.7	3	mV
Input Offset Current		4	10	nA
Input Bias Current		60	100	nA
Voltage Gain		100		V/mV
Response Time		200		ns
Common Mode Range	0.3		3.8	V
Output Voltage Swing			50	V
Output Current			50	mA
Fan Out (DTL/TTL)	8			
Supply Current		3	5	mA

with a corresponding increase in the input voltage range. Other characteristics are essentially unchanged at the higher voltages.

LOW LEVEL APPLICATIONS

A circuit that will detect zero crossing in the output of a magnetic transducer within a fraction of a millivolt is shown in Figure 2. The magnetic

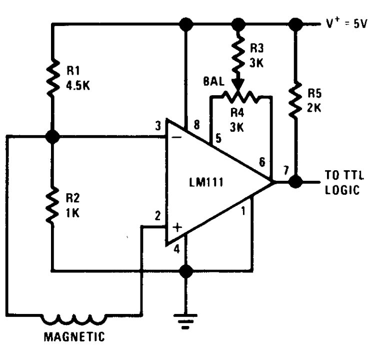

FIGURE 2. Zero Crossing Detector for Magnetic Transducer

pickup is connected between the two inputs of the comparator. The resistive divider, R_1 and R_2, biases the inputs 0.5V above ground, within the common mode range of the IC. The output will directly drive DTL or TTL. The exact value of the pull up resistor, R_5, is determined by the speed required from the circuit since it must drive any capacitive loading for positive-going output signals. An optional offset-balancing circuit using R_3 and R_4 is included in the schematic.

Figure 3 shows a connection for operating with MOS logic. This is a level detector for a photodiode that operates off a −10V supply. The output changes state when the diode current reaches 1 μA. Even at this low current, the error contributed by the comparator is less than 1%.

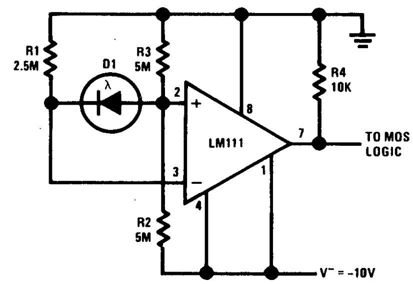

FIGURE 3. Level Detector for Photodiode

Higher threshold currents can be obtained by reducing R_1, R_2 and R_3 proportionally. At the switching point, the voltage across the photodiode is nearly zero, so its leakage current does not cause an error. The output switches between ground and −10V, driving the data inputs of MOS logic directly.

The circuit in Figure 3 can, of course, be adapted to work with a 5V supply. At any rate, the accuracy of the circuit will depend on the supply-voltage regulation, since the reference is derived from the supply. Figure 4 shows a method

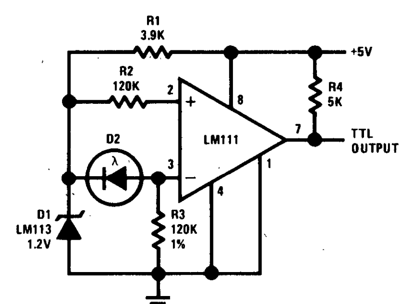

FIGURE 4. Precision Level Detector for Photodiode

of making performance independent of supply voltage. D_1 is a temperature-compensated reference diode with a 1.23V breakdown voltage. It acts as a shunt regulator and delivers a stable voltage to the comparator. When the diode current is large enough (about 10 μA) to make the voltage drop across R_3 equal to the breakdown voltage of D_1, the output will change state. R_2 has been added to make the threshold error proportional to the offset current of the comparator, rather than the bias current. It can be eliminated if the bias current error is not considered significant.

A zero crossing detector that drives the data input of MOS logic is shown in Figure 5. Here, both a

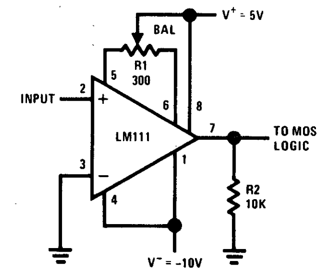

FIGURE 5. Zero Crossing Detector Driving MOS Logic

positive supply and the −10V supply for MOS circuits are used. Both supplies are required for the circuit to work with zero common-mode voltage. An alternate balancing scheme is also shown in the schematic. It differs from the circuit in Figure 2 in that it raises the input-stage current by a factor of three. This increases the rate at which the input voltage follows rapidly-changing signals from 7V/µs to 18V/µs. This increased common-mode slew can be obtained without the balancing potentiometer by shorting both balance terminals to the positive-supply terminal. Increased input bias current is the price that must be paid for the faster operation.

DIGITAL INTERFACE CIRCUITS

Figure 6 shows an interface between high-level logic and DTL or TTL. The input signal, with 0V and 30V logic states is attenuated to 0V and 5V by R_1 and R_2. R_3 and R_4 set up a 2.5V threshold

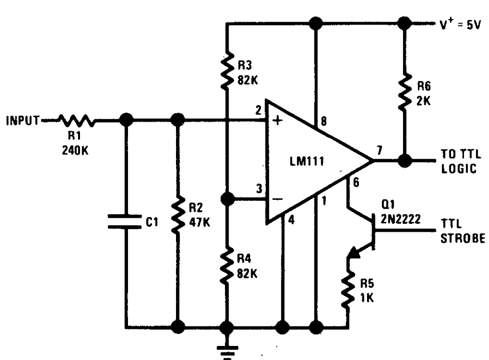

FIGURE 6. Circuit for Transmitting Data Between High-Level Logic and TTL

level for the comparator so that it switches when the input goes through 15V. The response time of the circuit can be controlled with C_1, if desired, to make it insensitive to fast noise spikes. Because of the low error currents of the LM111, it is possible to get input impedances even higher than the 300 kΩ obtained with the indicated resistor values.

The comparator can be strobed, as shown in Figure 6, by the addition of Q_1 and R_5. With a logic one on the base of Q_1, approximately 2.5 mA is drawn out of the strobe terminal of the LM111, making the output high independent of the input signal.

Sometimes it is necessary to transmit data between digital equipments, yet maintain a high degree of electrical isolation. Normally, this is done with a transformer. However, transformers have problems with low-duty-cycle pulses since they do not preserve the dc level.

The circuit in Figure 7 is a more satisfactory method of obtaining isolation. At the transmitting

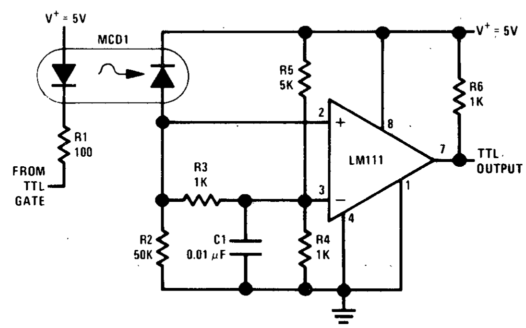

FIGURE 7. Data Transmission System with Near-Infinite Ground Isolation

end, a TTL gate drives a gallium-arsenide light-emitting diode. The light output is optically coupled to a silicon photodiode, and the comparator detects the photodiode output. The optical coupling makes possible electrical isolation in the thousands of megohms at potentials in the thousands of volts.

The maximum data rate of this circuit is 1 MHz. At lower rates (~200 kHz) R_3 and C_1 can be eliminated.

MULTIVIBRATORS AND OSCILLATORS

The free-running multivibrator in Figure 8 is another example of the versatility of the comparator. The inputs are biased within the common mode range by R_1 and R_2. DC stability, which insures starting, is provided by negative feedback through R_3. The negative feedback is reduced at high frequencies by C_1. At some frequency, the positive feedback through R_4 will be greater than the negative feedback; and the circuit will oscillate. For the component values shown, the circuit delivers a 100 kHz square wave output. The frequency can be changed by varying C_1 or by adjusting R_1 through R_4, while keeping their ratios constant.

Because of the low input current of the comparator, large circuit impedances can be used. Therefore, low frequencies can be obtained with relatively-small capacitor values: it is no problem to get down to 1 Hz using a 1 μF capacitor. The speed of the comparator also permits operation at frequencies above 100 kHz.

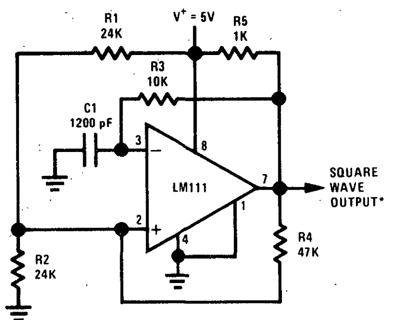

FIGURE 8. Free-Running Multivibrator

The frequency of oscillation depends almost entirely on the resistance and capacitor values because of the precision of the comparator. Further, the frequency changes by only 1% for a 10% change in supply voltage. Waveform symmetry is also good, but the symmetry can be varied by changing the ratio of R_1 to R_2.

A crystal-controlled oscillator that can be used to generate the clock in slower digital systems is shown in Figure 9. It is similar to the free running multivibrator, except that the positive feedback is obtained through a quartz crystal. The circuit oscillates when transmission through the crystal is at a maximum, so the crystal operates in its shunt-resonant mode. The high input impedance of the comparator and the isolating capacitor, C_2,

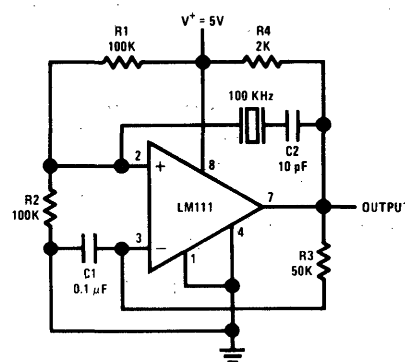

FIGURE 9. Crystal-Controlled Oscillator

minimize loading of the crystal and contribute to frequency stability. As shown, the oscillator delivers a 100 kHz square-wave output.

FREQUENCY DOUBLER

In a digital system, it is a relatively simple matter to divide by any integer. However, multiplying by an integer is quite another story especially if operation over a wide frequency range and waveform symmetry are required.

A frequency doubler that satisfies the above requirements is shown in Figure 10. A compar-

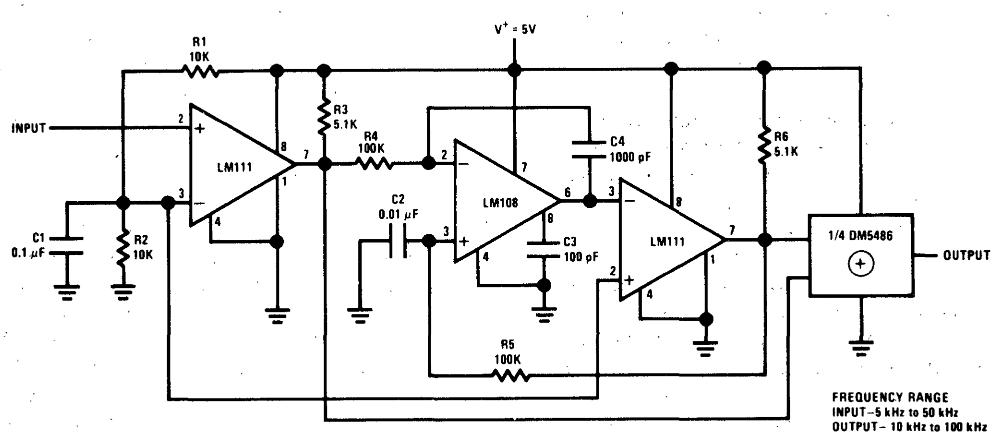

FIGURE 10. Frequency Doubler

ator is used to shape the input signal and feed it to an integrator. The shaping is required because the input to the integrator must swing between the supply voltage and ground to preserve symmetry in the output waveform. An LM108 op amp, that works from the 5V logic supply, serves as the integrator. This feeds a triangular waveform to a second comparator that detects when the waveform goes through a voltage equal to its average value. Hence, as shown in Figure 11, the output

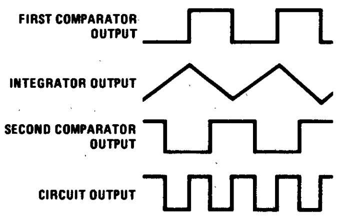

FIGURE 11. Waveforms for the Frequency Doubler

of the second comparator is delayed by half the duration of the input pulse. The two comparator outputs can then be combined through an exclusive-OR gate to produce the double-frequency output.

With the component values shown, the circuit operates at frequencies from 5 kHz to 50 kHz. Lower frequency operation can be secured by increasing both C_1 and C_2.

APPLICATION HINTS

One of the problems encountered in using earlier IC comparators like the LM710 or LM106 was that they were prone to erratic operation caused by oscillations. This was a direct result of the high speed of the devices, which made it mandatory to provide good input-output isolation and low-inductance bypassing on the supplies. These oscillations could be particularly puzzling when they occurred internally, showing up at the external terminals only as erratic dc characteristics.

In general, the LM111 is less susceptible to spurious oscillations both because of its lower speed (200 ns response time vs 40 ns) and because of its better power supply rejection. Feedback between the output and the input is a lesser problem with a given source resistance. However, the LM111 can operate with source resistances that are orders of magnitude higher than the earlier devices, so stray coupling between the input and output should be minimized. With source resistances between 1 kΩ and 10 kΩ, the impedance (both capacitive and resistive) on both inputs should be made equal, as this tends to reject the signal fed back. Even so, it is difficult to completely eliminate oscillations in the linear region with source resistances above 10 kΩ, because the 1 MHz open loop gain of the comparator is about 80 dB. However, this does not affect the dc characteristics and is not a problem unless the input signal dwells within 200 μV of the transition level. But if the oscillation does cause difficulties, it can be eliminated with a small amount of positive feedback around the comparator to give a 1 mV hysteresis.

Stray coupling between the output and the balance terminals can also cause oscillations, so an attempt should be made to keep these leads apart. It is usually advisable to tie the balance pins together to minimize the effect of this feedback. If balancing is used, the same result can be accomplished by connecting a 0.1 μF capacitor between these pins.

Normally, individual supply bypasses on every device are unnecessary, although long leads between the comparator and the bypass capacitors are definitely not recommended. If large current spikes are injected into the supplies in switching the output, bypass capacitors should be included at these points.

When driving the inputs from a low impedance source, a limiting resistor should be placed in series with the input lead to limit the peak current to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Low impedance sources do not cause a problem unless their output voltage exceeds the negative supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

Large capacitors on the input (greater than 0.1 μF) should be treated as a low source impedance and isolated with a resistor. A charged capacitor can hold the inputs outside the supply voltage if the supplies are abruptly shut off.

Precautions should be taken to insure that the power supplies for this or any other IC never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC can conduct excessive current, fuzing internal aluminum interconnects. This usually takes more than 0.5A. If there is a possibility of reversal, clamp diodes with an adequate peak current rating should be installed across the supply bus.

No attempt should be made to operate the circuit with the ground terminal at a voltage exceeding either supply voltage. Further, the 50V output-voltage rating applies to the potential between the output and the V^- terminal. Therefore, if the comparator is operated from a negative supply, the maximum output voltage must be reduced by an amount equal to the voltage on the V^- terminal.

The output circuitry is protected for shorts across the load. It will not, for example, withstand a short to a voltage more negative than the ground terminal. Additionally, with a sustained short, power dissipation can become excessive if the voltage across the output transistor exceeds about 10V.

The input terminals can exceed the positive supply voltage without causing damage. However, the 30V maximum rating between the inputs and the V^- terminal must be observed. As mentioned earlier, the inputs should not be driven more negative than the V^- terminal.

CONCLUSIONS

A versatile voltage comparator that can perform many of the precision functions required in digital systems has been produced. Unlike older comparators, the IC can operate from the same supply voltage as the digital circuits. The comparator is particularly useful in circuits requiring considerable sensitivity and accuracy, such as threshold detectors for low level sensors, data transmission circuits or stable oscillators and multivibrators.

The comparator can also be used in many analog systems. It operates from standard ±15V op amp supplies, and its dc accuracy equals some of the best op amps. It is also an order of magnitude faster than op amps used as comparators.

The new comparator is considerably more flexible than older devices. Not only will it drive RTL, DTL and TTL logic; but also it can interface with MOS logic or deliver ±15V to FET analog switches. The output can switch 50V, 50 mA loads, making it useful as a driver for relays, lamps or light-emitting diodes. Further, a unique output stage enables it to drive loads referred to either supply or to ground and provide ground isolation between the comparator inputs and the load.

The LM111 is a plug-in replacement for comparators like the LM710 and LM106 in applications where speed is not of prime concern. Compared to its predecessors in other respects, it has many improved electrical specifications, more design flexibility and fewer application problems.

February 1971

IC PROVIDES ON-CARD REGULATION FOR LOGIC CIRCUITS

INTRODUCTION

Because of the relatively high current requirements of digital systems, there are a number of problems associated with using one centrally-located regulator. Heavy power busses must be used to distribute the regulated voltage. With low voltages and currents of many amperes, voltage drops in connectors and conductors can cause an appreciable percentage change in the voltage delivered to the load. This is aggravated further with TTL logic, as it draws transient currents many times the steady-state current when it switches.

These problems have created a considerable interest in on-card regulation, that is, to provide local regulation for the subsystems of the computer. Rough preregulation can be used, and the power distributed without excessive concern for line drops. The local regulators then smooth out the voltage variations due to line drops and absorb transients.

A monolithic regulator is now available to perform this function. It is quite simple to use in that it requires no external components. The integrated circuit has three active leads—input, output and ground—and can be supplied in standard transistor power packages. Output currents in excess of 1A can be obtained. Further, no adjustments are required to set up the output voltage, and overload protection is provided that makes it virtually impossible to destroy the regulator. The simplicity of the regulator, coupled with low-cost fabrication and improved reliability of monolithic circuits, now makes on-card regulation quite attractive.

DESIGN CONCEPTS

A useful on-card regulator should include everything within one package—including the power-control element, or pass transistor. The author has previously advanced arguments against including the pass transistor in an integrated circuit regulator.[1] First, there are no standard multi-lead power packages. Second, integrated circuits necessarily have a lower maximum operating temperature, because they contain low-level circuitry. This means that an IC regulator needs a more massive heat sink. Third, the gross variations in chip temperature due to dissipation in the pass transistors worsen load and line regulation. However, for a logic-card regulator, these arguments can be answered effectively.

For one, if the series pass transistor is put on the chip, the integrated circuit need only have three terminals. Hence, an ordinary transistor power package can be used. The practicality of this approach depends on eliminating the adjustments usually required to set up the output voltage and limiting current for the particular application, as external adjustments require extra pins. A new solid-state reference, to be described later, has sufficiently-tight manufacturing tolerances that output voltages do not always have to be individually trimmed. Further, thermal overload protection can protect an IC regulator for virtually any set of operating conditions, making current-limit adjustments unnecessary.

Thermal protection limits the maximum junction temperature and protects the regulator regardless of input voltage, type of overload or degree of heat sinking. With an external pass transistor, there is no convenient way to sense junction temperature so it is much more difficult to provide thermal limiting. Thermal protection is, in itself, a very good reason for putting the pass transistor on the chip.

When a regulator is protected by current limiting alone, it is necessary to limit the output current to a value substantially lower than is dictated by dissipation under normal operating conditions to prevent excessive heating when a fault occurs. Thermal limiting provides virtually absolute protection for any overload condition. Hence, the maximum output current under normal operating conditions can be increased. This tends to make up for the fact that an IC has a lower maximum junction temperature than discrete transistors.

Additionally, the 5V regulator works with relatively low voltage across the integrated circuit. Because of the low voltage, the internal circuitry can be operated at comparatively high currents without causing excessive dissipation. Both the low voltage and the larger internal currents permit higher junction temperatures. This can also reduce the heat sinking required—especially for commercial-temperature-range parts.

Lastly, the variations in chip temperature caused by dissipation in the pass transistor do not cause serious problems for a logic-card regulator. The tolerance in output voltage is loose enough that it is relatively easy to design an internal reference that is much more stable than required, even for temperature variations as large as 150°C.

CIRCUIT DESCRIPTION

The internal voltage reference for this logic-card regulator is probably the most significant departure from standard design techniques. Temperature-compensated zener diodes are normally used for the reference. However, these have breakdown voltages between 7V and 9V which puts a lower limit on the input voltage to the regulator. For low voltage operation, a different kind of reference is needed.

The reference in the LM109 does not use a zener diode. Instead, it is developed from the highly-predictable emitter-base voltage of the transistors. In its simplest form, the reference developed is equal to the energy-band-gap voltage of the semiconductor material. For silicon, this is 1.205V, so the reference need not impose minimum input voltage limitations on the regulator. An added advantage of this reference is that the output voltage is well determined in a production environment so that individual adjustment of the regulators is frequently unnecessary.

A simplified version of this reference is shown in Figure 1. In this circuit, Q_1 is operated at a

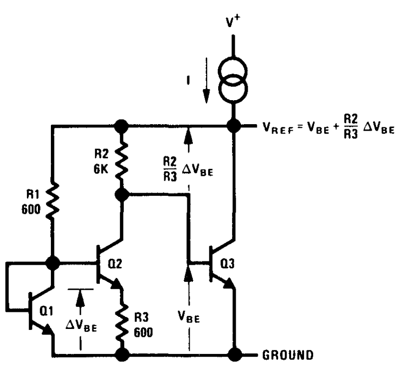

Figure 1. The Low Voltage Reference in One of Its Simpler Forms.

relatively high current density. The current density of Q_2 is about ten times lower, and the emitter-base voltage differential (ΔV_{BE}) between the two devices appears across R_3. If the transistors have high current gains, the voltage across R_2 will also be proportional to ΔV_{BE}. Q_3 is a gain stage that will regulate the output at a voltage equal to its emitter base voltage plus the drop across R_2. The emitter base voltage of Q_3 has a negative temperature coefficient while the ΔV_{BE} component across R_2 has a positive temperature coefficient. It will be shown that the output voltage will be temperature compensated when the sum of the two voltages is equal to the energy-band-gap voltage.

Conditions for temperature compensation can be derived starting with the equation for the emitter-base voltage of a transistor which is[2]

$$V_{BE} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{nkT}{q}\log_e\frac{T_0}{T} + \frac{kT}{q}\log_e\frac{I_C}{I_{C0}}, \qquad (1)$$

Where V_{g0} is the extrapolated energy-band-gap voltage for the semiconductor material at absolute zero, q is the charge of an electron, n is a constant which depends on how the transistor is made (approximately 1.5 for double-diffused, NPN transistors), k is Boltzmann's constant, T is absolute temperature, I_C is collector current and V_{BE0} is the emitter-base voltage at T_0 and I_{C0}.

The emitter-base voltage differential between two transistors operated at different current densities is given by[3]

$$\Delta V_{BE} = \frac{kT}{q}\log_e\frac{J_1}{J_2}, \qquad (2)$$

where J is current density.

Referring to Equation (1), the last two terms are quite small and are made even smaller by making I_C vary as absolute temperature. At any rate, they can be ignored for now because they are of the same order as errors caused by nontheoretical behavior of the transistors that must be determined empirically.

If the reference is composed of V_{BE} plus a voltage proportional to ΔV_{BE}, the output voltage is obtained by adding (1) in its simplified form to (2):

$$V_{ref} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{kT}{q}\log_e\frac{J_1}{J_2}. \qquad (3)$$

Differentiating with respect to temperature yields

$$\frac{\partial V_{ref}}{\partial T} = -\frac{V_{g0}}{T_0} + \frac{V_{BE0}}{T_0} + \frac{k}{q}\log_e\frac{J_1}{J_2}. \qquad (4)$$

For zero temperature drift, this quantity should equal zero, giving

$$V_{g0} = V_{BE0} + \frac{kT_0}{q}\log_e\frac{J_1}{J_2}. \qquad (5)$$

The first term on the right is the initial emitter-base voltage while the second is the component proportional to emitter-base voltage differential. Hence, if the sum of the two are equal to the energy-band-gap voltage of the semiconductor, the reference will be temperature-compensated.

A simplified schematic for a 5V regulator is given in Figure 2. The circuitry produces an output voltage that is approximately four times the basic reference voltage. The emitter-base voltage of Q_3, Q_4, Q_5 and Q_8 provide the negative-temperature-coefficient component of the output voltage. The voltage dropped across R_3 provides the positive-temperature-coefficient component. Q_6 is operated at a considerably higher current density than Q_7, producing a voltage drop across R_4 that is proportional to the emitter-base voltage differential of the two transistors. Assuming large current gain in the transistors, the voltage drop across R_3 will be proportional to this differential, so a temperature-compensated-output voltage can be obtained.

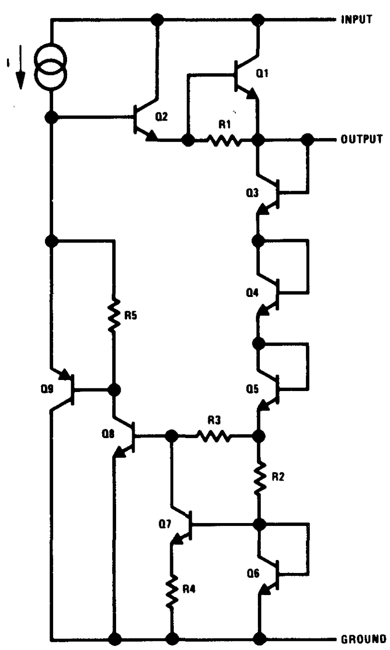

Figure 2. Schematic Showing Essential Details of The 5V Regulator.

In this circuit, Q_8 is the gain stage providing regulation. Its effective gain is increased by using a vertical PNP, Q_9, as a buffer driving the active collector load represented by the current source. Q_9 drives a modified Darlington output stage (Q_1 and Q_2) which acts as the series pass element. With this circuit, the minimum input voltage is not limited by the voltage needed to supply the reference. Instead, it is determined by the output voltage and the saturation voltage of the Darlington output stage.

Figure 3 shows a complete schematic of the LM109, 5V regulator. The ΔV_{BE} component of the output voltage is developed across R_8 by the collector current of Q_7. The emitter-base voltage differential is produced by operating Q_4 and Q_5 at high current densities while operating Q_6 and Q_7 at much lower current levels. The extra transistors improve tolerances by making the emitter-base voltage differential larger. R_3 serves to compensate the transconductance[4] of Q_5, so that the ΔV_{BE} component is not affected by changes in the regulator output voltage or the absolute value of components.

The voltage gain for the regulating loop is provided by Q_{10}, with Q_9 buffering its input and Q_{11} its output. The emitter base voltage of Q_9 and Q_{10} is added to that of Q_{12} and Q_{13} and the drop across R_8 to give a temperature-compensated, 5V output. An emitter-base-junction capacitor, C_1, frequency compensates the circuit so that it is stable even without a bypass capacitor on the output.

The active collector load for the error amplifier is Q_{17}. It is a multiple-collector lateral PNP[4]. The output current is essentially equal to the collector current of Q_2, with current being supplied to the zener diode controlling the thermal shutdown, D_2, by an auxiliary collector. Q_1 is a collector FET[4] that, along with R_1, insures starting of the regulator under worst-case conditions.

The output current of the regulator is limited when the voltage across R_{14} becomes large enough to turn on Q_{14}. This insures that the output current cannot get high enough to cause the pass transistor to go into secondary breakdown or damage the aluminum conductors on the chip. Further, when the voltage across the pass transistor exceeds 7V, current through R_{15} and D_3 reduces the limiting current, again to minimize the

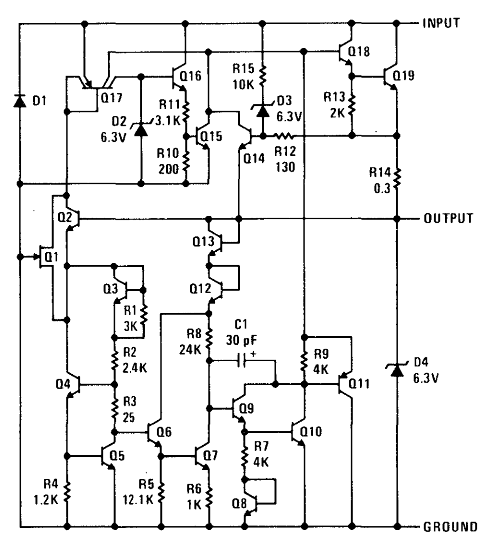

Figure 3. Detailed Schematic of The Regulator.

chance of secondary breakdown. The performance of this protection circuitry is illustrated in Figure 4.

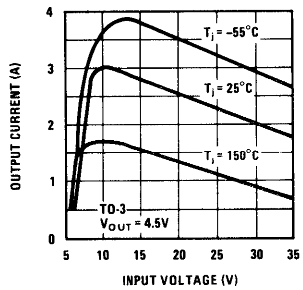

Figure 4. Current-Limiting Characteristics.

Even though the current is limited, excessive dissipation can cause the chip to overheat. In fact, the dominant failure mechanism of solid state regulators is excessive heating of the semiconductors, particularly the pass transistor. Thermal protection attacks the problem directly by putting a temperature regulator on the IC chip. Normally, this regulator is biased below its activation threshold; so it does not affect circuit operation. However, if the chip approaches its maximum operating temperature, for any reason, the temperature regulator turns on and reduces internal dissipation to prevent any further increase in chip temperature.

The thermal protection circuitry develops its reference voltage with a conventional zener diode, D_2. Q_{16} is a buffer that feeds a voltage divider, delivering about 300 mV to the base of Q_{15} at 175°C. The emitter-base voltage, Q_{15}, is the actual temperature sensor because, with a constant voltage applied across the junction, the collector current rises rapidly with increasing temperature.

Although some form of thermal protection can be incorporated in a discrete regulator, IC's have a distinct advantage: the temperature sensing device detects increases in junction temperature within milliseconds. Schemes that sense case or heat-sink temperature take several seconds, or longer. With the longer response times, the pass transistor usually blows out before thermal limiting comes into effect.

Another protective feature of the regulator is the crowbar clamp on the output. If the output voltage tries to rise for some reason, D_4 will break down and limit the voltage to a safe value. If this rise is caused by failure of the pass transistor such that the current is not limited, the aluminum conductors on the chip will fuse, disconnecting the load. Although this destroys the regulator, it does protect the load from damage. The regulator is also designed so that it is not damaged in the event the unregulated input is shorted to ground when there is a large capacitor on the output. Further, if the input voltage tries to reverse, D_1 will clamp this for currents up to 1A.

The internal frequency compensation of the regulator permits it to operate with or without a bypass capacitor on the output. However, an output capacitor does improve the transient response and reduce the high frequency output impedance. A plot of the output impedance in Figure 5 shows that it remains low out to 10 kHz even without a capacitor. The ripple rejection also remains high out to 10 kHz, as shown in Figure 6. The irregularities in this curve around 100 Hz are caused by thermal feedback from the pass transistor to the reference circuitry. Although an output capacitor is not required, it is necessary to bypass the input of the regulator with at least a 0.22 μF capacitor to prevent oscillations under all conditions.

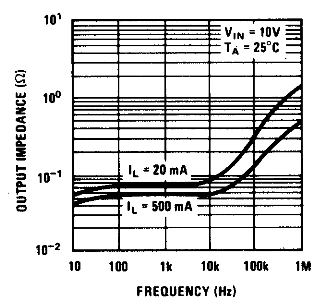

Figure 5. Plot of Output Impedance As A Function of Frequency.

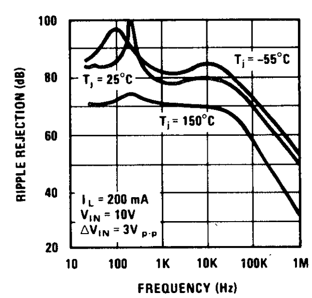

Figure 6. Ripple Rejection of The Regulator.

Figure 7 is a photomicrograph of the regulator chip. It can be seen that the pass transistors, which must handle more than 1A, occupy most of the chip area. The output transistor is actually broken into segments. Uniform current distribution is insured by also breaking the current limit resistor into segments and using them to equalize the currents. The overall electrical performance of this IC is summarized in Table 1.

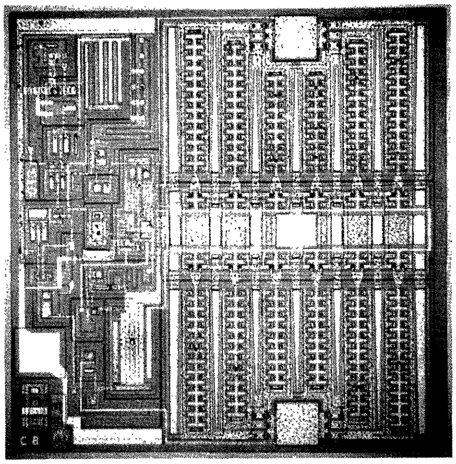

Figure 7. Photomicrograph of The Regulator Shows That High Current Pass Transistor (Right) Takes More Area Than Control Circuitry (Left).

PARAMETER	CONDITIONS	TYP
Output Voltage		5.0V
Output Current		1.5A
Output Resistance		0.03Ω
Line Regulation	$7.0V \leq V_{IN} \leq 35V$	0.005%/V
Temperature Drift	$-55°C \leq T_A \leq 125°C$	0.02%/°C
Minimum Input Voltage	$I_{OUT} = 1A$	6.5V
Output Noise Voltage	$10\ Hz \leq f \leq 100\ kHz$	40 μV
Thermal Resistance Junction to Case	LM109H (TO-5) LM109K (TO-3)	15°C/W 3°C/W

Table 1. Typical Characteristics of The Logic-Card Regulator: $T_A = 25°C$.

APPLICATIONS

Because it was designed for virtually foolproof operation and because it has a singular purpose, the LM109 does not require a lot of application information, as do most other linear circuits. Only one precaution must be observed: it is necessary to bypass the unregulated supply with a 0.22 μF capacitor, as shown in Figure 8, to prevent

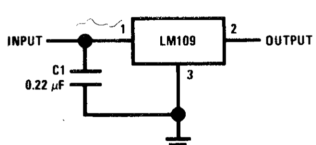

Figure 8. Fixed 5V Regulator

oscillations that can cause erratic operation. This, of course, is only necessary if the regulator is located an appreciable distance from the filter capacitors on the output of the dc supply.

Although the LM109 is designed as a fixed 5V regulator, it is also possible to use it as an adjustable regulator for higher output voltages. One circuit for doing this is shown in Figure 9.

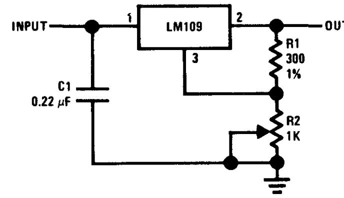

Figure 9. Using The LM109 As An Adjustable-Output Regulator.

The regulated output voltage is impressed across R_1, developing a reference current. The quiescent current of the regulator, coming out of the ground terminal, is added to this. These combined currents produce a voltage drop across R_2 which raises the output voltage. Hence, any voltage above 5V can be obtained as long as the voltage across the integrated circuit is kept within ratings.

The LM109 was designed so that its quiescent current is not greatly affected by variations in input voltage, load or temperature. However, it is not completely insensitive, as shown in Figures 10 and 11, so the changes do affect regulation somewhat. This tendency is minimized by making the reference current through R_1 larger than the quiescent current. Even so, it is difficult to get the regulation tighter than a couple percent.

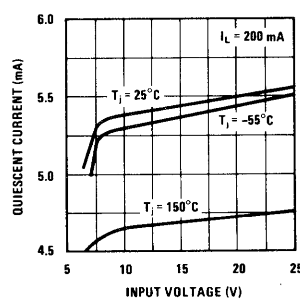

Figure 10. Variation of Quiescent Current With Input Voltage At Various Temperatures.

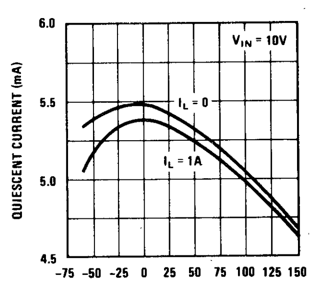

Figure 11. Variation of Quiescent Current With Temperature For Various Load Currents.

The LM109 can also be used as a current regulator as is shown in Figure 12. The regulated output voltage is impressed across R_1, which determines the output current. The quiescent current is added to the current through R_1, and this puts a lower limit of about 10 mA on the available output current.

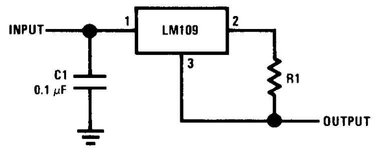

Figure 12. Current Regulator.

The increased failure resistance brought about by thermal overload protection make the LM109 attractive as the pass transistor in other regulator circuits. A precision regulator that employs the IC thusly is shown in Figure 13. An operational amplifier compares the output voltage with the output voltage of a reference zener. The op amp controls the LM109 by driving the ground terminal through an FET.

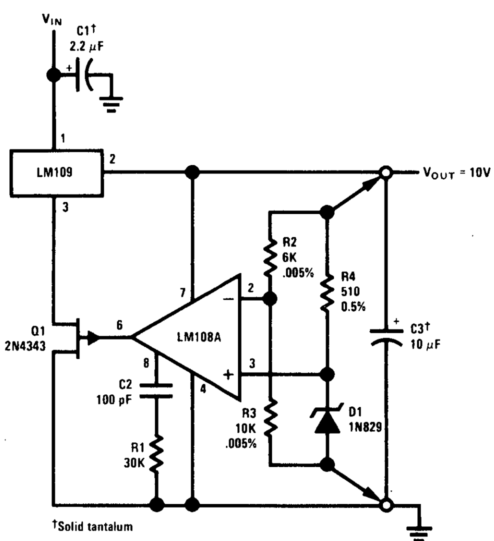

Figure 13. High Stability Regulator.

The load and line regulation of this circuit is better than 0.001%. Noise, drift and long term stability are determined by the reference zener, D_1. Noise can be reduced by inserting 100 kΩ, 1% resistors in series with both inputs of the op amp and bypassing the non-inverting input to ground. A 100 pF capacitor should also be included between the output and the inverting input to prevent frequency instability. Temperature drift can be reduced by adjusting R_4, which determines the zener current, for minimum drift. For best performance, remote sensing directly to the load terminals, as shown in the diagram, should be used.

CONCLUSIONS

The LM109 performs a complete regulation function on a single silicon chip, requiring no external components. It makes use of some unique advantages of monolithic construction to achieve performance advantages that cannot be obtained in discrete-component circuits. Further, the low cost of the device suggests its use in applications where single-point regulation could not be justified previously.

Thermal overload protection significantly improves the reliability of an IC regulator. It even protects the regulator for unforseen fault conditions that may occur in field operation. Although this can be accomplished easily in a monolithic regulator, it is usually not completely effective in a discrete or hybrid device.

The internal reference developed for the LM109 also advances the state of the art for regulators. Not only does it provide a low voltage, temperature-compensated reference for the first time, but also it can be expected to have better long term stability than conventional zeners. Noise is inherently much lower, and it can be manufactured to tighter tolerances.

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June 1971

THE PHASE LOCKED LOOP IC AS A COMMUNICATION SYSTEM BUILDING BLOCK

INTRODUCTION

The phase locked loop has been found to be a useful element in many types of communication systems. It is used in two fundamentally different ways: (1) as a demodulator, where it is used to follow phase or frequency modulation and (2) to track a carrier or synchronizing signal which may vary in frequency with time.

When operating as a demodulator, the phase locked loop may be thought of as a matched filter operating as a coherent detector. When used to track a carrier, it may be thought of as a narrow-band filter for removing noise from a signal.

Recently, a phase locked loop has been built on a monolithic integrated circuit, incorporating the basic elements necessary for operation: a double balanced phase detector and a highly linear voltage controlled oscillator, the frequency of which can be varied with either a resistor or capacitor.

BASIC PHASE LOCK LOOP OPERATION

Figure 1 shows the basic blocks of a phase locked loop. The input signal e_i is a sinusoid of arbitrary frequency, while the VCO output signal, e_o, is a sinsuoid of the same frequency as the input but of arbitrary phase. If

$$e_i = \sqrt{2}\ E_i\ [\sin \omega_o t + \theta_1(t)] \qquad (1)$$

$$e_o = \sqrt{2}\ E_o\ [\sin \omega_o t + \theta_2(t)] \qquad (2)$$

the output of the multiplier (phase detector) is

$$\begin{aligned} e_d = e_i \cdot e_o &= 2E_iE_o \sin [\omega_o t + \theta_1(t)] \cdot \cos [\omega_o t + \theta_2(t)] \\ &= E_iE_o \sin [\theta_1(t) - \theta_2(t)] \\ &\quad + \sin [2\ \omega_o t + \theta_1(t) + \theta_2(t)] \end{aligned} \qquad (3)$$

the low pass filter of the loop removes the ac components of the multiplier output; the dc term is seen to be a function of the phase angle between the VCO and the input signal.

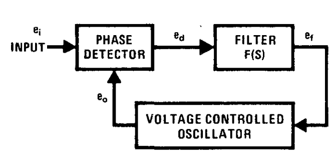

FIGURE 1. Basic Phase Locked Loop

The output of the VCO is related to its input control voltage by

$$\dot{\theta}_2(t) = K_o e_f \qquad (4)$$

for $e_f = 0$, let $\dot{\theta}_2 = \omega\theta$, then

$$\theta_2(t) = \int e_f(t)\ dt \qquad (5)$$

It can be seen that the action of the VCO is that of an integrator in the feedback loop when the phase locked loop is considered in servo theory.

A better understanding of the operation of the loop may be obtained by considering that initially, the loop is not in lock, but that the frequency of the input signal e_i and VCO e_o are very close in frequency. Under these conditions e_d will be a beat note, the frequency of which is equal to the frequency difference of e_o and e_i. This signal is also applied to the VCO input, since it is low enough to pass through the filter. The instantaneous frequency of the VCO is therefore changing and at some point in time, if the VCO frequency equals the input frequency, lock will result. At this instant, e_f will assume a level sufficient to hold the VCO frequency in lock with the input frequency. If the tuning of the VCO is changed (such as by varying the value of the tuning capacitor) the frequency output of the VCO will attempt to change; however, this will result in an instantaneous change in phase angle between e_i and e_o, resulting in a change in the dc level of e_d which will act to maintain frequency lock: no average frequency change will result.

Similarly, if e_i changes frequency, an instantaneous change will result in a phase change between e_i and e_o and hence a dc level change in e_d. This level shift will change the frequency of the VCO to maintain lock.

The amount of phase error resulting from a given frequency shift can be found by knowing the "dc" loop gain of the system. Considering the phase detector to have a transfer function:

$$E_d = K_D(\theta_1 - \theta_2)$$

and the voltage controlled oscillator to have a transfer function:

$$\dot{\theta}_2 = K_o\ e_f \qquad (6)$$

or taking the Laplace transform

$$\theta_2(s) = \frac{K_o e_f}{s} \qquad (7)$$

the phase of the VCO output will be proportional to the integral of the control voltage.

Combining these equations:

$$\frac{\theta_2(s)}{\theta_1(s)} = \frac{K_o K_d F(s)}{s + K_o K_D F(s)} \qquad (8)$$

$$\frac{\theta_1(s) - \theta_2(s)}{\theta_1(s)} = \frac{s}{s + K_o K_D F(s)} \qquad (9)$$

Application of the final value theorem of Laplace transforms yields

$$\lim_{t \to \infty} \theta_1(s) - \theta_2(s) = \lim_{s \to o} \frac{s^2 \theta_1(s)}{s + K_o K_D F(s)} \qquad (10)$$

With a step change in phase of the input $\Delta\theta_1$, the Laplace transform of the input is

$$\theta_1(s) = \frac{\Delta\theta_1}{s} \text{ which gives } \theta_e(s) = \theta_1(s) - \theta_2(s)$$

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to o} \frac{s\Delta\theta_1}{s + K_o K_D F(s)} = o \qquad (11)$$

the loop will eventually track out any change of input phase, and there will be no phase error in the steady state solution.

If the input is a step in frequency, of magnitude $\Delta\omega$, the change in input phase will be a ramp:

$$\theta_1(s) = \Delta\omega / s^2$$

substitution of this value θ, into (10) results in

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to o} \frac{\Delta\omega}{s + K_o K_D F(s)} = \frac{\Delta\omega}{K_o K_D F(o)} \qquad (12)$$

this result shows the resulting phase error is dependent on the magnitude of the frequency step and the "dc" loop gain $K_o K_D$, which is also called the velocity error coefficient K_v. It should be noted that the dimensions of $K_o K_D$ are 1/sec. This can also be seen by considering K_D = volts/radian, while K_o = radians/sec/volt. The product is

$$\frac{\text{volts}}{\text{radian}} \times \frac{\text{radians/sec}}{\text{volt}} = \frac{1}{\text{sec}}$$

this can be thought of as the "dc" loop gain. (Note that additional dc gain between the phase detector and the voltage controlled oscillator will increase the loop gain and hence reduce the steady state phase error resulting from a change in frequency of the input.)

THE LOOP FILTER

In working with phase locked loops, it is necessary to consider not only the "dc" performance described above, but the "ac" or transient performance which is governed by the components of the loop filter placed between the phase detector and the voltage controlled oscillator. In fact, it is this loop filter that makes the phase locked loop so powerful: only a resistor and capacitor are all that is needed to produce an arbitrarily narrow bandwidth at any selected center frequency.

The simplest filter is a single capacitor, Figure 2, and is used for wide bandwidth applications, such as where wideband data modulation must be followed. The transfer function of the filter is simply:

$$\frac{e_f}{e_d} = \frac{1}{1 + sR_1C_1} \qquad (13)$$

substitution into (8) results in

$$\frac{\theta_2(s)}{\theta_1(s)} = \frac{K_o K_D / \tau_1}{s^2 + s/\tau_1 + K_o K_D / \tau_1} \qquad (14)$$

$$\tau_1 = R_1 C_1$$

In terms of servo theory, the damping factor and natural frequencies are

$$\omega_n = \left[\frac{K_o K_D}{R_1 C_1}\right]^{1/2} \qquad (15)$$

$$\zeta = \left[\frac{1}{2\,(R_1 C_1 K_o K_D)}\right]^{1/2} \qquad (16)$$

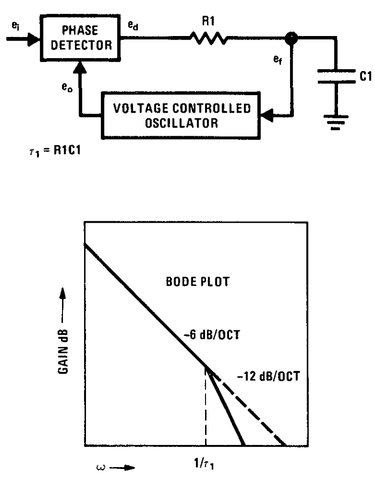

FIGURE 2. Phase Locked Loop with Simple Filter

From this it can be seen that large time constants for R_1C_1 or high loop gain will reduce the damping factor and hence decrease stability. Therefore, if a narrow bandwidth is desired, the damping factor will become very small and instability will result. It is not possible to adjust bandwidth, loop gain, and damping independently with this simple filter.

With the addition of a damping resistor R_2 as shown in Figure 3, it is possible to choose bandwidth, damping factor and loop gain independently; the transfer function of this filter is

$$\frac{e_d}{e_f} = \frac{s\tau_2 + 1}{s(\tau_1 + \tau_2)} \qquad (17)$$

the loop transfer function becomes:

$$\frac{\theta_2(s)}{\theta_1(s)} =$$

$$\frac{K_oK_D\,(s\tau_2 + 1)\,(\tau_1 + \tau_2)}{s^2 + s(1 + K_oK_d\,\tau_2)/(\tau_1 + \tau_2) + K_oK_D/(\tau_1 + \tau_2)} \qquad (18)$$

the loop natural frequency is

$$\omega_n = \left[\frac{K_oK_D}{\tau_1 + \tau_2}\right]^{1/2} \qquad (19)$$

while the damping factor becomes

$$\delta = \frac{1}{2}\left[\frac{K_oK_D}{\tau_1 + \tau_2}\right]^{1/2}\left[\tau_2 + \frac{1}{K_oK_D}\right] \qquad (20)$$

$$\simeq \frac{\omega_n\,\tau_2}{2} \qquad (21)$$

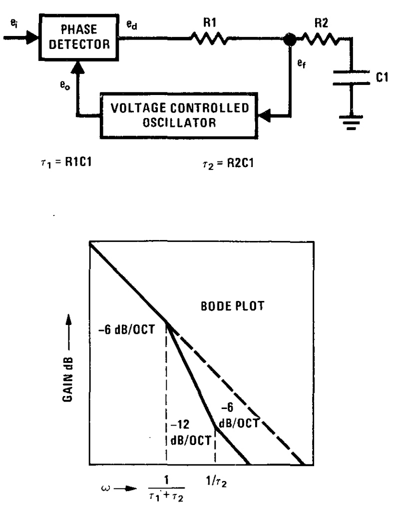

FIGURE 3. Phase Locked Loop with Damping Resistor Added

In practice, for a fixed loop gain K_oK_D, the natural frequency of the loop may be chosen and will be dependent mainly on τ_1, since $\tau_2 << \tau_1$ in most cases. Then, according to (21), damping may be determined by τ_2 and for all practical purposes, will be an independent adjustment. These equations are plotted in Figures 4 and 5 and may be used for design purposes.

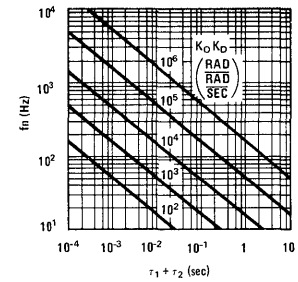

FIGURE 4. Filter Time Constant vs Natural Frequency

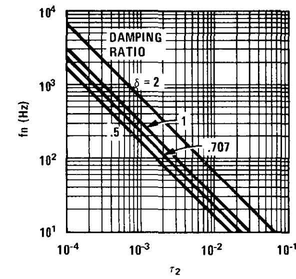

FIGURE 5. Damping Time Constant vs Natural Frequency

DESIGN CONSIDERATIONS

Considering the above discussion, there are really two primary considerations in designing a phase locked loop. The use to which the loop is to be put will affect the design criterion of the loop components. The two primary factors to consider are:

1. Loop gain. As pointed out previously, this affects the phase error between the input signal and the voltage controlled oscillator for a given frequency shift of the input signal. It also determines the "hold in range" of the loop providing no components of the loop go into limiting or saturation. This is because the loop will remain in lock as long as the phase difference between the input and the VCO is less than ±90°. The higher the loop gain, the further the input can change in frequency before the 90° phase error is reached. The hold in range is

$$\Delta\omega_H = \pm K_oK_D \qquad (22)$$

   (providing saturation or limiting does not occur).

2. Natural Frequency. The bandwidth of the loop is determined by the filter components R_1, R_1 and C_1 and the loop gain. Since the loop gain is normally selected by the criterion in 1. above, the filter components are used to select the bandwidth. The selection of loop bandwidth may be governed by several things: noise bandwidth, modulation rates if the loop is to be

used as an FM demodulator, pull-in time and hold-in range. There are two conflicting requirements that will have an affect on loop bandwidth:

(a) Loop bandwidth must be as narrow as possible to minimize output phase jitter due to external noise.

(b) The loop bandwidth should be made as large as possible to minimize transient error due to signal modulation, output jitter due to internal oscillator (VCO) noise, and to obtain best tracking and acquisition properties.

These two principles are in direct opposition and, depending on what it is that the loop is to accomplish, an optimum solution will lie somewhere between the two extremes.

If the phase locked loop is to be used to demodulate frequency modulation, the design should proceed with the criterion of b above. It is necessary to provide sufficient loop bandwidth to accommodate the expected modulation. It must be remembered that at all times, the loop must remain in lock, (peak phase error less than 90°), even under extremes of modulation, such as peaks or step changes in frequency.

For the case of sinusoidal frequency modulation, the peak phase error as a function of frequency deviation and damping factor is shown in Figure 6.

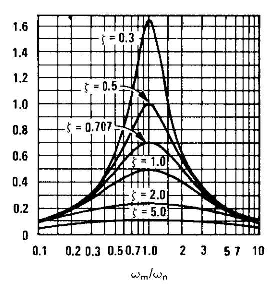

FIGURE 6. Steady-State Peak Phase Error Due to Sinusoidal FM (High-Gain, Second-Order Loop.)

It can be seen that the maximum phase error occurs when the modulating frequency ω_m equals the loop natural frequency ω_n; if the loop has been designed with a damping factor of .707, the peak phase error (in radians) will be .71 $\Delta\omega/\omega_n$ ($\Delta\omega$ = frequency deviation). From this plot, it is possible to choose ω_n for a given deviation and modulation frequency.

If the loop is to demodulate frequency shift keying (FSK), it must follow step changes in frequency. The filter components must then be chosen in accordance with the transient phase error shown in Figure 7. It must be remembered that the loop filter must be wide enough so the loop will not lose lock when a step change in frequency occurs: the greater the frequency step, the wider the loop filter must be to maintain lock.

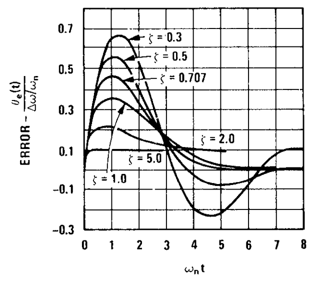

FIGURE 7. Transient Phase Error $\theta_e(t)$ Due to a Step in Frequency $\Delta\omega$. (Steady-State Velocity Error, $\Delta\omega/K_v$, Neglected.)

There is some frequency-step limit below which the loop does not skip cycles, but remains in lock, called the "pull-out frequency" ω_{po}. Viterbi has analyzed this and his results are shown in Figure 8, which plots normalized pull out frequency for various damping factors for high gain second order loops. Peak phase errors for other types of input signals are shown in Figures 8 and 9.

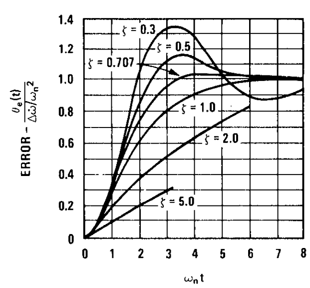

FIGURE 8. Transient Phase Error $\theta_e(t)$ Due to a Ramp in Frequency $\Delta\omega$. (Steady-State Acceleration Error, $\Delta\dot{\omega}/\omega_n^2$, included. Velocity Error, $\Delta\dot{\omega}t/K_v$, Neglected

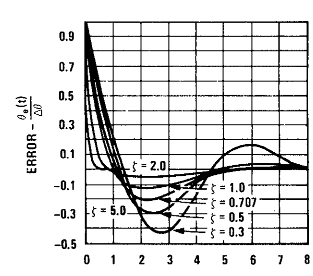

FIGURE 9. Phase Error $\theta_e(t)$ Due to a Step in Phase $\Delta\theta$

In designing loops to track a carrier or synchronizing signal, it is desirable to make the loop bandwidth narrow so that phase error due to external noise will be small. However, it is necessary to make the loop bandwidth wide enough so that any frequency jitter on the input signal will be followed.

NOISE PERFORMANCE

Since one of the main uses of phase locked loops is to demodulate or track signals in noise, it is helpful to look at how noise affects the operation of the phase locked loop.

The phase locked loop, as mentioned earlier, may be thought of as a filter with a fixed, adjustable bandwidth. We have seen how to calculate the loop natural frequency ω_n (15), (19), and the damping factor ζ (16), (20). Without going through a derivation, the loop noise bandwidth B_L may be shown to be

$$B_L = \int_0^\infty |H(j\omega)|^2 df = \frac{\omega_n}{2}\left[\zeta + \frac{1}{4\zeta}\right] \text{Hz} \quad (23)$$

for a high gain, second order loop. This equation is plotted in Figure 10. It should be noted that the dimensions of noise bandwidth are cycles per second while the dimensions of ω_n are radians per second.

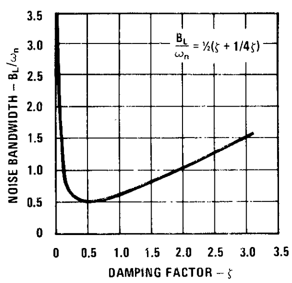

FIGURE 10. Loop-Noise Bandwidth (For High-Gain, Second-Order Loop)

Noise threshold is a difficult thing to analyze in a phase locked loop, since we are talking about a statistical quantity. Noise will show up in the input signal as both amplitude and phase modulation. It can be shown that near optimum performance of a phase locked loop can be obtained if a limiter is used ahead of the phase detector, or if the phase detector is allowed to operate in limiting. With the use of a limiter, amplitude modulation of the input signal by noise is removed, and the noise appears as phase modulation. As the input signal to noise ratio decreases, the phase jitter of the input signal due to noise increases, and the probability of losing lock due to instantaneous phase excersions will increase. In practice it is nearly impossible to acquire lock if the signal to noise ratio in the loop $(SNR)_L$ = 0 dB. In general, $(SNR)_L$ of +6 dB is needed for acquisition. If modulation or transient phase error is present, a higher signal to noise ratio is needed to acquire and hold lock.

A computer simulation performed by Sanneman and Rowbotham has shown the probability of skipping cycles for various loop signal to noise ratios for high gain, second order loops. Their data is shown in Figure 11.

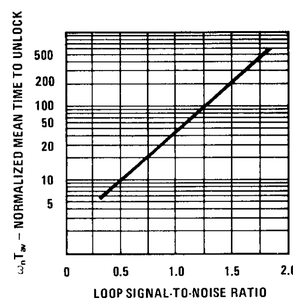

FIGURE 11. Unlock Behavior of High-Gain, Second-Order Loop, ζ = 0.707

When designing the loop filter components, enough bandwidth in the loop must be allowed for instantaneous phase change due to input noise. In the previous section, the filter was selected on the basis that the peak error due to modulation would be less than 90° (so the loop would not loose lock). However, if noise is present, the peak phase error will increase due to the noise. So if the loop is not to lose lock on these noise peaks, the peak allowable error due to modulation must be reduced to something less, on the order of 40° to 50°.

LOCKING

Initially, a loop is unlocked and the VCO is running at some frequency. If a signal is applied to the input, locking may or may not occur depending on several things.

If the signal is within the bandwidth of the loop filter, locking will occur without a beat note being generated or any cycles being skipped. This frequency is given by

$$\Delta\omega_L = \frac{K_o K_D \tau_2}{\tau_1 + \tau_2} \approx 2\zeta\omega_n \quad (24)$$

If the frequency of the input signal is further away from the VCO frequency, locking may still occur, with a beat note being generated. The greatest frequency that can be pulled in is called the "pull in frequency" and is found from the approximation

$$\Delta\omega_P \approx \sqrt{2}\,(2\zeta\omega_n K_o K_D - \omega_n^2)^{1/2} \quad (25)$$

which works well for moderate and high gain loops $(\omega_n/K_oK_D < .4)$.

An approximate expression for pull in time (the time required to achieve lock from some frequency offset $\Delta\omega$) is given by:

$$T_P \approx \frac{(\Delta\omega)^2}{2\zeta\omega_n^3}$$

A MONOLITHIC PHASE LOCKED LOOP

A complete phase locked loop has been built on a monolithic integrated circuit. It features a very linear voltage controlled oscillator and a double balanced phase detector.

A simplified schematic of this voltage controlled oscillator is shown in Figure 12. Q_2 is a voltage controlled current source whose collector current is a linear function of the control voltage e_f. Initially Q_5 is OFF and the collector current of Q_2 passes through D_2 and changes C in a linear fashion. The voltage across C is therefore a ramp, and continues to increase until Q_7 is turned ON; this turns OFF Q_8, causing Q_9 and Q_{11} to turn ON. This in turn turns ON Q_5. With Q_5 ON, the anode of D_1 is clamped close to $-V_{CC}$ and D_2 stops conducting, since its cathode is more positive than its anode.

All of the current supplied by Q_2 is diverted through D_1 and Q_3, which sets up an equal current in Q_4. This current is supplied by the charged capacitor C (which now discharges linearly), causing the voltage across it to decrease. This continues until a lower trip point is reached and Q_7 turns OFF and the cycle repeats. Due to the matching of Q_3 and Q_4, the charge current of C is equal to the discharge current and therefore the duty cycle is very nearly 50%. Figure 13 shows the wave forms at (1) and (2).

Figure 14 shows the double balanced phase detector and amplifier used in the microcircuit. Transistors Q_1 through Q_4 are switched with the output

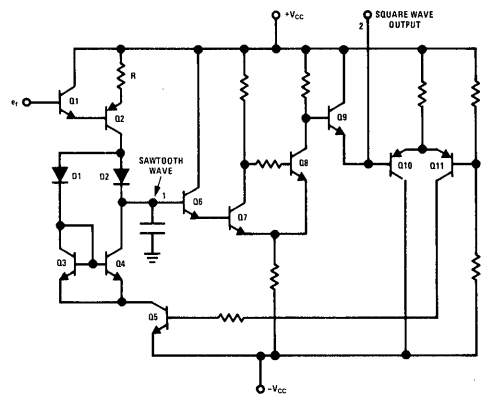

FIGURE 12. Simplified Voltage Controlled Oscillator

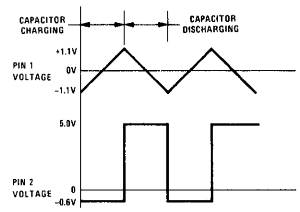

FIGURE 13. VCO Waveforms

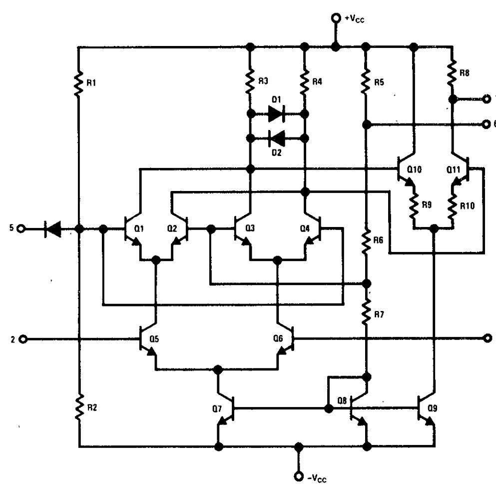

FIGURE 14. Phase Detector and Amplifier

of the VCO, while the input signal is applied to the bases of Q_5 and Q_6. The output current in resistors R_3 and R_4 is then proportional to the difference in phase between the VCO output and the input; the ac component of this current will be at twice the frequency of the VCO due to the full wave switching action transistors Q_1 through Q_4. The waveforms of Figure 15 illustrate how the phase detector works. Diodes D_1 and D_2 serve to limit the peak to peak amplitude of the collector voltage. The output of the phase detector is further amplified by Q_{10} and Q_{11}, and is taken as a voltage at pin 7.

R_8 serves as the resistive portion of the loop filter, and additional resistance and capacitance may be added here to fix the loop bandwidth. For use as an FM demodulator, the voltage at pin 7 will be the demodulated output; since the dc level here is fairly high, a reference voltage has been provided so that an operational amplifier with differential input can be used for additional gain and level shifting.

The complete microcircuit, called the LM565, is shown in Figure 16.

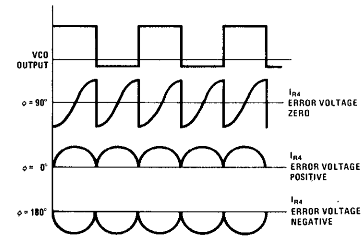

FIGURE 15. Phase Detector Waveforms, Showing Limit Cases for Phase Shift Between Input and VCO Signals

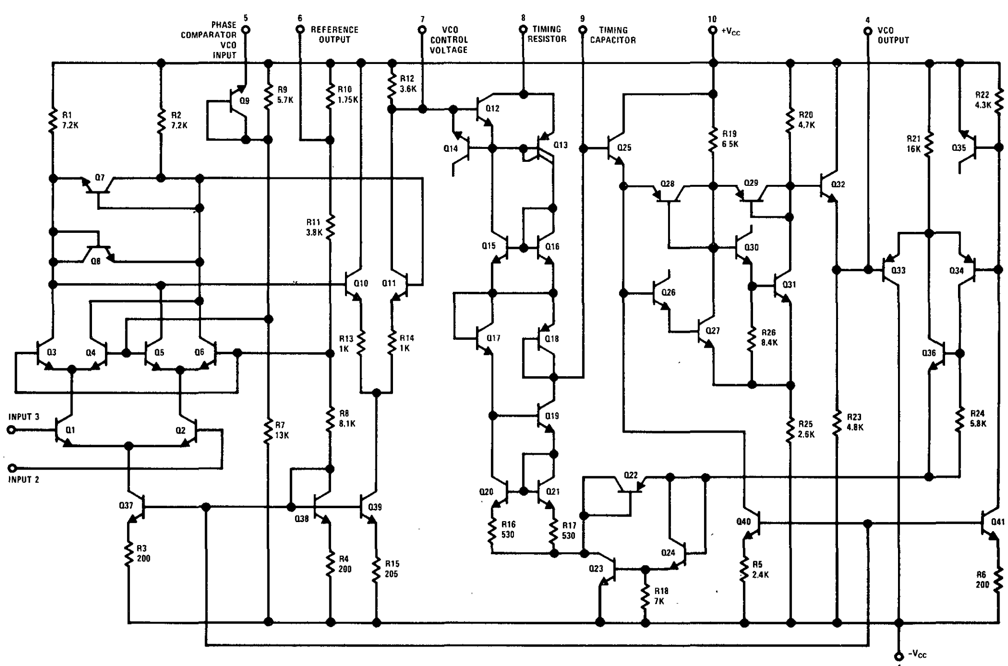

FIGURE 16. LM565 Phase Locked Loop

USING THE LM565

Some of the important operating characteristics of the LM565 are shown in the table below. (V_{CC} = ±6V, T_A = 25°C).

Phase Detector	
Input Impedance	5 kΩ
Input Level for Limiting	10 mV
Output Resistance	3.6 kΩ
Output Common Mode Voltage	4.5V
Offset Voltage (Between pins 6 and 7)	100 mV
Sensitivity K_D	.5V/rad
Voltage Controlled Oscillator	
Stability	
Temperature	200 ppm/°C
Supply Voltage	200 ppm/%
Square Wave Output Pin 4	5.4 V_{pp}
Triangle Wave Output Pin 9	2.4 V_{pp}
Maximum Operating Frequency	500 kHz
Sensitivity K_o	4.5 f_o rad/sec/V (f_o: osc. freq. in Hz)
Closed Loop Performance	
Loop Gain K_oK_D	2.8 f_o/sec
Demod. Output, ±10% Deviation	300 mV
(A .001 μF capacitor is needed between pins 7 and 8 to stop parasitic oscillations).	

To best illustrate how the LM565 is used, several applications are covered in detail, and should provide insight into the selection of external components for use with the LM565.

IRIG CHANNEL DEMODULATOR

In the field of missile telemetry, it is necessary to send many channels of relatively narrow band data via a radio link. It has been found convenient to frequency modulate this information on a set of subcarriers with center frequencies in the range of 400 Hz to 200 kHz. Standardization of these frequencies was undertaken by the Inter-Range Instrumentation Group (IRIG) and has resulted in several sets of subcarrier channels, some based on deviations that are a fixed percentage of center frequency and other sets that have a constant deviation regardless of center frequency. IRIG channel 13 has been selected as an example of demonstrate the usefulness of the LM565 as an FM demodulator.

IRIG Channel	13
Center Frequency	14.5 kHz
Max Deviation	±7.5%
Frequency Response	220 Hz
Deviation Ratio	5

Since with a deviation of ±10%, the LM565 will produce approximately 300 mV peak to peak output, with a deviation of 7.5%, we can expect an output of 225 mV. It is desirable to amplify and level shift this signal to ground so that plus and minus output voltages can be obtained for frequency shifts above and below center frequency.

An LM107 can be used to provide the necessary additional gain and the level shift. In Figure 17, R_4 is used to set the output at zero volts with no input signal. The frequency of the VCO can be adjusted with R_3 to provide zero output voltage when an input signal is present.

The design of the filter network proceeds as follows:

It is necessary to choose ω_n such that the peak phase error in the loop is less than 90° for all conditions of modulation. Allowing for noise modulation at low levels of signal to noise, a desirable peak phase error might be 1 radian or 57 degrees, leaving a 33 degree margin for noise. Assuming sinusoidal modulation, Figure 6 can be used to estimate the peak normalized phase error. It will be necessary to make several sample calculations, since the normalized phase error is a function of ω_n.

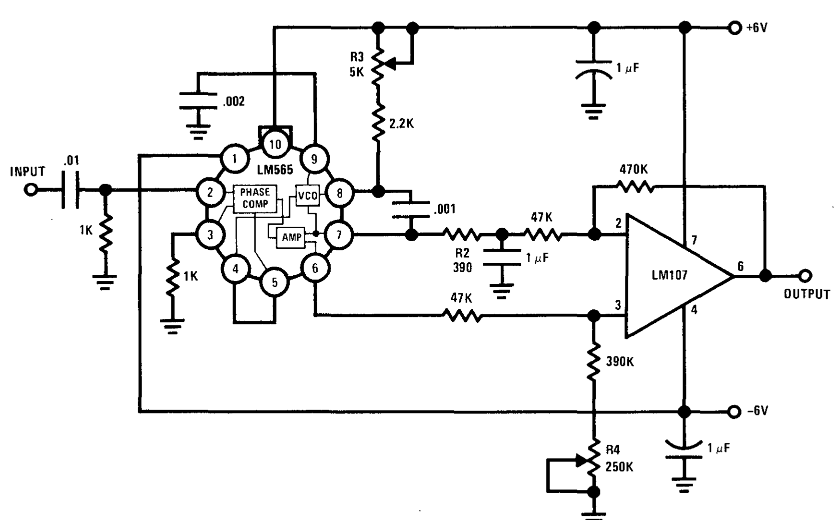

FIGURE 17. IRIG Channel 13 Demodulator

Selecting a worst case of $\omega_n/\omega_m = 1$, $\omega_n = 2\pi X$ 220 Hz; selecting a damping factor of .707,

$$\frac{\theta}{\Delta\omega/\omega_n} = .702$$

or

$$\theta_e = .702 \frac{\Delta\omega}{\omega_n} = .702 \frac{2\pi X 1088 \text{ Hz}}{2\pi X 220 \text{ Hz}}$$

$$= 3.45 \text{ radians}$$

this is unacceptable, since it would throw the loop out of lock, so it is necessary to try a higher value of ω_n. Let $\omega_n = 2\pi x$ 500 Hz, then $\omega_m/\omega_n = .44$, and

$$\theta_e = .44 \frac{\Delta\omega}{\omega_n} = .44 X \frac{2\pi X 1088}{2\pi X 500} = .95 \text{ radians}$$

this should be a good choice, since it is close to radian. Operating at 14.5 kHz, the LM565 has a loop gain K_oK_D of

$$2.28 \times 14.5 \times 10^3 = 33 \times 10^3 \text{ sec}$$

the value of the loop filter capacitor, C_1, can be found from Figure 4:

$$\tau_1 + \tau_2 = 3.5 \times 10^{-3} \text{ sec}$$

from Figure 5, the value of τ_2 can be found (for a damping factor of .707)

$$\tau_2 = 4.4 X 10^{-4} \text{ sec}$$

$$\tau_1 = (35 - 4.4) X 10^{-4} \text{ sec} = 31.4 X 10^{-4} \text{ sec}$$

$$C_1 = \frac{\tau_1}{R} = 31.4 X 10^{-4} \text{ sec} = 1 \mu F$$

$$R_2 = \frac{4.4 X 10^{-4} \text{ sec}}{1 X 10^{-6} \mu F} = 440\,\Omega$$

Looking at Figure 10, the noise bandwidth B_L can be estimated to be

$$B_L = .6\,\omega_n = .6 X 3150 \text{ rad/sec}$$

$$= 1890 \text{ Hz}$$

the complete circuit is shown in Figure 17. Measured performance of the circuit is summarized below with a fully modulated signal as described above and an input level of 40 mVrms:

f 3 dB	200
ζ	0.8
Output Level	770 mVrms
Distortion	0.4%
Signal to Noise at verge of loss of lock (bandwidth of noise = 100 kHz)	–8.4 dB

It will be noted that the loop is capable of demodulating signals lower in level than the noise; this is not in disagreement with earlier statements that loss of lock occurs at signal to noise ratios of approximately +6 dB because of the bandwidths involved. The above number of –8.4 dB signal to noise for threshold was obtained with a noise spectrum 100 kHz wide. The noise power in the loop will be reduced by the ratio of loop noise bandwidth to input noise bandwidth

$$\frac{B_{LOOP}}{B_{INPUT}} = \frac{1890 \text{ Hz}}{100 \text{ kHz}} = .02 \text{ or } -17 \text{ dB}$$

the equivalent signal to noise in the loop is –8.4 dB +17 dB = +8.6 dB which is close to the above-mentioned limit of +6 dB. It should also be noted that loss of lock was noted with full modulation of the signal which will degrade threshold somewhat (although the measurement is more realistic).

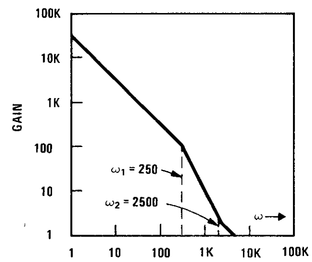

FIGURE 18. Bode Plot for Circuit of Figure 17

FSK DEMODULATOR

Frequency shift keying (FSK) is widely used for the transmission of Teletype information, both in the computer peripheral and communications field. Standards have evolved over the years, and the commonly used frequencies are as follows:

a)	mark	2225	Hz
	space	2975	Hz
b)	mark	1070	Hz
	space	1270	Hz
c)	mark	2025	Hz
	space	2225	Hz

a) is commonly used as subcarrier tones for radio Teletype, while b) and c) are used as carriers for data transmission over telephone and land lines.

As a design example, a demodulator for the 2025 Hz and 2225 Hz mark the space frequencies will be discussed.

Since this is an FM system employing square wave modulation, the natural frequency of the loop must be chosen again so that peak phase errors do not exceed 90° under all conditions. Figure 7 shows peak phase error for a step in frequency; if a damping factor of .707 is selected, the peak phase error is

$$\frac{\theta_e}{\Delta\omega/\omega_n} = .45$$

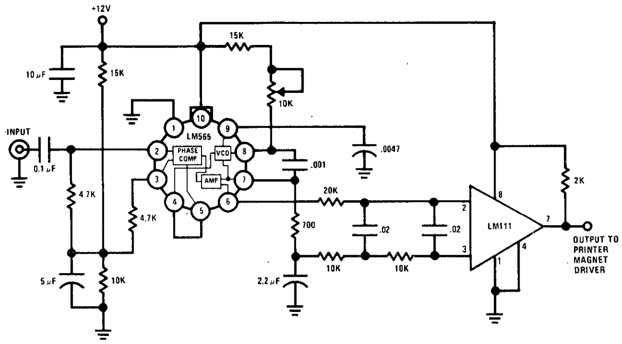

FIGURE 19. FSK Demodulator (2025-2225 cps)

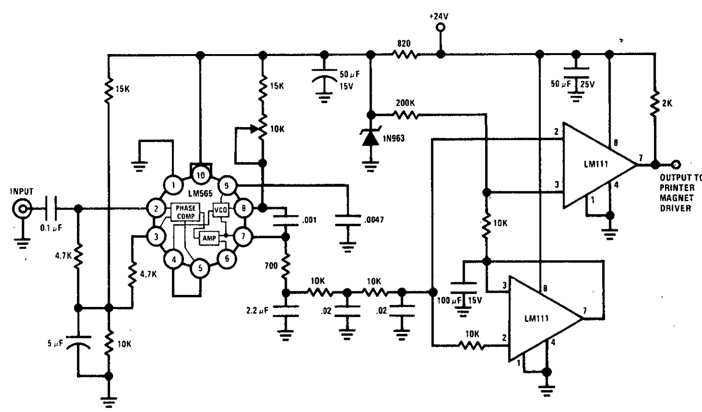

FIGURE 20. FSK Demodulator with DC Restoration

or

$$\theta_e = .45\,\frac{\Delta\omega}{\omega_n}$$

$$\omega_n = .45\,\frac{\Delta\omega}{\theta_e}$$

in our case, $\Delta\omega = 2\,\pi\text{x}\ 200\text{ Hz} = 1250$, if $\theta_e = 1$ radian,

$$\omega_n = .45\,\frac{1250\text{ rad/sec}}{1\text{ radian}} = 500\text{ rad/sec}$$

$$f_n = 80\text{ Hz}$$

The final circuit is shown in Figure 19. The values of the loop filter components ($C_1 = 2.2\ \mu F$ and $R_1 = 700\Omega$) were changed to accommodate a keying rate of 300 bauds (150 Hz), since the values calculated above caused too much roll off of a square wave modulation signal of 150 Hz. The two 10k resistors and .02 μF capacitors at the input to the LM111 comparator provide further filtering of the carrier, and hence smoother operation of the circuit.

A problem encountered with this simple demodulator is that of dc drift. The frequency must be adjusted to provide zero volts to the input of the comparator so that with modulation, switching occurs. Since the deviation of the signal is small (approximately 10%), the peak to peak demodulated output is only 150 mV. It should be apparent that any drift in frequency of the VCO will cause a dc change and hence may lock the comparator in one state or the other. A circuit to overcome this problem is shown in Figure 20. While using the same basic demodulator configuration, an

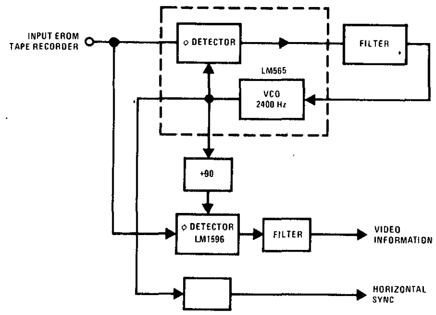

FIGURE 21. Block Diagram of Weather Satellite Demodulator

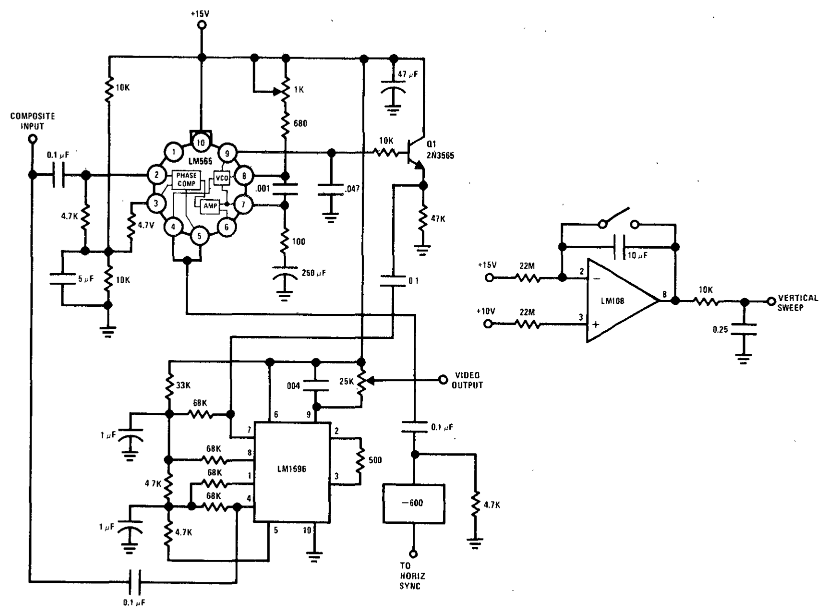

FIGURE 22. Weather Satellite Picture Demodulator

LM111 is used as an accurate peak detector to provide a dc bias for one input to the comparator. When a "space" frequency is transmitted, and the output at pin 8 of the LM565 goes negative and switching occurs, the detected and filtered voltage of pin 3 to the comparator will not follow the change. This is a form of "dc restorer" circuit: it will track changes in drift, making the comparator self compensating for changes in frequency, etc.

WEATHER SATELLITE PICTURE DEMODULATOR

As a last example of how a phase locked loop can be used in communications systems, a weather satellite picture demodulator is shown. Weather satellites of the Nimbus, ESSA, and ITOS series continually photograph the earth from orbits of 100 to 800 miles. The pictures are stored immediately after exposure in an electrostatic storage vidicon, and read out during a succeeding 200 second period. The video information is AM modulated on a 2.4 kHz subcarrier which is frequency modulated on a 137.5 MHz RF carrier. Upon reception, the output from the receiver FM detector will be the 2.4 kHz tone containing AM video information. It is common practice to record the tone on an audio quality tape recorder for subsequent demodulation and display. The 2.4 kHz subcarrier frequency may be divided by 600 to obtain the horizontal sync frequency of 4 Hz.

Due to flutter in the tape recorder, noise during reception, etc., it is desirable to reproduce the 2.4 kHz subcarrier with a phase locked loop, which will track any flutter and instability in the recorder, and effectively filter out noise, in addition to providing a signal large enough for the digital frequency divider. In addition, an in phase component of the VCO signal may be used to drive a synchronous demodulator to detect the video information. A block diagram of the system is shown in Figure 21, and a complete schematic in Figure 22.

The design of the loop parameters was based on the following objectives

$$f_n = 10 \text{ Hz}, \omega_n = 75 \text{ rad/sec}$$

$$B_L = 40 \text{ Hz (from Figure 10)}$$

the complete loop filter, calculated from Figures 4 and 5, is shown in Figure 22. When the loop is in lock and the free running frequency of the VCO is 2.4 kHz, the VCO square wave at pin 4 of the 565 will be in quadrature (90°) from the input signal; however, the zero crossings of the triangle wave across the timing capacitor will be in phase, and if their signal is applied to a double balanced demodulator, such as an LM1596, switching will occur in the demodulator in phase with the 2.4 kHz subcarrier. The double balanced demodulator will produce an output proportional to the amplitude of the subcarrier applied to its signal input. An emitter follower, Q_1, is used to buffer the triangle wave across the timing capacitor so excessive loading does not occur.

The demodulated video signal from the LM1596 is taken across a 25k potentiometer and filtered to a bandwidth of 1.4 kHz, the bandwidth of the transmitted video. Depending on the type of display to be used (oscilloscope, slow scan TV monitor, of facsimile reproducer), it may be necessary to further buffer or amplify the signal obtained. If desired, another load resistor may be used between pin 6 and VCO to obtain a differential output; an operational amp could then be used to provide more gain, level shift, etc.

A vertical sweep circuit is shown using an LM308 low input current op amp as a Miller rundown circuit. The values are chosen to produce an output voltage ramp of –4.5V/220 sec, although this may be adjusted by means of the 22 meg. charging resistor. If an oscilloscope is used as a readout, the horizontal sync can be supplied to the trigger input with the sweep set to provide a total sweep time of something less than 250 ms. A camera is used to photograph the 200 second picture.

SUMMARY AND CONCLUSIONS

A brief review of phase lock techniques has been presented and several useful design tools have been presented that may be useful in predicting the performance of phase locked loops.

A phase locked loop integrated circuit has been described and several applications have been given to illustrate the use of the circuit and the design techniques presented.

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1. Floyd M. Gardner, "Phaselock Techniques", *John Wiley and Sons,* 1966.
2. Elliot L. Greenberg, "Handbook of Telemetry and Remote Control", *McGraw-Hill,* 1967.
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August 1971

APPLICATIONS FOR A NEW ULTRA-HIGH SPEED BUFFER

INTRODUCTION

Voltage followers have gained in popularity in applications such as sample and hold circuits, general purpose buffers, and active filters since the introduction of IC operational amplifiers. Since they were not specifically designed as followers, these early IC's had limited usage due to low bandwidth, low slew rate and high input current. Usage of voltage followers was expanded in 1967 with the introduction of the LM102, the first IC designed specifically as a voltage follower. With the LM102, engineers were able to obtain an order of magnitude improvement in performance and extend usage into medium speed applications. The LM110, an improved LM102, was introduced in late 1969. However, even higher speeds and lower input currents were needed for very fast sample and holds, A to D and D to A converters, coax cable drivers, and other video applications.

The solution to this application problem was attained by combining technologies into a single package. The result, the LH0033 high speed buffer, utilizes JFET and bipolar technology to produce a ultra-fast voltage follower and buffer whose propagation delay closely approaches speed-of-light delay across its package, while not compromising input impedance or drive characteristics. Table I compares various voltage followers and illustrates the superiority of the LH0033 in both low input current or high speed video applications.

CIRCUIT CONSIDERATIONS

The junction FET makes a nearly ideal input device for a voltage follower, reducing input bias current to the picoamp range. However, FET's exhibit moderate voltage offsets and offset drifts which tend to be difficult to compensate. The simple voltage follower of Figure 1 eliminates initial offset and offset drift if Q_1 and Q_2 are identically matched transistors. Since the gate to source voltage of Q_2 equals zero volts, then Q_1's gate to source voltage equals zero volts. Furthermore as V_{P1} changes with temperature (approximately 2.2 mV/°C), V_{P2} will change by a corresponding amount. However, as load current is drawn from the output, Q_1 and Q_2 will drift at different rates. A circuit which overcomes offset voltage drift is used in a new high speed buffer amplifier, the LH0033. Initial offset is typically 5 mV and offset drift is 20 μV/°C. Resistor R_2 is used to establish the drain current of current source transistor, Q_2 at 10 mA.

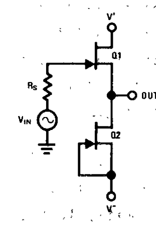

FIGURE 1. Simple Voltage Follower Schematic

The same drain current flows through Q_1 causing a voltage at the source of approximately 1.1V. The 10 mA flowing through R_1 plus Q_3's V_{BE} of 0.6V causes the output to sit at zero volts for zero volts in. Q_3 and Q_4 eliminate loading the input stage (except for base current) and CR_1 and CR_2 establish the output stage collector current.

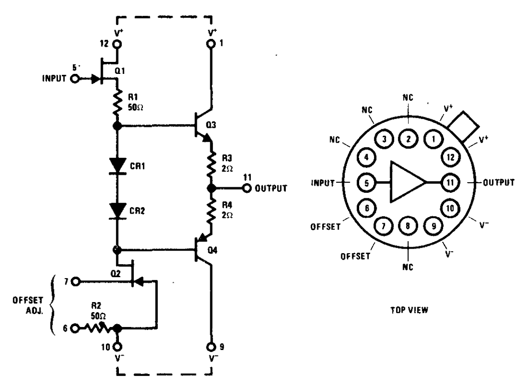

FIGURE 2. LH0033 Schematic

If Q_1 and Q_2 are matched, the resulting drift is reduced to a few μV/°C.

TABLE I COMPARISON OF VOLTAGE FOLLOWERS

PARAMETER	CONVENTIONAL MONOLITHIC OP AMP LM741	FIRST GENERATION VOLTAGE FOLLOWER LM102	SECOND GENERATION VOLTAGE FOLLOWER LM110	SPECIALLY DESIGNED VOLTAGE FOLLOWER LH0033
INPUT BIAS CURRENT	200 nA	3.0 nA	1.0 nA	0.05 nA
SLEW RATE	0.5V/µs	10V/µs	30V/µs	1500V/µs
BANDWIDTH	1.0 MHz	10 MHz	20 MHz	100 MHz
PROP. DELAY TIME	350 ns	35 ns	18 ns	1.2 ns
OUTPUT CURRENT CAPABILITY	±5 mA	±2 mA	±2 mA	±100 mA

PERFORMANCE OF THE LH0033 FAST VOLTAGE FOLLOWER/BUFFER

The major electrical characteristics of the LH0033 are summarized in Table II. All the virtues of a ultra-high speed buffer have been incorporated. Figure 3 is a plot of input bias current vs temperature and shows the typical FET input characteristics. Other typical performance curves are illustrated in Figures 4 through 10. Of particular interest is Figure 8, which demonstrates the performance of the LH0033 in video applications to over 100 MHz.

TABLE II

PARAMETER	CONDITIONS	VALUE	PARAMETER	CONDITIONS	VALUE
Output Offset Voltage	R_S = 100 kΩ	5 mV	Output Current Capability		±100 mA peak
Input Bias Current		50 pA	Slew Rate	R_S = 50Ω, R_L = 1k	1500V/µs
Input Impedance	V_{IN} = 1.0 Vrms R_L = 1k, f = 1 kHz	10^{11} Ω	Propagation Delay		1.2 ns
Voltage Gain	V_{IN} = 1.0 Vrms R_L = 1k, f = 1 kHz, R_S = 100k	0.98	Bandwidth	V_{IN} = 1.0 Vrms R_S = 50Ω, R_L = 1k	100 MHz
Output Voltage Swing	V_S = ±15V, R_S = 100k R_L = 1k	±13V			

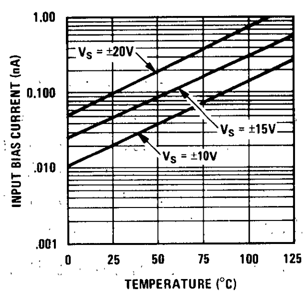

FIGURE 3. Input Bias Current vs Temperature

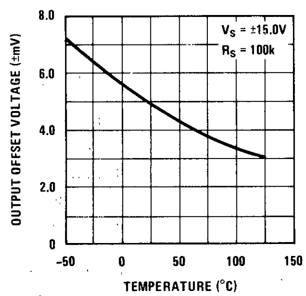

FIGURE 4. Output Offset Voltage vs Temperature

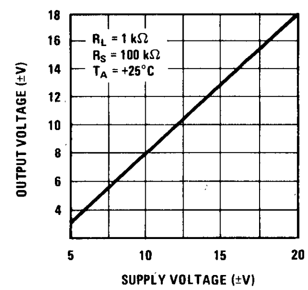

FIGURE 5. Output Voltage vs Supply Voltage

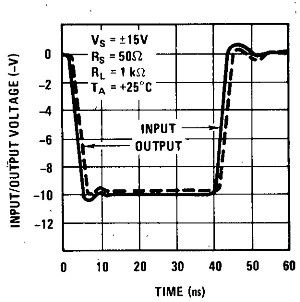

FIGURE 6. Negative Pulse Response

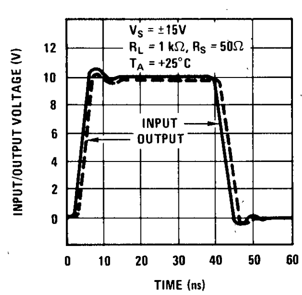

FIGURE 7. Positive Pulse Response

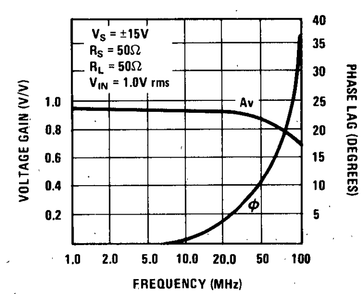

FIGURE 8. Frequency Response

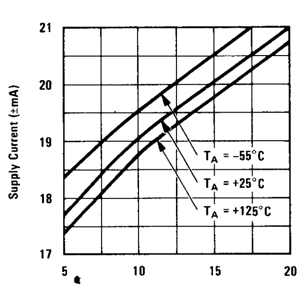

FIGURE 9. Supply Current vs Supply Voltage

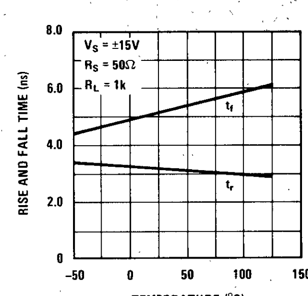

FIGURE 10. Rise and Fall Time vs Temperature

APPLICATIONS FOR ULTRA-FAST FOLLOWERS

The LH0033's high input impedance ($10^{11}\ \Omega$, shunted by 2 pF) and high slew rate assure minimal loading and high fidelity in following high speed pulses and signals. As shown below, the LH0033 is used as a buffer between MOS logic and a high speed dual limit comparator. The device's high input impedance prevents loading of the MOS logic signal (even a conventional scope probe will distort high output impedance MOS). The LH0033 adds about a 1.5 ns to the total delay of the comparator. Adjustment of voltage divider R_1, R_2 allows interface to TTL, DTL and other high speed logic forms.

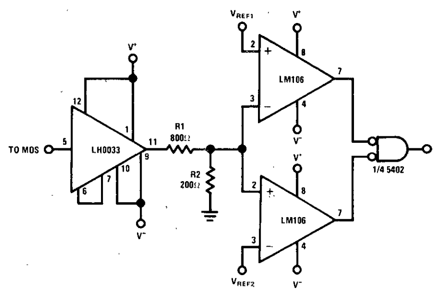

FIGURE 11. High Speed Dual Limit Comparator for MOS Logic

The LH0033 was designed to drive long cables, shielded cables, coaxial cables and other generally stringent line driving requirements. It will typically drive 200 pF with no degradation in slew rate and several thousand pF at a reduced rate. In order to prevent oscillations with large capacitive loads, provision has been made to insert damping resistors between V^+ and pin 1, and V^- and pin 9. Values between 47 and 100Ω work well for $C_L > 1000$ pF. For non-reactive loads, pin 12 should be shorted to pin 1 and pin 10 shorted to pin 9. A coaxial driver is shown in Figure 13. Pin 6 is shorted to pin 7, obtaining an initial offset of 5.0 mV, and the 43Ω coupled with the LH0033's output impedance (about 6Ω) match the coaxial cable's characteristic impedance. C_1 is adjusted as a function of cable length to optimize rise and fall time. Rise time for the circuit as shown in Figure 12, is 10 ns.

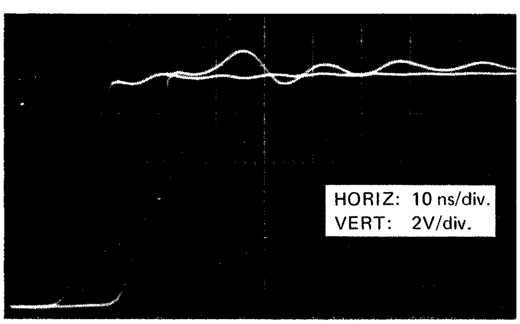

FIGURE 12. LH0033 Pulse Response into 10 Foot Open Ended Coaxial Cable

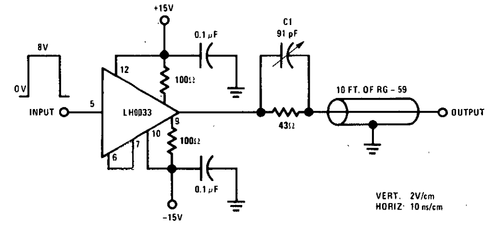

FIGURE 13.

Another application that utilizes the low input current, high speed and high capacitance drive capabilities of the LH0033 is a shield or line driver for high speed automatic test equipment. In this example, the LH0033 is mounted close to the device under test and drives the cable shield thus allowing higher speed operation since the device under test does not have to charge the cable.

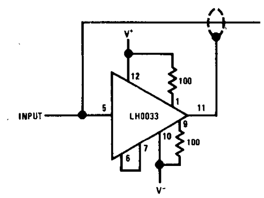

FIGURE 14. Instrumentation Shield/Line Driver

The LH0033's high input impedance and low input bias current may be utilized in medium speed circuits such as Sample and Hold, and D to A converters. Figure 15 shows an LH0033 used as a buffer in medium speed D to A converter.

Offset null is accomplished by connecting a 100Ω pot between pin 7 and V^-. It is generally a good idea to insert 20Ω in series with the pot to prevent excessive power dissipation in the LH0033 when the pot is shorted out. In non-critical or AC coupled applications, pin 6 should be shorted to pin 7. The resulting output offset is typically 5 mV at 25°C.

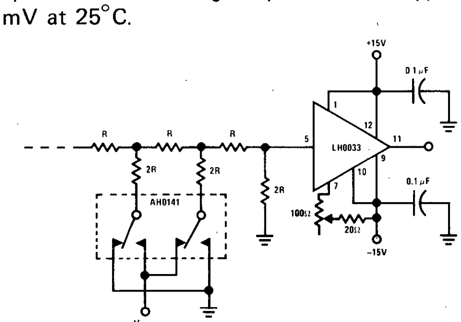

FIGURE 15.

The high output current capability and slew rate of the LH0033 are utilized in the sample and hold circuit of Figure 16. Amplifier, A1 is used to buffer high speed analog signals. With the configuration shown, acquisition time is limited by the time constant of the switch "ON" resistance and sampling capacitor, and is typically 200 or 300 ns. A_2's low input bias current, results in drifts in hold mode of $\frac{50\text{ mV}}{\text{sec}}$ at 25°C and $\frac{1\text{V}}{\text{sec}}$ at 125°C.

The LH0033 may be utilized in AC applications such as video amplifiers and active filters. The circuit of Figure 17 utilizes boot strapping to achieve input impedances in excess of 10 MΩ.

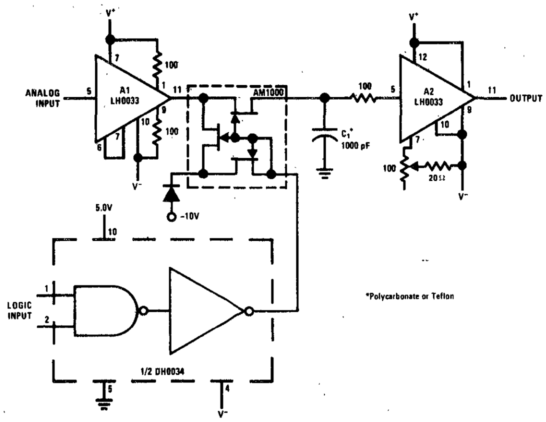

FIGURE 16. High Speed Sample & Hold

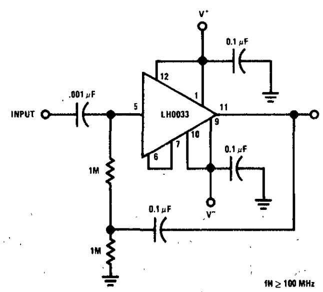

FIGURE 17. High Input Impedance AC Coupled Amplifier

A single supply, AC coupled amplifier is shown in Figure 18. Input impedance is approximately 500k and output swing is in excess of 8V peak-to-peak with a 12V supply.

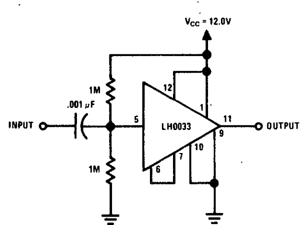

FIGURE 18. Single Supply AC Amplifier

The LH0033 may be readily used in applications where symmetrical supplies are unavailable or may not be desirable. A typical application might be an interface to an MOS shift register where $V^+ = 5.0V$ and $V^- = -25V$. In this case, an apparent output offset occurs. In reality, the output voltage is due to the LH0033's voltage gain of less than unity. The output voltage shift due to asymmetrical supplies may be predicted by:

$$\Delta V_O \cong (1 - Av)\frac{(V^+ - V^-)}{2} = .005\,(V^+ - V^-)$$

where: Av = No load voltage gain, typically 0.99.

V^+ = Positive Supply Voltage.

V^- = Negative Supply Voltage.

For the foregoing application, ΔV_O would be −100 mV. This apparent "offset" may be adjusted to zero as outlined above.

Figure 19 shows a high Q, notch filter which takes advantage of the LH0033's wide bandwidth. For the values shown, the center frequency is 4.5 MHz.

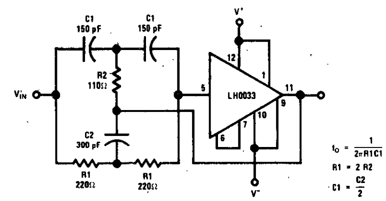

FIGURE 19. 4.5 MHz Notch Filter

The LH0033 can also be used in conjunction with an operational amplifier as current booster as shown in Figure 20. Output currents in excess of 100 mA may be obtained. Inclusion of 150Ω resistors between pins 1 and 12, and 9 and 10 provide short circuit protection, while decoupling pins 1 and 9 with 1000 pF capacitors allow near full output swing.

The value for the short circuit current is given by:

$$I_{SC} \cong \frac{V^+}{R_{LIMIT}} = \frac{V^-}{R_{LIMIT}}$$

where: $I_{SC} \leq 100$ mA.

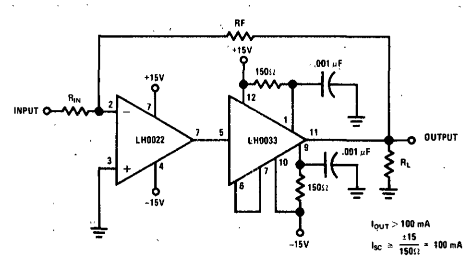

FIGURE 20. Using LH0033 as an Output Buffer

SUMMARY

The advantages of a FET input buffer have been demonstrated. The LH0033 combines very high input impedance, wide bandwidth, very high slew rate, high output capability, and design flexibility, making it an ideal buffer for applications ranging from DC to in excess of 100 MHz.

August 1971

PIN DIODE DRIVERS

INTRODUCTION

The DH0035/DH0035C is a TTL/DTL compatible, DC coupled, high speed PIN diode driver. It is capable of delivering peak currents in excess of one ampere at speeds up to 10 MHz. This article demonstrates how the DH0035 may be applied to driving PIN diodes and comparable loads which require high peak currents at high repetition rates. The salient characteristics of the device are summarized in Table I.

PARAMETER	CONDITIONS	VALUE
Differential Supply Voltage ($V^+ - V^-$)		30V Max.
Output Current		1000 mA
Maximum Power		1.5W
t_{delay}	PRF = 5.0 MHz	10 ns
t_{rise}	$V^+ - V^- = 20V$ 10% to 90%	15 ns
t_{fall}	$V^+ - V^- = 20V$ 90% to 10%	10 ns

Table I DH0035 Characteristics

PIN DIODE SWITCHING REQUIREMENTS

Figure 1 shows a simplified schematic of a PIN diode switch. Typically, the PIN diode is used in RF through microwave frequency modulators and switches. Since the diode is in shunt with the RF path, the RF signal is attenuated when the diode is forward biased ("ON"), and is passed unattenuated when the diode is reversed biased ("OFF").

There are essentially two considerations of interest in the "ON" condition. First, the amount of "ON" control current must be sufficient such that RF signal current will not significantly modulate the "ON" impedance of the diode. Secondly, the time required to achieve the "ON" condition must be minimized.

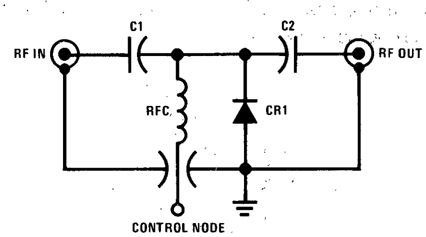

FIGURE 1. Simplified PIN Diode Switch

The charge control model of a diode[1,2] leads to the charge continuity equation given in equation (1).

$$i = \frac{dQ}{dt} + \frac{Q}{\tau} \qquad (1)$$

where: Q = charge due excess minority carriers
τ = mean life time of the minority carriers

Equation (1) implies a circuit model shown in Figure 2. Under steady conditions $\frac{dQ}{dt} = 0$, hence:

$$I_{DC} = \frac{Q}{\tau} \text{ or } Q = I_{DC}\,\tau \qquad (2)$$

where: I = steady state "ON" current.

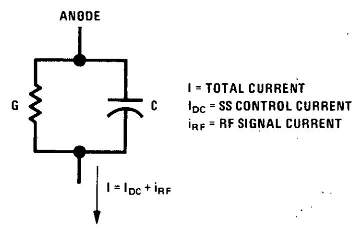

FIGURE 2. Circuit Model for PIN Switch

The conductance is proportional to the current, I; hence, in order to minimize modulation due to the RF signal, $I_{DC} >> i_{RF}$. Typical values for I_{DC} range from 50 mA to 200 mA depending on PIN diode type, and the amount of modulation that can be tolerated.

The time response of the excess charge, Q, may be evaluated by taking the Laplace transform of equation (1) and solving for Q:

$$Q(s) = \frac{\tau I(s)}{1 + s\tau} \qquad (3)$$

Solving equation (3) for Q(t) yields:

$$Q(t) = L^{-1}[Q(s)] = I\tau(1 - \epsilon^{-t/\tau}) \qquad (4)$$

The time response of Q is shown in Figure 3a. As can be seen, several carrier lifetimes are required to achieve the steady state "ON" condition ($Q = I_{DC} \cdot \tau$).

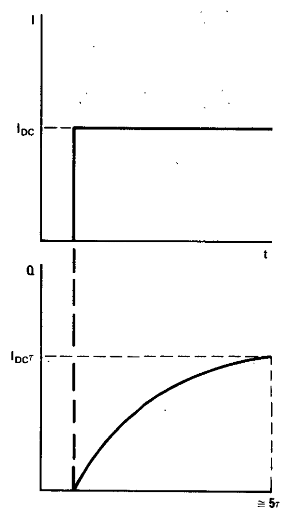

FIGURE 3a.

The time response of the charge, hence the time for the diode to achieve the "ON" state could be shortened by applying a current spike, Ipk, to the diode and then dropping the current to the steady state value, I_{DC}, as shown in Figure 3b. The optimum response would be dictated by:

$$(Ipk)(t) = \tau \cdot I_{DC} \qquad (5)$$

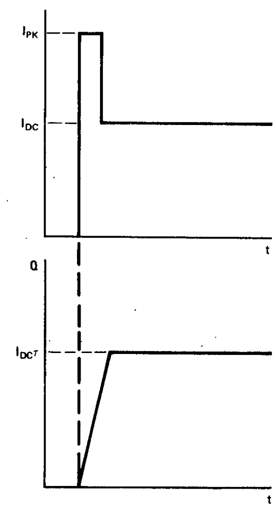

FIGURE 3b.

The turn off requirements for the PIN diode are quite similar to the turn on, except that in the "OFF" condition, the steady current drops to the diode's reverse leakage current.

A charge, $I_{DC} \cdot \tau$, was stored in the diode in the "ON" condition and in order to achieve the "OFF" state this charge must be removed. Again, in order to remove the charge rapidly, a large peak current (in the opposite direction) must be applied to the PIN diode:

$$-Ipk >> \frac{Q}{\tau} \qquad (6)$$

It is interesting to note an implication of equation (5). If the peak turn on current were maintained for a period of time, say equal to τ, then the diode would acquire an excess charge equal to Ipk·T. This same charge must be removed at turn off, instead of a charge $I_{DC} \cdot \tau$, resulting in a considerably slower turn off. Accordingly, control of the width of turn on current peak is critical in achieving rapid turn off.

APPLICATION OF THE DH0035 AS A PIN DIODE DRIVER

The DH0035 is specifically designed to provide both the current levels and timing intervals required to optimally drive PIN diode switches. Its

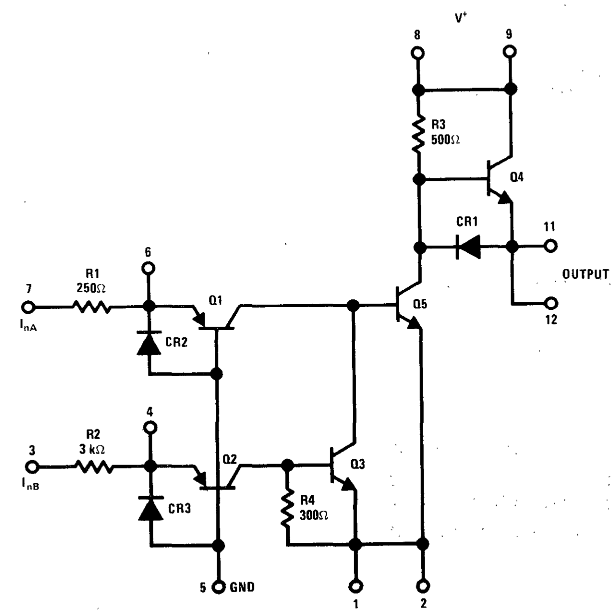

FIGURE 4. DH0035 Schematic Diagram

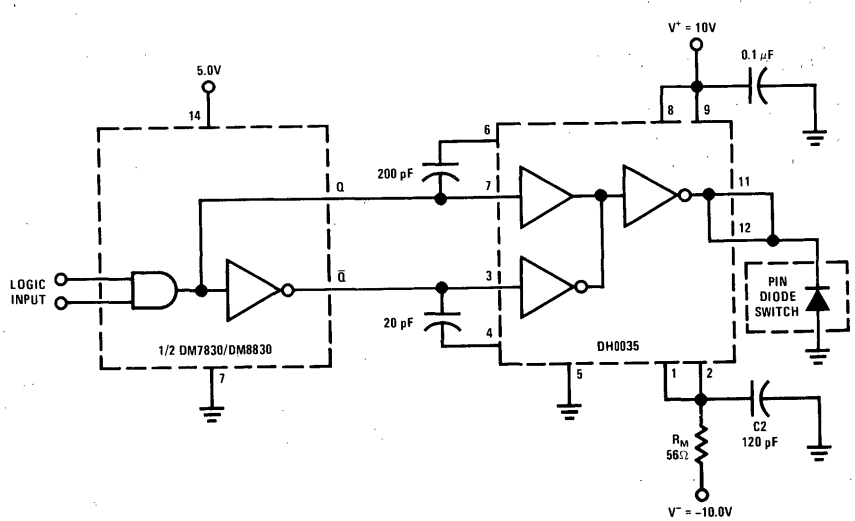

FIGURE 5. Cathode Grounded Design

schematic is shown in Figure 4. The device utilizes a complementary TTL input buffer such as the DM7830/DM8830 or DM5440/DM7440 for its input signals.

Two configurations of PIN diode switch are possible: cathode grounded and anode grounded. The design procedures for the two configurations will be considered separately.

ANODE GROUND DESIGN

Selection of power supply voltages is the first consideration. Table I reveals that the DH0035 can withstand a total of 30V differentially. The supply voltage may be divided symmetrically at ±15V, for example. Or asymmetrically at +20V and −10V. The PIN diode driver shown in Figure 5, uses ±10V supplies.

When the Q output of the DM8830 goes high a transient current of approximately 50 mA is applied to the emitter of Q_1 and in turn to the base of Q_5.

Q_5 has an h_{fe} = 20, and the collector current is h_{fe} x 50 or 1000 mA. This peak current, for the most part, is delivered to the PIN diode turning it "ON" (RF is "OFF").

Ipk flows until C_2 is nearly charged. This time is given by:

$$t = \frac{C2\,\Delta V}{Ipk} \quad (7)$$

where: ΔV = the change in voltage across C_2.

Prior to Q_5's turn on, C_2 was charged to the minus supply voltage of −10V. C_2's voltage will rise to within two diode drops plus a V_{sat} of ground:

$$V = |V^-| - Vf(\text{PIN Diode}) - Vf_{CR1} - V_{sat_{Q5}} \quad (8)$$

for V^- = −10V, ΔV = 8V.

Once C_2 is charged, the current will drop to the steady state value, I_{DC}, which is given by:

$$I_{DC} = \frac{V}{R_M} - \frac{V^+}{R_3} - \frac{V_{CC}}{R_1} \quad (9)$$

where: V_{CC} = 5.0V
R_1 = 250Ω
R_3 = 500Ω

$$\therefore R_M = \frac{(R_3)\,(\Delta V)\,(R_1)}{R_1 V^+ + I_{DC} R_3 R_1 + V_{CC} R_3} \quad (9a)$$

For the driver of Figure 5, and I_{DC} = 100 mA, R_M is 56 ohms (nearest standard value).

Returning to equation (7) and combining it with equation (5) we obtain:

$$t = \frac{\tau I_{DC}}{Ipk} = \frac{C_2 V}{Ipk} \quad (10)$$

Solving equation (10) for C_2 gives:

$$C_2 = \frac{I_{DC}\tau}{V} \quad (11)$$

For τ = 10 ns, C_2 = 120 pF.

One last consideration should be made with the diode in the "ON" state. The power dissipated by the DH0035 is limited to 1.5W (see Table I). The DH0035 dissipates the maximum power with Q_5 "ON". With Q_5 "OFF", neglible power is dissipated by the device. Power dissipation is given by:

$$P\,diss \cong \left[I_{DC}\,(|V^-| - \Delta V) + \frac{(V^+ - V^-)^2}{R3} \right] \times (D.C.) \leq P_{max} \quad (12)$$

where: D.C. = Duty Cycle =

$$\frac{(\text{"ON" time})}{(\text{"ON" time} + \text{"OFF" time})}$$

$$Pmax = 1.5W$$

In terms of I_{DC}:

$$I_{DC} \leq \frac{\left[\frac{(Pmax)}{(D.C.)} - \frac{(V^+ - V^-)^2}{500} \right]}{|V^-| - \Delta V} \quad (12a)$$

For the circuit of Figure 5 and a 50% duty cycle, P diss = 0.5W.

Turn-off of the PIN diode begins when the Q output of the DM8830 returns to logic "0" and the $\overline{Q}$ output goes to logic "1". Q_2 turns "ON", and in turn, causes Q_3 to saturate. Simultaneously, Q_1 is turned "OFF" stopping the base drive to Q_5. Q_3 absorbs the stored base charge of Q_5 facilitating its rapid turn-off. As Q_5's collector begins to rise, Q_4 turns "ON". At this instant, the PIN diode is still in conduction and the emitter of Q_4 is held at approximately −0.7V. The instantaneous current available to clear stored charge out of the PIN diode is:

$$Ipk = \frac{V^+ - V_{BE\,Q4} + V_{f(PIN)}}{\frac{R_3}{h_{fe}+1}} \cong \frac{(h_{fe}+1)\,(V^+)}{R_3} \quad (13)$$

where:

$h_{fe} + 1$ = current gain of Q_4 = 20
$V_{BE\,Q4}$ = base-emitter drop of Q_4 = 0.7V
$V_{f(PIN)}$ = forward drop of the PIN diode = 0.7V

For typical values given, Ipk = 400 mA. Increasing V^+ above 10V will improve turn-off time of the diode, but at the expense of power dissipation in the DH0035. Once turn-off of the diode has been achieved, the DH0035 output current drops to the reverse leakage of the PIN diode. The attendant power dissipation is reduced to about 35 mW.

CATHODE GROUND DESIGN

Figure 6 shows the DH0035 driving a cathode grounded PIN diode switch. The peak turn-on current is given by:

$$Ipk \cong \frac{(V^+ - V^-)\,(h_{fe}+1)}{R_3} \quad (14)$$

= 800 mA for the values shown.

The steady state current, I_{DC}, is set by Rp and is given by:

$$I_{DC} = \frac{V^+ - 2V_{BE}}{\frac{R_3}{h_{fe}+1} + R_P} \quad (15)$$

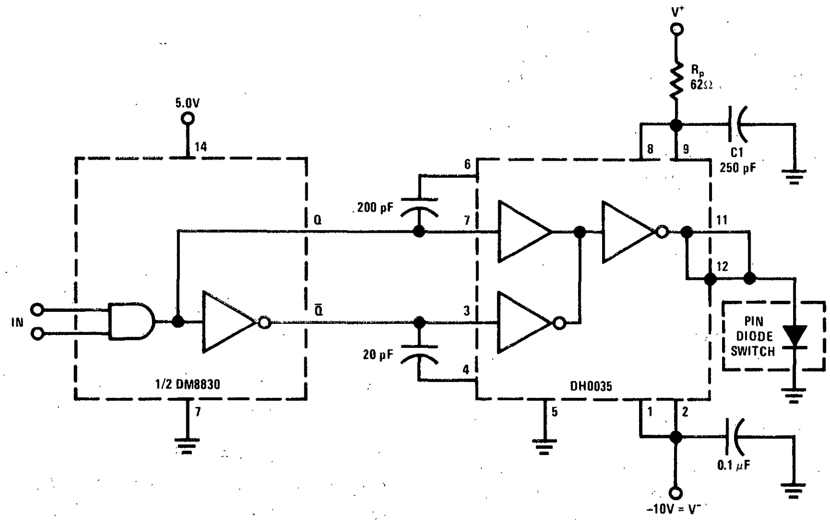

FIGURE 6. Anode Grounded Driver

where: $2V_{BE}$ = forward drop of Q_4 base emitter junction plus V_f of the PIN diode = 1.4V.

In terms of Rp, equation (15) becomes:

$$Rp = \frac{(h_{fe}+1)(V^+ - 2V_{BE}) - I_{DC}R_3}{(h_{fe}+1)\,I_{DC}} \qquad (15a)$$

For the circuit of Figure 6, and I_{DC} = 100 mA, Rp is 62 ohms (nearest standard value).

It now remains to select the value of C_1. To do this, the change in voltage across C_1 must be evaluated. In the "ON" state, the voltage across C_1, Vc, is given by:

$$(Vc)_{ON} = \frac{V^+R_3 + Rp(h_{fe}+1)(2V_{BE})}{R_3 + (h_{fe}+1)\,Rp} \qquad (16)$$

For the values indicated above, $(Vc)_{ON}$ = 3.8V.

In the "OFF" state, Vc is given by:

$$(Vc)_{OFF} = \frac{V^+R_3 - |V^-|Rp}{Rp + R_3} \qquad (17)$$

= 8.0V for the circuit of Figure 6.

Hence, the change in voltage across C_1 is:

$$\begin{aligned} V &= (Vc)_{OFF} - (Vc)_{ON} \qquad (18)\\ &= 8.0 - 3.8\\ &= 4.2V \end{aligned}$$

The value of C_1 is given, as before, by equation (11):

$$C_1 = \frac{I_{DC}\tau}{V^-} \qquad (19)$$

For a diode with τ = 10 ns and I_{DC} = 100 mA, C_1 = 250 pF.

Again, the power dissipated by the DH0035 must be considered. In the "OFF" state, the power dissipation is given by:

$$P_{OFF} = \left[\frac{(V^+ - V^-)^2}{R_3}\right](D.C.) \qquad (20)$$

where: D.C. = duty cycle =

$$\frac{\text{"OFF" time}}{\text{"OFF" time + "ON" time}}$$

The "ON" power dissipation is given by:

$$P_{ON} = \left[\frac{(Vc)_{ON}^{\,2}}{R_3} + I_{DC} \times (Vc)_{ON}\right](1 - D.C.) \qquad (21)$$

where: $(Vc)_{ON}$ is defined by equation (16).

Total power dissipated by the DH0035 is simply $P_{ON} + P_{OFF}$. For a 50% duty cycle and the circuit of Figure 6, P diss = 616 mW.

The peak turn-off current is, as indicated earlier, equal to 50 mA x h_{fe} which is about 1000 mA. Once the excess stored charge is removed, the current through Q_5 drops to the diodes leakage current. Reverse bias across the diode = $V^- - V_{sat} \cong -10V$ for the circuit of Figure 6.

REPETITION RATE CONSIDERATIONS

Although ignored until now, the PRF, in particular, the "OFF" time of the PIN diode is important in selection of C_2, R_M, and C_1, Rp. The capacitors must recharge completely during the diode "OFF" time. In short:

$$4\,R_MC_2 \leq t_{OFF} \qquad (22a)$$

$$4\,RpC_1 \leq t_{OFF} \qquad (22b)$$

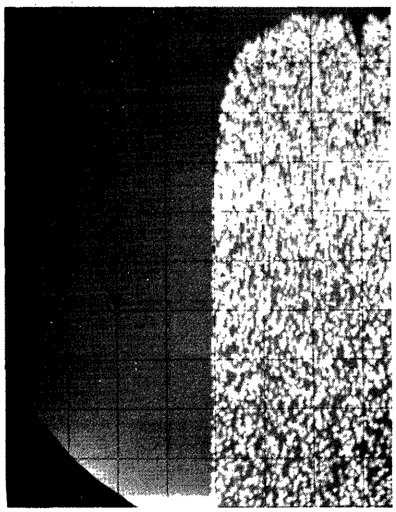

FIGURE 7. RF Turn-On (10 ns/cm)

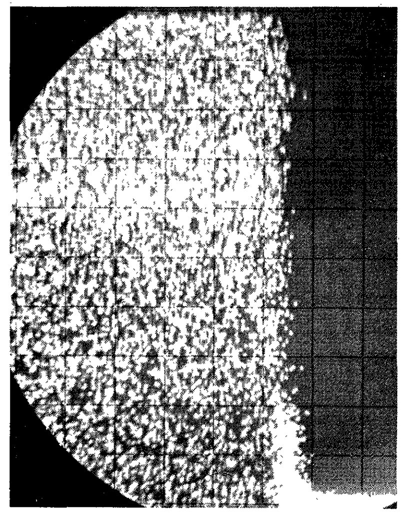

FIGURE 8. RF Turn-Off (10 ns/cm)

CONCLUSION

The circuit of Figure 6 was breadboarded and tested in conjunction with a Hewlett-Packard 33622A PIN diode.

I_{DC} was set at 100 mA, $V^+ = 10.0V$, $V^- = 10V$. Input signal to the DM8830 was a 5V peak, 100 kHz, 5 µs wide pulse train. RF turn-on was accomplished in 10-12 ns while turn-off took approximately 5 ns, as shown in Figures 7 and 8.

In practice, adjustment C_2 (C_1) may be required to accommodate the particular PIN diode minority carrier life time.

SUMMARY

A unique circuit utilized in the driving of PIN diodes has been presented. Further a technique has been demonstrated which enable the designer to tailor the DH0035 driver to the PIN diode application.

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2. "Models of Transistors and Diodes", John G. Linvill, *McGraw-Hill Book* Company, Inc., New York, N.Y.
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September 1971

A UNIQUE MONOLITHIC AGC/SQUELCH AMPLIFIER

INTRODUCTION

As complexity and usage of communication systems increases, there is a growing use of a special class of circuitry, designed to make the system more convenient to the user, as well as allowing it to adapt to changes in the transmission channel. The most common function is voltage-variable gain, used in volume compression and expansion, and a specialized case, squelch, in which gain remains either in its maximum or minimum state.

The main problem in such circuitry is finding a suitable nonlinear element to do the job. Conventional elements, appearing in Table 1, share common problems of distortion, cost, limited signal handling capability, sometimes limited gain reduction range, and usually insert unwanted transients onto the signal during periods of rapid gain changing. Two mechanisms may be defined for these elements; either effective resistance or effective transconductance is varied by the DC control voltage. Because the variation is accomplished by changing quiescent operating points, DC decoupling is required at the output, and only AC signals may be handled. DC decoupling, however, still allows rapid changes in DC operating point to be transmitted as switching transients. While linearity is claimed for FET and the lamp-photocell schemes, such linearity is still only part of a large-signal nonlinear characteristic. With any of the elements, quasi-linearity is obtained by traversing a small segment of the overall element range; hence, variable gain elements must precede any system voltage gain.

TABLE 1. Conventional Gain Control Elements

ELEMENT	MECHANISM	CONTROL RANGE	CONTROL/ OUTPUT ISOLATION	LARGE SIGNAL HANDLING	COMMENTS
P-N Junction	Forward Resistance	Good	Poor	Poor	Simple, predictable
Bipolar Transistor	Saturation Resistance	Fair	Poor	Fair	Beta Dependent
FET	Channel Resistance	Good	Poor	Fair	Unpredictable gate control voltage requirements; for driving fairly high impedance loads
Photocell-Lamp	Photocell Resistance	Good	Good	Good	Requires power to drive lamp; cell must be shielded from ambient light
FET	Transconductance	Fair	Poor	Poor	Unpredictable gate control voltage requirements; for driving fairly high impedance loads
Bipolar Transistor	Transconductance	Fair	Poor	Poor	Commonly used in AM-IF applications
Tetrode Vacuum Tube	Transconductance	Fair	Poor	Good	Filament Power

A MONOLITHIC APPROACH

Because of the inexpensive complexity possible with monolithic construction, techniques may be used which circumvent many of the shortcomings of discrete gain control circuits. The balanced diode attenuator of Figure 1 allows variable series-

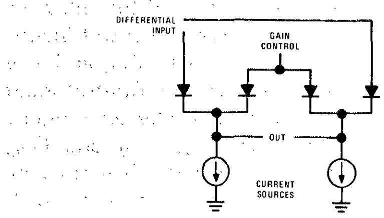

FIGURE 1. Balanced Diode Attenuator

shunt attenuation, and if used in a differential circuit, with monolithic matching, can cancel all spurious control-signal effects at the output. Figure 2 gives a subsystem block diagram, for effectively controlling the balanced arrangement of Figure 1. An input differential amplifier provides differential diode drive even if only single ended inputs are available, and keeps the common-mode DC level to Q_3 and Q_6 at a constant level. Notice that emitter followers have been substituted for simple diodes, giving higher input impedance, and superior gain reduction range. The input diff.-amp. also prevents gain changes from affecting the input impedance. Since the control elements are quasi-linear only for small signal voltages, the input diff.-amp. has unity gain, with all circuit gain being performed after the variable elements.

A feedback circuit senses common-mode output from the emitter followers, and compares it with the DC control voltage, to reliably set attenuation characteristics. For maximum gain, Q_3 and Q_6 behave as ordinary emitter followers. As the control voltage rises, Q_4 and Q_5 begin to conduct, effectively "robbing" Q_3 and Q_6 of available DC emitter current. Consequently, dynamic emitter resistances of Q_3 and Q_6, in series with the signal, increase, while those of Q_4 and Q_5 decrease, shunting across the signal. In the limit, Q_3 and Q_6 are completely cut off, and the shunt pair fully conducting.

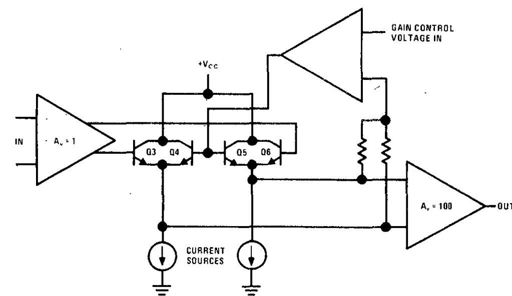

FIGURE 2. System Block Diagram

Emitter follower output is fed into a differential input, single-ended output amplifier, where common-mode changes resulting from the gain control voltage are rejected, and the signal is amplified to usable levels. Thus, the system is a variable gain DC amplifier.

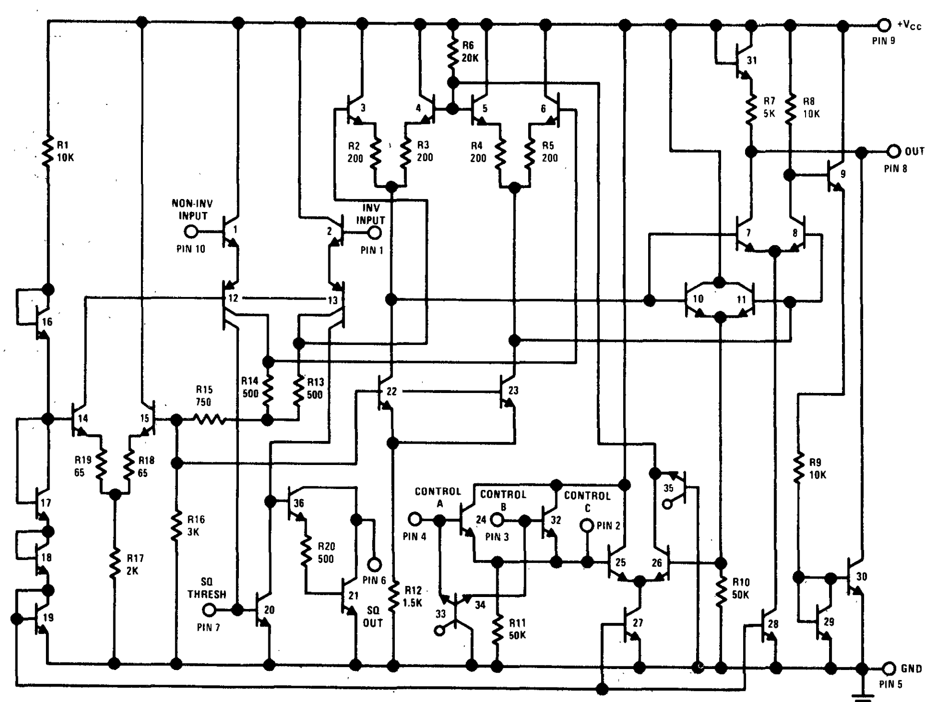

FIGURE 3. LM170 Schematic

MONOLITHIC REALIZATION

A practical version of Figure 2's block diagram, National's LM170 appears as a schematic in Figure 3. Despite its apparent complexity, and its use of 34 junction devices and 20 resistors, the entire circuit has been compressed onto a 39 x 42 mil monolithic chip, Figure 4, smaller than most operational amplifiers.

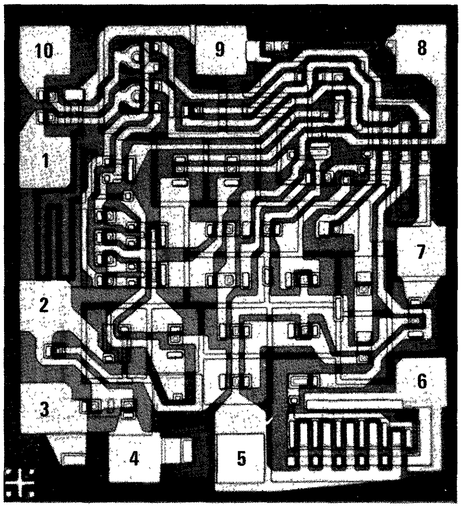

FIGURE 4. LM170 Chip

Examining first the input circuit, Figure 5, one may notice that the configuration is essentially that of the highly successful LM101 operational amplifier. Emitter followers, Q_1 and Q_2, combine with an unusual lateral PNP configuration, Q_{12} and Q_{13}, to allow large common-mode input range (up to and including the positive supply voltage), low input offset voltage, and the ability to withstand large differential input overvoltages without damage. Common-mode feedback to a differential current source, Q_{14} and Q_{15}, along with a stable, diode determined reference, automatically biases the differential input configuration to give constant and predictable DC common-mode output voltage, despite variations in the relatively unpredictable lateral PNP "beta". The input circuit draws constant power supply current regardless of power supply voltage, and consequently exhibits predictable input impedance and bias currents.

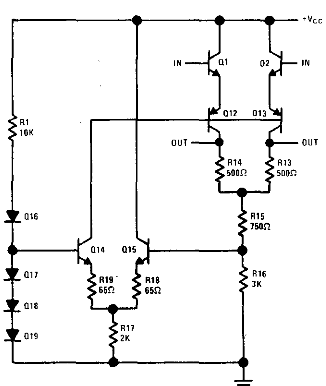

FIGURE 5. LM170 Input Differential Amplifier

The gain control circuit, Figure 6, operates as outlined in Figure 2; Q_{25}, Q_{26} and Q_{27} form the control feedback amplifier; Q_{22} and Q_{23} are matched constant current sources, whose operation is stabilized by the same circuit that regulates the input stage. Rather than obtain a common-mode feedback voltage with resistors as in Figure 2, Q_{10} and Q_{11} are used, saving chip space reducing emitter follower loading, and giving a fixed voltage drop at the summing point. Two emitter followers, Q_{24} and Q_{32} are available as gain control inputs, allowing considerable control versatility, and may be used as peak detectors, as well. Control input overvoltage protection is provided by zener diodes (reverse base-emitter junctions), Q_{33} and Q_{34}, while feedback amplifier excursion is limited by another zener, Q_{35}. Bias levels are set so that AGC action begins when the applied control voltage equals three forward diode drops, about +2.1V. As control voltage is further increased, gain is reduced by progressively shunting current from Q_3 and Q_6 into Q_4 and Q_5; the "transition width" of the system is about 400 mV, so that above approximately +2.5V, minimum gain is obtained. These control levels were chosen to be compatible with tuned gain control amplifiers, such as the LM171 RF/IF amplifier, elsewhere in the system, and to allow the circuit to be driven, in switched-gain applications, by standard monolithic 5V logic, such as TTL, DTL, or RTL.

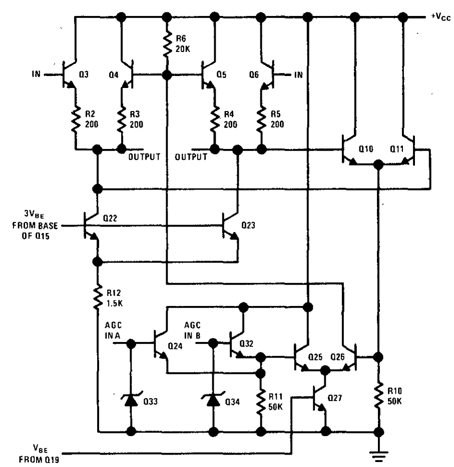

FIGURE 6. LM170 AGC Section

To increase usable dynamic input range, and decrease distortion, R_2, R_3, R_4 and R_5 are added to the differential gain control section. These resistors have little effect on other circuit parameters, but help to "linearize" the transfer characteristic throughout the gain control region.

The output stage, Figure 7, provides large common-mode rejection, and a single-ended output, which has a quiescent value halfway between ground and the positive supply. Output stage voltage gain is a function of supply voltage, being approximately 100 (40 dB) at V_{CC} = 12V. Thus, except for its lower gain, the LM170 has the same configuration and essential characteristics as an operational amplifier.

Output impedance is intentionally high (5000 ohms), and short-circuit resistant. Thus, any num-

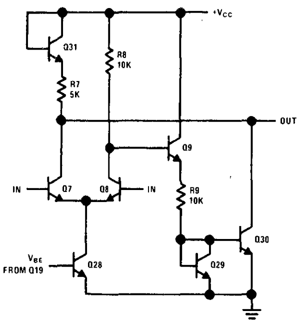

FIGURE 7. LM170 Output Stage

ber of LM170's may be directly tied together at their outputs, for multi-channel mixing or switching applications.

For AGC systems, output signal voltage is usually peak-detected, and fed back to the gain control input, maintaining essentially constant output voltage with widely varying input signals. In the case of squelch, however, the output is normally completely off, in the absence of input signals; thus, control voltage for squelch operation cannot be derived from the output, but must be sampled before the gain-reduction stage. Figure 8 shows the built-in squelch amplifier and detector. Lateral PNP transistors Q_{12} and Q_{13} are constructed with two collectors each, so that differential signals drive the gain control stage, across R_{13} and R_{14}, and separately, from the second pair of collectors, drive Q_{20}, Q_{36}, and Q_{21}. The quiescent current from the extra collectors is regulated by the same feedback circuit that controls operation of the input stage. If an external resistor (or potentiometer) is connected from Pin 7 to ground, it will serve as collector load for Q_{12}, and can be user adjusted so that Q_{20}, normally saturated, turns off for peak signal voltages exceeding any desired value. When this happens, Q_{36} and Q_{21} turn on, discharging an external capacitor, and bringing the voltage at Pin 6 below the threshold required to turn the amplifier fully on. Since the collector load for Q_{20} is a current source, in parallel with a high impedance Darlington pair, Q_{36} and Q_{21}, the voltage gain of the squelch detector is very high, and abrupt action occurs with even small incoming signals.

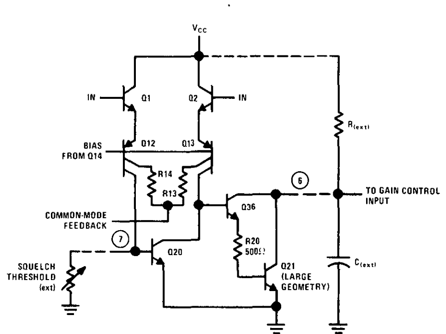

FIGURE 8. LM170 Squelch Detector

The external capacitor and large charging resistor can be chosen for time constants up to several seconds, for releasing the squelch; the geometry of Q_{21}, however, is large, allowing a very fast discharge of the time constant capacitor, so that effective fast-attack, slow-release squelch occurs. Since Q_{21} is part of a Darlington, and has a base current limiting resistor, R_{20}, it will neither saturate nor damage itself when large electrolytic capacitors are used; however, it will draw sufficiently large currents to bring the capacitor below the 2.1V gain control threshold, and then taper off in discharge rate.

GENERAL APPLICATION CONSIDERATIONS

As with any device capable of producing gain, when using the LM170, consideration must be given to proper layout of the device and its external circuitry to prevent any undesirable feedback that may cause oscillation. Since the inputs may be biased either directly from V_{CC} or indirectly through a divider network, effective power supply bypassing is essential. To guarantee effective bypassing at all frequencies, multiple bypassing should be used. A large capacitor, 10 μF or greater, should be used to absorb all low frequency power supply variations and a smaller capacitor, approximately .01 μF, to prevent any high frequency feedback through V_{CC}. These should be located as physically close to the device as possible.

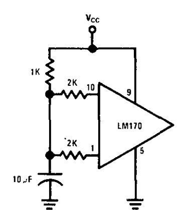

FIGURE 9. Input Biasing and Decoupling Network

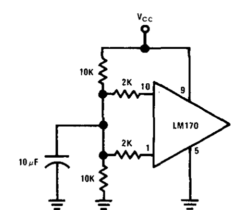

FIGURE 10. Input Biasing and Decoupling Network

Additional DC input stability may be necessary. This is most easily accomplished by a series RC roll-off from V_{CC} to the inputs to ground. If the inputs are to be biased directly from V_{CC}, the network should be connected as in Figure 9. Values of 1k ohms and 10 μF give a roll-off that is 3 dB down, at approximately 17 Hz. Since the input bias current is typically around 8.0 μA, the voltage drop across the 1k ohm resistor will be negligible. If the inputs are biased at some common mode voltage less than V_{CC}, then the addition of a single capacitor from the common mode input point to ground accomplishes the same thing (see Figure 10). Again, a value of approximately 10 μF will give effective roll-off.

The input stage exhibits the same high tolerance to abuse as does the LM101; large currents forced into either input (when input voltage exceeds the positive supply by more than 0.7V, for example) should be avoided. If such transients normally occur in the system, as frequently is the case during turn on or turn off, protect the inputs with series input resistance.

An inspection of the self-balancing action within the LM170 explains how large gain changes can be achieved, without appreciable DC output shift. Obviously, if all components in the circuit are exactly matched, this will work perfectly. There are two possible sources of DC output shift in the LM170. The first is an unavoidable small V_{BE} mismatch between critical components, causing small differential shifts to appear ahead of the output gain stage, along with the usual large common-mode shifts. Units are selected, to various specifications, at the factory, for low output shift. The second source of DC shift is externally induced input offset voltage. As with any operational-type amplifier, a certain bias current must flow into each input, in the microampere range, to operate the input transistors. While input offset current (the difference between the two input currents) is very low, use of unequal source resistances will cause different voltage drops across each input resistor or a net input offset voltage. For critical applications, then, especially if large input resistance is used, it is recommended that equal input resistors be used. Conversely, if the least expensive graded units are used, and minimum output shift is still of importance, input offset voltage may be individually trimmed for each unit, to give nearly ideal characteristics, as observed on an oscilloscope.

Another serious source of offset can occur when a large capacitor is used to couple to the input of the LM170. This may cause brief periods of positive feedback during a portion of the input waveform cycle, during which the device may oscillate. This may be easily prevented, however, by connecting a capacitor of approximately the same value as the input capacitor from the unused input terminal to ground.

Gain control inputs, Pins 3 and 4, are shunted by 6.5V zener diodes. If control voltage is anticipated to go above +6.5V, and if the driving source is capable of providing more than about 10 mA under these conditions, it is advisable to protect the zeners with a series resistance at each gain control input.

While the large geometry squelch output transistor, Q_{21}, is capable of sinking large instantaneous discharge currents from electrolytic capacitors, it is not advisable to attempt sinking large (more than 50 or 100 mA) continuous currents from "stiff" voltage sources, which may cause large dissipation on the chip.

The LM170's ability to accept common-mode input voltage equal to the positive supply can be a great convenience to the circuit designer, and saves several components, in such applications as direct dynamic microphone drive. It should be realized, however, that this system works only with the small (under 100 mV) input signals for which the circuit was intended. While input transistors Q_1 and Q_2 still are effective as emitter followers with zero, and even less than zero volts collector-to-base, large positive base voltages (more than about 400 mV above the positive supply, will allow Q_1 and Q_2 to saturate, degrading amplifier gain, input impedance, bandwidth, and input bias current. Normal operation should never see more than about 50 mV of input signal, so that this is not a problem.

AGC APPLICATIONS

AGC Using Built in Detectors

In most systems, the LM170 will be followed by further voltage amplification. This may be advantageous, as it can provide increased forward gain in the AGC loop, resulting in tighter output regulation. In systems having widely varying load impedances, AGC derived from the system output can automatically compensate for additional output loading. Connected as in Figure 11, the emitter follower at Pin 4 is used as a high impedance detector, with detector smoothing performed by a capacitor at Pin 2. DC threshold for the detector is set at any desired level by a potentiometer, determining the positive peak output voltage which initiates gain regulation.

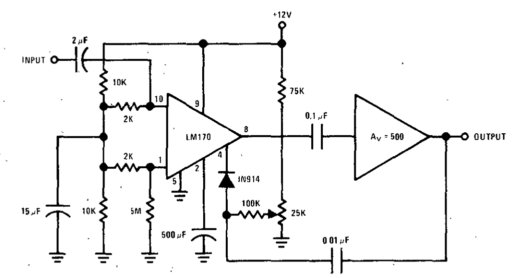

FIGURE 11. LM170 AGC Using Internal Peak Detector and Additional System Gain

A word of caution is necessary here. When operating the LM170 with an external gain stage to provide very high AGC loop gains (on the order of several hundred), proper layout is essential. As with any high gain circuitry, good power supply regulation is a necessity. Multiple bypass capacitors are used (Figure 11) to give effective wide band filtering. This should prevent any undesirable ripples or transient spikes from being transferred from one device to another through V_{CC}.

Depending on the amount of external loop gain desired, several other steps may be necessary. As with many other AGC circuits, there is a DC shift in output voltage associated with the change in applied AGC control voltage. If this shift is fast enough and of sufficient magnitude, it may be coupled from the output of the LM170 to the following gain stage. This may cause severe spiking in the output of the LM170 which may swing the gain stage into limiting causing extreme distortion. This can be prevented by providing a given amount of offset in a given direction to the input of the LM170. If an increase in AGC voltage at the AGC threshold causes a positive shift in output voltage, it may be fed back through the system to cause a further increase in AGC control voltage. If, however, an increase in AGC voltage causes a negative shift in output voltage, when this shift is fed back it will tend to decrease AGC voltage which should help to prevent the spike from occurring. In normal application, the LM170 inputs are biased with approximately 2 kΩ resistors. If a resistor on the order of 5 MΩ is tied from the inverting input (Pin 1) to ground, it will provide enough offset to control both the direction and magnitude of the output shift. A potentiometer may be substituted to trim the offset to any desired value.

The other problem that may occur can result from too large an AC swing at the AGC control point. Pins 3 and 4 are protected from positive over voltages by a 6.3V zener. If the AC swing is so large that it swings negative below .7V, the zener will be forward biased. If this occurs, a parasitic NPN transistor can be formed causing an undesired transistor action. To prevent this, two solutions are available. In the first a germanium diode can be used to shunt all negative swings from the AGC pin to ground. It is tied directly from the AGC pin (Pin 3 or Pin 4) to ground, being forward biased if the AC signal tries to swing negative. The alternate method, as shown in Figure 11 is a silicon diode in series with the AGC pin. It is forward biased for all positive voltages so DC bias is provided and all positive going AC swings provide proper AGC action. All negative swing are promptly cut off at +0.7V.

Care should be taken to avoid exposing the circuit to any RF radiation or 60 Hz power line fields as they may get into the high gain loop and cause erratic AGC action. Coupling capacitors should be selected to give proper operation over the desired range of frequencies. In Figure 11, the low frequency limiting factor is the .01 AGC feedback capacitor which gives a roll off near 160 Hz. Increasing its size would proportionally lower the low frequency cutoff.

Figure 12 shows the output regulation resulting from this system with an added 46 dB of voltage gain following the LM170.

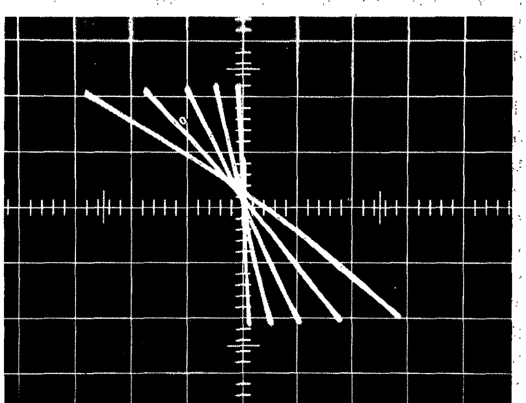

FIGURE 12. AGC Transfer Characteristics, Internal Detector, For Varying Inputs

Vert. = output, 10 mV/cm
Horiz. = input, 10 mV/cm

Both available AGC inputs may be used, as in Figure 13, to provide full-wave output detection, which responds to both positive and negative output peak voltages.

If a transformer is used to provide full wave AGC detection as shown in Figure 13, it must be chosen to meet two criteria. First, it must have a high enough input impedance to avoid loading down the

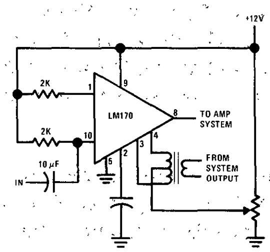

FIGURE 13. Internal Full Wave AGC Detection

output of the LM170 or of following gain stages if they are used. If driven directly from the output of the LM170, a primary impedance greater than 50 kΩ is acceptable. Figure 14 shows that AGC voltage inputs greater than approximately 2.5V will provide maximum available gain reduction. There-

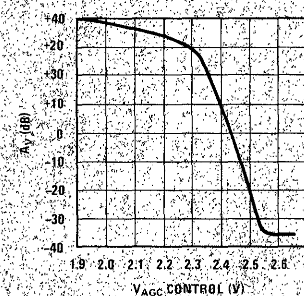

FIGURE 14. Typical Voltage Gain vs AGC Control Voltage (Pin 3 or Pin 4)

fore if the transformer output provides a voltage swing of approximately 3V peak, it will be more than adequate to operate the LM170 over its entire AGC range.

AGC CIRCUIT WITH TRANSISTOR DETECTOR

In Figure 15, an external PNP transistor acts as a negative peak detector, with threshold set by a potentiometer. In its quiescent state, the PNP transistor is off; negative going signal peaks, AC coupled to the detector, cause momentary conduction, which turns on the high impedance gain control input, Pin 4. Pin 2 is bypassed by a relatively large capacitor which will charge, and maintain a sufficient DC voltage to operate the amplifier's gain at the correct level. This level, set by the threshold potentiometer, is the point at which negative peaks marginally turn on the PNP transistor. Thus, as input signal level increases, the circuit automatically lowers gain, to maintain a constant peak-to-peak output level. Since the capacitor at Pin 2 cannot follow instantaneous audio

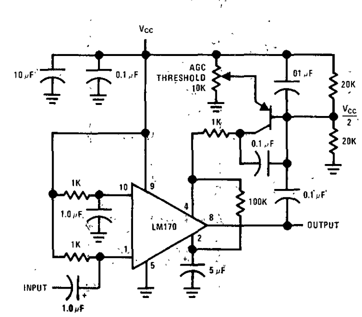

FIGURE 15. AGC Circuit with External Peak Detector

variations, audio frequency linearity is not disturbed, although charging from the low impedance of Pin 2 and discharging through a much higher resistance, causes fast attack, slow release AGC action.

In this example, common-mode input bias is obtained directly from V_{CC}, through equal resistors, to minimize offsets resulting from input bias current.

The family of transfer characteristics, Figure 16, shows that some output increase occurs as the input increases, but by only a small percentage.

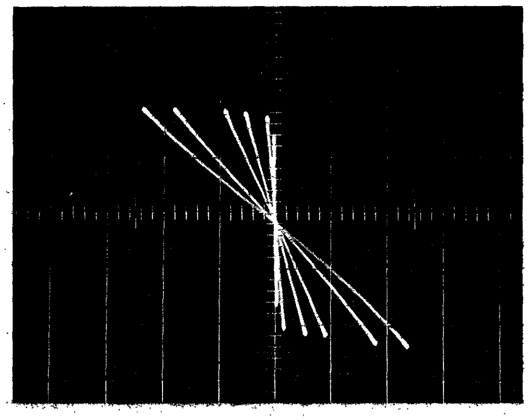

FIGURE 16. AGC Transfer Characteristics Transistor Detector, For Varying Inputs

Vert. = output, 10mV/cm
Horiz. = input, 10mV/cm

When using an external peak detector, proper layout and biasing are essential to prevent the transistor from oscillating. As always multiple bypassing of the power supply should be used. In addition, a capacitor of approximately .01 μF should be connected from the base of the PNP to the collector and from the base to V_{CC}. These prevent any positive feedback from causing the external peak detector to oscillate.

SQUELCH APPLICATIONS

Squelch Preamplifier with Hysteresis

Audio squelch is useful in noisy acoustic environments, to suppress background microphone noises, and in receiving systems, where the constant clatter

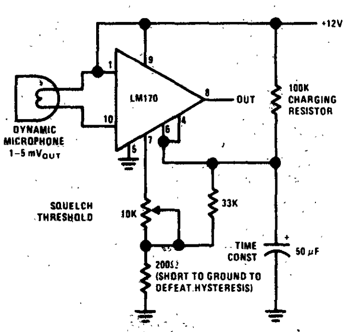

FIGURE 17. Squelched Preamplifier with Hysteresis

of an unused transmission channel must be removed, until useful information is received. The squelch circuit of Figure 17 includes a number of refinements, which make it smooth-acting, and easy on the ear of the listener.

The threshold potentiometer at Pin 7 is manually set to cut in at any desired input level. The large capacitor at Pin 6, and its associated charging resistor, may be chosen to give squelch release times of as much as several seconds, while the large current sinking capability into Pin 6 assures fast attack, so that first speech syllables are not lost.

A portion of the voltage at Pin 6 is fed back to the threshold potentiometer; since there are two stable voltage states at Pin 6, this creates a controlled amount of hysteresis in the squelch circuit. Thus, there exists a "dead band" of squelch sensitivity, which greatly enhances the circuit's immunity to rapid transmission channel fading, or erratic speech patterns. Combined with the slow-release characteristic, hysteresis gives a very well-behaved squelch system. A typical threshold control setting might be one at which amplification begins above a 20 mV p-p input. With the feedback values shown, the input level must consistently stay below 12 mV p-p before gain is cut off. The small feedback resistor may be eliminated if hysteresis is not required.

While squelch attack is abrupt, release follows the slow charging contour of the time constant capacitor, through the logarithmic gain control region. Thus, gain "fades out" following cessation of speech, rather than the less ear-pleasing effect of conventional squelch circuits, in which a rush of background noise may be heard, followed by an abrupt and often percussive cutoff.

The time constant capacitor is charged by a voltage divider, rather than a single resistor, so that its quiescent charged voltage is about +3V, with the values shown, from a +12V supply. There is no need to charge the capacitor much above this point, because gain has already been completely cut off, and further charging only makes more work for the large geometry transistor at Pin 6, in performing its rapid discharge function. In any event, if a single charging resistor is used, the timing capacitor cannot charge above about +6.5V, because both Pins 3 and 4 are shunted internally by protective zener diodes.

In Figure 17, the LM170 appears in another of its many possible input configurations. It is directly driven by a low resistance dynamic or controlled-magnetic microphone, with no other input biasing components required. The amplifier is compact enough to fit inside even the smallest commercial microphone cases; its low current drain from supplies between +4.5 and +6.0V would permit inclusion of batteries within the same case.

Figure 18 illustrates how a large number of such microphones could be directly connected to a

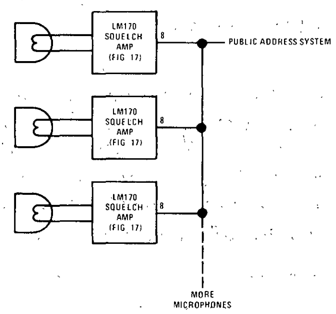

FIGURE 18. Random Access Microphone System

common bus, at their outputs, to give a random access, automatic break-in public address or paging system, which might be useful, for example, at a large conference table, or in a courtroom. While background noises at each microphone location would be suppressed, close talking would immediately allow one or more speakers to be heard. Because squelch switching levels are compatible with TTL logic, a priority logic system could be devised, which would not only give certain speakers "break-in" priority, but allow them to automatically cut off certain other speakers at the same time.

TRANSMITTER OR TAPE RECORDER VOX

In addition to squelching its own gain, the LM170 can become a voice-operated-relay control, or VOX, to switch high powered electronic or electromechanical devices. Automatic transmit-receive operation is possible in two way communication systems, or tape recorder motors may be switched on at the first syllable of infrequent speech, such as in dictation, conserving tape.

To handle large amounts of power, all that is needed is a small PNP power transistor, driving a relay, which can have multiple poles. Action is essentially the same as in squelch operation, except that the capacitor discharged by Pin 6 is charged by the relay driving circuitry. The amplifier may simultaneously be used as a continuous-running preamplifier, may be squelched along with the relay, or may even operate with an independent AGC signal, into Pin 3 or 4.

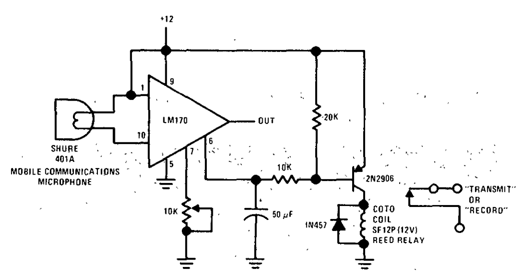

FIGURE 19. VOX Preamp

A reed relay is shown in the schematic of Figure 19, but any fast acting relay may be used. The relay coil is shunted by a diode, to protect the PNP transistor. If power supply impedance is high the circuit may tend to oscillate; bypassing the supply with a fairly large capacitor will eliminate the problem.

OSCILLATORS

Wien-Bridge Oscillator Using the LM170

The classic Wien-Bridge Oscillator is still a popular choice for many designs.

A brief review of the principle of this form of oscillator will show how ideally suited is the LM170 to this configuration.

Figure 20 shows the general configuration of the Wien-Bridge oscillator.

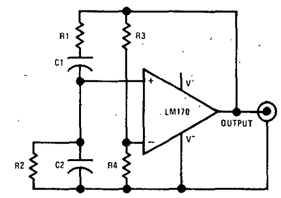

FIGURE 20. General Wien-Bridge Oscillator Configuration

The components R_1C_1 and R_2C_2 form a positive feedback network whose transfer, it can be shown, is a maximum when the lead produced by R_1C_1 and the lag afforded by R_2C_2 have the same value. At this condition the "gain" of the network's is

$$A_V = \frac{1}{(1 + R_1/R_2 + C_2/C_1)}$$

and the frequency is given by the expression:

$$f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

R_3 and R_4 form a negative feedback loop and control the gain of the amplifier. For sustained oscillation, the loop gain of the system must equal unity (in practice slightly greater), therefore the condition for oscillation is

$$\frac{R_3 + R_4}{R_4} = 1 + \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

or

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

Amplitude control of an oscillator assists in stabilizing its frequency as well as amplitude since it prevents the poles from wandering about on their root locus plot with gain changes and ensures starting.

Practically, one of the negative feedback resistors is often made voltage sensitive to ensure reliable starting and to control the output amplitude. If R_3 is chosen to be voltage sensitive, its characteristic has to be negative (such as a thermistor) or more usually R_4 is the control element, using, very often, a light bulb which has a positive voltage-resistance characteristic.

The simple elements such as the thermistor and light bulb rely for their action on their thermal characteristics. The response time for these devices limits their usefulness.

Alternatively the gain of the amplifier itself may be varied to afford amplitude stability.

It can now be seen how the LM170 dovetails nicely with the Wien-Bridge Oscillator configuration. It has gain, plus and minus inputs and an auxiliary control of gain via its "AGC Control inputs".

Figure 21 shows a suitable low-frequency oscillator design embodying the principles just discussed.

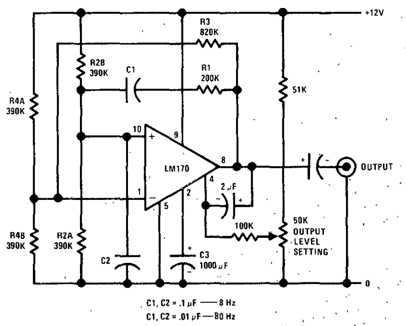

FIGURE 21. Wien-Bridge Oscillator

The positive feedback loop from Pin 8, the output, to Pin 10 uses R = 200k and C = .1 for 8 Hz. The R of the lag arm is formed from two resistors which provide bias for Pin 10, they are of course in parallel with regard to signal. The bias for Pin 1 is provided in the same manner. The 820k resistor together with the bias resistors provides a maximum loop gain of about 4, the system needs a gain of three for oscillation since the attenuation of the positive feedback loop at resonance is 3.

The resulting output is peak detected at constant Pin 4 of the device which is the base of an emitter follower biased by the external adjustable potentiometer chain, the amplitude adjustment. Detector smoothing is provided by the 1000 µF capacitor connected to Pin 2, the emitter of the detector emitter follower. The large value is dictated in this particular design by the desire to achieve regulation at about 10 Hz.

The frequency may be changed by changing only the capacitors up to a few kHz, beyond that it is desirable to reduce the bridge resistor values so that the input current offset characteristics of the LM170 do not limit the performance. Oscillators up to a few MHz may then be fabricated.

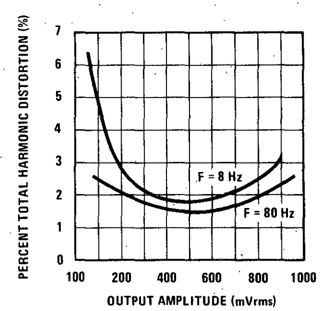

FIGURE 22. Oscillator Distortion vs Output Level

Figure 22 shows the distortion versus output amplitude of the circuit shown in Figure 3 for 8 Hz and 80 Hz versions of the oscillator.

Decade Tunable Oscillator

By using a modified twin-tee feedback network, the LM170 will produce a sine wave oscillation, tunable over one decade in frequency. The technique used is shown in Figure 23 where wideband positive feedback is applied to the non-inverting input by the capacitive divider C_1 & C_2. Capacitor C_1 also decouples the input from supply noise.

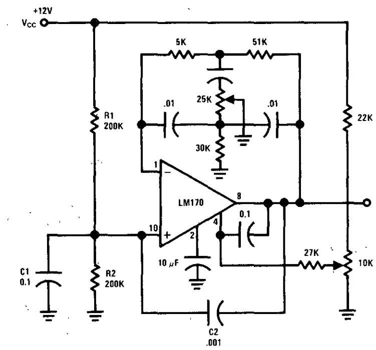

FIGURE 23. Decade Tunable Oscillator

Negative feedback occurs through the twin T at all frequencies except the null frequency of the T network, allowing the circuit to oscillate there. The nominal low frequency of oscillation for the circuit is approximately 320 Hz with the assymmetric parallel T shown. At this frequency and 1V rms out, the total harmonic distortion is under 0.25%. At the upper frequency limit, 3300 Hz the output has dropped less than 1.5 dB and the distortion is 0.45%.

A Modulated 455 kHz Signal Generator

An inexpensive, high "Q", 455 kHz ceramic filter may be substituted for the twin-tee feedback net-

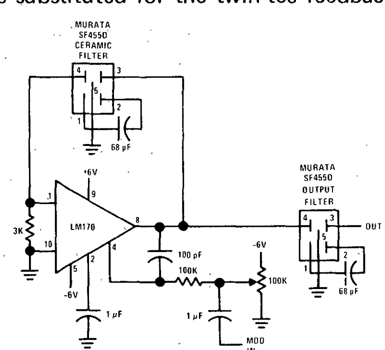

FIGURE 24. 455 kHz Modulated Constant Output Oscillator

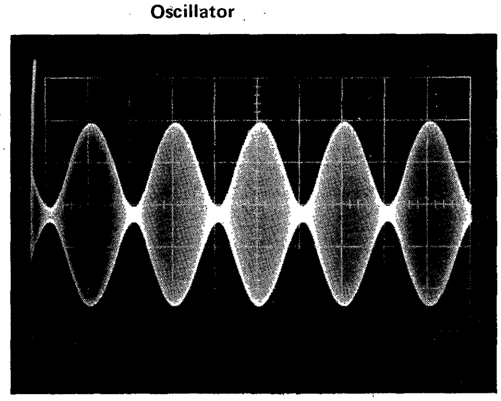

FIGURE 25. 455 kHz Modulated by 100 Hz

work of the previous example, to create a regulated-output AM IF alignment generator, Figure 24. If the AGC threshold voltage, which determines stabilized output, is varied at a low (audio) rate, the output amplitude will be forced to track the audio modulation, as in Figure 25.

The input configuration shown in Figure 19 may be used when two power supplies are available elsewhere in the system, as it allows the inputs and output of the LM170 to be referred to ground. Of course, any other suitable input biasing scheme may be used instead, for the 455 kHz signal generator.

Simultaneous Squelch & AGC Using the LM170

An interesting application of the LM170 involves simultaneously obtaining AGC and a fast attack, slow release squelch. It has been contributed by B. Chandler Shaw of Bendix Electrodynamics, North Hollywood, California.

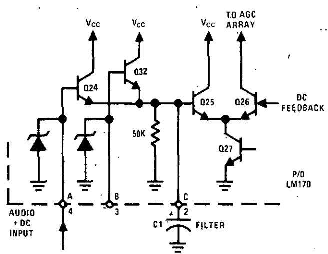

FIGURE 26. Internal AGC Control Circuitry

In normal AGC operation, a filter capacitor is required on Pin 2 to store the peak AGC control signal. The circuitry involved, shown in Figure 26, uses the emitter follower Q_{24} as a buffer and peak detector. Obviously, the voltage on the filter capacitor can be rapidly increased (lowering the gain) by the current available through the emitter follower but decreases slowly by discharging through the 50k resistor (increasing the gain). This is exactly opposite of what we require. The normal squelch circuitry, shown in Figure 27 connects one of the AGC control pins, Pin 4, to the collector of a saturating switch, Q_{21}, at Pin 6. With no signal, Q_{20} is saturated and Q_{21} is off, and Pin 6 sits at the voltage determined by the supply and resistive dividing network, or by the internal zener.

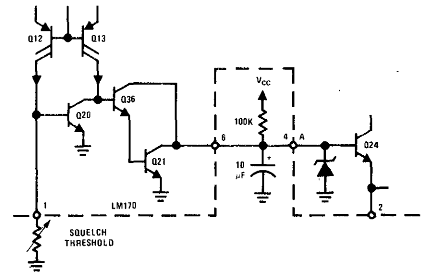

FIGURE 27. Normal Squelch Circuit

Note that no capacitor is connected to Pin 2. When the combination of peak decreasing signal currents and low enough shunt-values of Squelch Threshold control are such that the base drive for Q_{20} no longer causes saturation, Q_{36} and Q_{21} immediately turn on, rapidly discharging the capacitor at Pin 6, lowering the voltage at Pins 4 and 2, and bringing the amplifier quickly up to full gain. Upon cessation of the signal, Q_{20} saturates again turning Q_{36} and Q_{21} off, and the voltage at Pin 4 rises according to the RC time constant of the network, giving some delay, and finally a smooth turn-off of the amplifier.

If a filter capacitor were connected from Pin 2 to ground, it would not be possible to lower quickly the voltage at Pin 2 to obtain a fast attack squelch. However, if the capacitor C_1 is connected to Pin 6, as shown in Figure 28, Pin 2 is drawn down rapidly when unsquelching and the low impedance path through Q_{21} provides the ground for the filtering action required for AGC with signal and threshold level applied at Pin 3. With no signal, Q_{21} turns off and the voltage at Pin 4 rises nor-

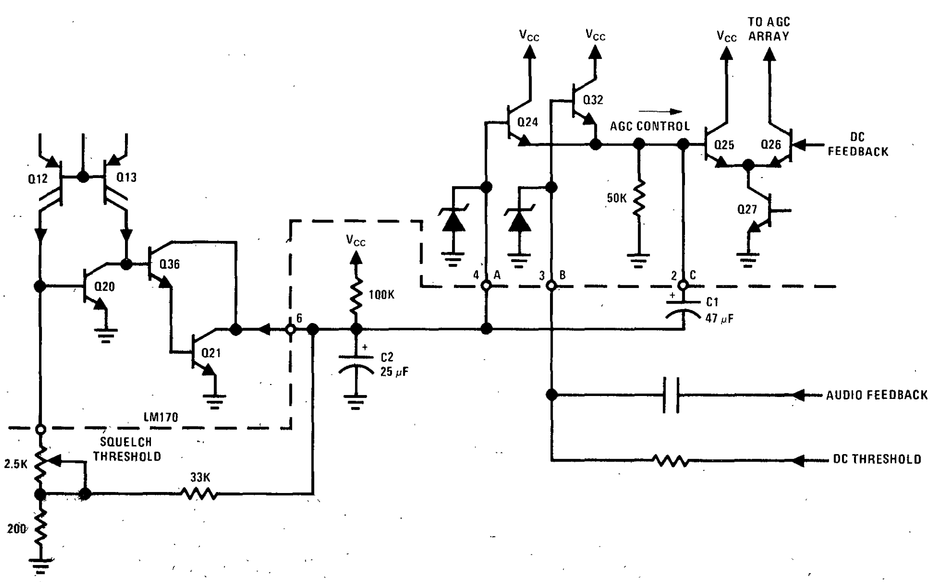

FIGURE 28. Simultaneous Squelch and AGC

mally, slowly squelching the amplifier. Note that C_1 becomes reverse biased with no signal. Since the voltage between Pin 4 and 2 is only one diode drop, this is insufficient to forward bias the capacitor and no deforming occurs. Hysteresis is provided by the positive feedback to the bottom end of the threshold control through the 33k resistor.

Temperature Compensating Techniques

The LM170 AGC control circuit is designed for a "transition width" of approximately 400 mV, to go from full gain to practically zero output swing. Due to this narrow control voltage width and to the AGC control stage being biased essentially from a three diode chain, the gain of the LM170 is subject to large variation with temperature. (See data sheet for curves of A_v vs Control Voltage at different temperatures.) With approximately a 2 mV per degree C shift per diode the three diode chain bias voltage can vary by 600 mV over a ΔT of 100°C. As a worst case, at a given control voltage of 2.4V at room temperature, the gain may vary from +40 dB at −55°C to −30 dB at +125°C. This necessitates the use of an external voltage compensation circuit that can stabilize gain variations over any temperature range from −55°C to +125°C.

Two circuits were found to be quite effective in reducing voltage gain drift. The first has less components but is less flexible, while the second is slightly more difficult to adjust but gives a wide degree of compensation over the guaranteed temperature operating range.

The first circuit is shown in Figures 29A and 29B. Figure 29A has only two diodes and is used only where a maximum shift of 4 mV/°C in AGC control voltage is required. This will be effective at gain levels only slightly below maximum. From the curves it can be seen that at lower gain levels, more than 4 mV/°C of compensation is required so the three diode chain shown in Figure 29B is used. Adjustment is simple. Once the amount of compensation needed is found from the curves and the correct circuit is chosen, potentiometer R_1 is adjusted to give the desired gain.

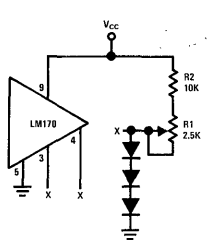

FIGURE 29A. Temperature Compensating Circuitry

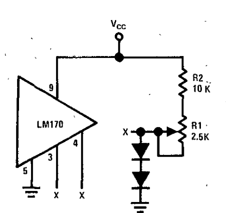

FIGURE 29B. Temperature Compensating Circuitry

If a more flexible circuit is desired, the one shown in Figure 30 can be used. Transistor T_1 biased by R_4 and $2R_4$ provides a maximum of 6 mV/°C thermal coefficient. Potentiometer R_1 shunting T_1, is adjusted to provide the amount of compensation needed. Potentiometer R_2 then sets the AGC control voltage going to Pin 3 or Pin 4 of the LM170 to give the desired gain. To adjust this circuit, the amount of thermal compensation needed is determined from the curves as before. The temperature shift over the desired operating range and the amount of gain needed are also known. Therefore, the amount of DC shift in AGC control voltage is also known by taking it straight from the A_v vs Control Voltage curves. This gives the number of mV per degree C required. Potentiometers R_1 and R_2 are then set to give proper operation. An example is shown below:

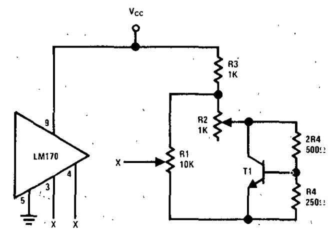

FIGURE 30. Temperature Compensating Circuitry

Gain Required	30 dB
Operating Temperature Range:	−55°C to +125°C
Change in AGC Control Voltage (from A_V vs Control Voltage Curves in data sheet)	1.9V to 2.7V = 800 mV
This means	$\frac{800 \text{ mV}}{180^\circ\text{C}}$ or 4.4 mV/°C

Potentiometer R_1 shunts T_1 thereby reducing the compensation from a maximum of 6 mV/°C. The value of R_1 was chosen to be approximately 10k ohms to prevent an unnecessary waste of current from V_{CC}.

$$\text{Let } R_1 = 10\ k\Omega$$

To set for a T.C. of 4.4 mV, set R_1 to 4.4/6.0 or 74% of its total value or 7400 ohms.

Now potentiometer R_2 is used to set the AGC control voltage to give a gain of 30 dB.

The relative displacement of the three temperature curves on the A_v vs Control voltage plot clearly shows that the relation between control voltage and temperature is not linear. Therefore, since both of the compensating techniques described above are approximately linear, some gain change with temperature is to be expected. This shift is minimized however, by either of these simple, easily adjusted, circuits so that total variations in gain less than ±3 dB over the entire operating range is possible.

Conclusion

The LM170 is an extremely versatile system component, allowing squelch and AGC in inexpensive communication systems. As a general purpose variable gain element, the device opens up many new areas of circuit design, in which closed loop gain feedback may be used to control other parameters, heretofore never considered as convenient variables. Its compatibility with ordinary monolithic logic creates possibilities in digital-communication system interfacing. The applications discussed in this report should stimulate fresh thinking, in finding new and useful services for a unique variable circuit element made possible only by monolithic technology.

APPENDIX

Squelch Release Timing

The timing capacitor from Pin 6 to ground in Figure 17 is charged by an external resistor (nominally 100 kΩ), to determine the delay between cessation of speech and turnoff of the LM170. Figures 31, 32 and 33 show timings available from 5, 10 and 25 μF capacitors. The upper trace is the input, 15 20 mV/cm. Notice that the input does not have to be completely shut off, but must only remain below the externally set squelch threshold long enough for the timing capacitor to charge to the gain control region. Both traces are shown at 200 ms per division.

The lower trace is the amplifier's output. At first, since input level is below the squelch threshold, output is zero. An abrupt increase in input level above the threshold causes almost immediate turn-on of the amplifier. When input level is decreased to its original value, amplifier output follows linearly, because gain is still at its maximum value. A delay period follows, during which the timing capacitor charges from the low voltage (less than 1V) previously forced by the squelch output, Pin 6, up to the gain control region, which begins at about +2.1V. The capacitor is still charging along an exponential RC curve while it passes through the gain control region, so that a gradual turnoff is observed, rather than the less pleasant abrupt turnoff of conventional squelch systems.

As an alternative to choosing different timing capacitor values for different release times, a single value may be used along with a potentiometer which would replace the 100k charging resistor. This would allow a front panel variable delay control, accessible by the system user.

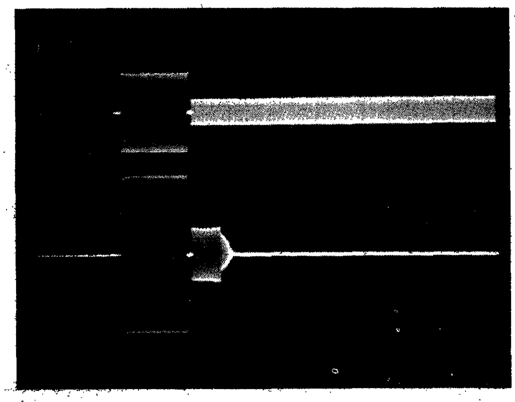

FIGURE 31. 5 μF Capacitor Timings

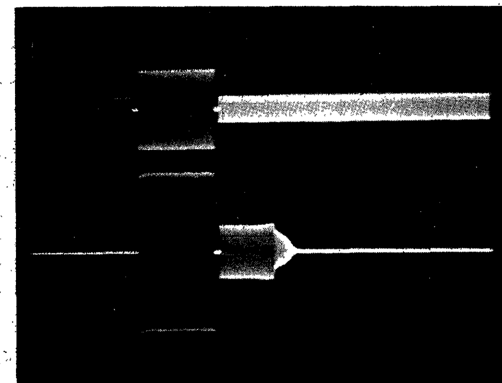

FIGURE 32. 10 μF Capacitor Timings

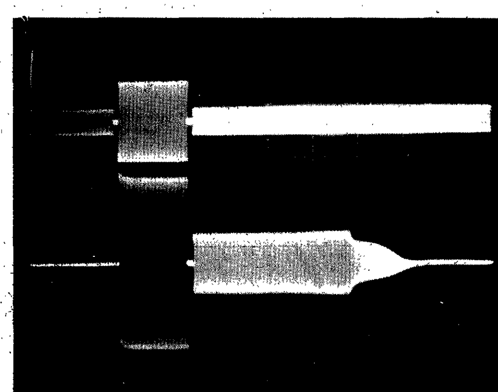

FIGURE 33. 25 μF Capacitor Timings

September 1971

HIGH SPEED ANALOG SWITCHES

SUMMARY

In the past, many factors combined to make precision, high speed analog switching circuits complex and expensive, if not impossible. A unique monolithic J-FET family opens new analog switching applications which require high toggle rates, high frequency signal handling ability, and high level analog signals with broad dynamic range.

Called the AM1000, AM1001 and AM1002 analog switches, these devices were developed specifically for high speed analog switching applications. The AM1000 series overcomes the problem of slow switching speed normally associated with junction FET analog switches. While MOS analog switches are noted for their high speed, they have the peculiar problem of their ON resistance being modulated by the analog signal level. The AM1000 series eliminates this problem too.

National's AM1000 series analog switches are simple N-channel monolithic integrated circuit J-FETs. They are packaged in TO-72 (4-pin TO-18) headers to reduce circuit board space and yet retain the advantages of a hermetically sealed package.

WHAT IS AN ANALOG SIGNAL?

An analog signal is an electrical voltage (or current) whose level is an analog of certain information. This information can be an electrical level itself, a voice signal, an electrical analog of a pressure, temperature, position, etc., or any other data source. The analog information may also be preconditioned by logarithmic compression or expansion, or other desired "distortion." If the analog information does not vary quickly with time and if many analog signals have to be handled in a system, the analog information may be sampled periodically rather than monitored continuously. Sampled data systems can dramatically reduce cost and weight by proper utilization of available information channel bandwidth where the cost of additional data channels becomes expensive.

The telephone companies are probably the most adept at signal multiplexing, but other applications are beginning to appear. Modern aircraft are using multiplexing to reduce weight in wire harnesses. Any applications requiring long multiconductor cable runs are prime targets for economic use of analog signal multiplexing.

TIME DOMAIN MULTIPLEXING

There are two basic types of multiplexing: frequency domain multiplexing and time domain multiplexing. Frequency domain multiplexing is common in RF communications, it uses a number of subcarriers on a data channel, each subcarrier being modulated in some manner. An example would be FM radio standard broadcast which has home stereo multiplex information (a suppressed carrier double sideband subcarrier) and the SCA commercial "background music" multiplex information (an FM modulated subcarrier). When the number of data channels becomes great, frequency domain multiplexing becomes difficult to implement.

In time domain multiplexing, a certain time slot is allowed for sampling of a particular data line. Thus, if you sample some analog information during a 10 μs time slot at a 10 kHz rate, you have time "left over" to sample nine other signals at 10 μs intervals at a 10 kHz rate. If you can improve the analog switch device to execute a suitable sample in only 1 μs, you have made a tenfold improvement and you have the choice of increasing system channel capability to 100 channels (with no change in analog signal bandwidth), increasing analog signal frequency bandwidth by 10 times (with no increase in channels), or a compromise between increasing signal bandwidth and increasing the number of data channels. This is what the AM1000 family of analog switches is all about; they allow shorter sampling times for a given signal accuracy.

WHAT MAKES A GOOD ANALOG SWITCH?

There are five principle parameters which determine how good an analog switch is:

- ON resistance
- ON resistance modulation
- OFF resistance
- Offset voltage
- Commutation rate

There are other considerations which may also be significant for special cases, but these five will almost always have significant bearing on a system design. For most applications, there are two devices which are the most popular—MOS switches and J-FET switches. Relays normally would be a good choice but they won't toggle very fast. In general, the MOS switches have had a speed advantage, and ease of fabrication advantage, whereas the J-FET switches have an advantage of lower ON resistance, no ON resistance modulation, higher voltage capability.[4,5,6] The AM1000 family of analog switches have all of the advantages of the J-FET plus high speed which makes it superior to any MOS switch in a precision system.

WHAT MAKES THE AM1000 FAST?

Figure 1 shows a typical J-FET circuit used in analog switching. Diode D_1 allows the gate drive signal to drive the gate negative thus turning off the J-FET switch. When the gate drive signal goes positive, diode D_1 decouples the drive from the gate and resistor R_g discharges the gate-source capacitance. R_g must be large so it doesn't load the analog signal, typical values for R_g are 100 kΩ and up; thus the gate capacitance—R_g time constant is large which precludes high switching rates. If C_{iss} of the J-FET is 15 pF nominal and R_g is 100 kΩ, the time constant is 1.5 μs thus making megacycle toggle rates impossible.

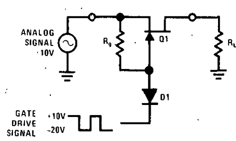

FIGURE 1. Typical J-FET Analog Switch

The AM1000 consists of three J-FETs. One large and two small ones. The large one acts as the analog signal pass transistor. The two smaller FETs act as a turn-on circuit which reduces switching transients.

The pinchoff voltage of all these FETs are almost identical and are all less than 10V. In Figure 3 (ignoring diode drops), the gates of all three FETs are at −20V and the AM1000 is turned off. There is at least −10V from gate to source of Q_1 so it is pinched off and leakage from input to output is in the pA range. Q_2 has −10V from gate to source so it is also pinched off and its current which shunts the input signal is in the pA range.

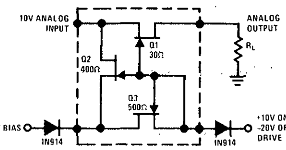

FIGURE 2. AM1000 Circuit

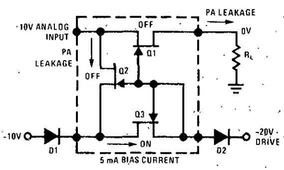

FIGURE 3. AM1000 Turned Off

Q_3 is operated at 0V gate-source so it draws saturation current, I_{DSS}. The bias supply for D_1 must be 10V more positive than the negative drive signal.

During turn-on, the drive signal ideally makes a step function change from −20V to +10V thus turning D_2 off. The gates of Q_1, Q_2 and Q_3 are then driven positive by the saturation current of Q_3 through diode D_1. The rate that this voltage slews is dependent on gate capacitance and I_{DSS} of Q_3. $C_{iss(off)}$ of the AM1000 is about 10 pF so the voltage slews at:

$$\frac{dv}{dt} = \frac{I_{DSS}}{C_{iss}} = \frac{5 \times 10^{-3}}{10^{-11}} = 5 \times 10^{8}\ \text{V/sec}$$

Within 5V of rise (about 10 ns), Q_2 begins to turn on and D_1 turns off. The remainder of the gate capacitance charge is discharged into the input (or source) of Q_1 via the ON resistance of Q_2 and Q_3. During this time interval the average series resistance of Q_2 and Q_3 is about 2 kΩ and the gate capacitance is changing from about 10 pF to about 25 pF. The approximate RC time constant is 20 pF and 2 kΩ, or 40 ns, depending on the level of the analog signal. Total turn on time is therefore about 50 ns. For a +10V analog signal, the correct analysis is a little more complex, but the AM1000 will turn on in about 70 ns for this circuit condition. The reason that the turn-on transient at R_L is drastically reduced is that the discharge path of gate capacitance does ***not*** flow through R_L. The small transient that may appear at R_L is due to the time that D_1 is on during turn-on.

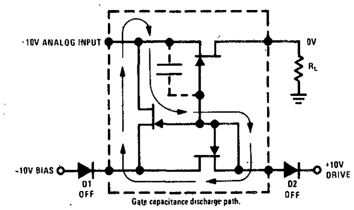

FIGURE 4. AM1000 Turning On

So, the AM1000 achieves its high switching speed because its R_g (see Figure 1) is very low during turn on, yet its R_g during the OFF state is in the G ohm range and thus doesn't load the signal.

TOGGLE RATE

The toggle rate (how fast the switch can be turned on and off) of an analog switch is not a simple straightforward parameter for a real system design. The reason is that most analog switches are specified at a ridiculously low impedance level; this is done in order to show the highest speed that the device can possibly go. This speed is not normally realistic for most systems designs. In order to demonstrate a realistic comparison, the AM1000 will be pitted against an MOS analog switch for a system with a ±10V analog signal swing.

TABLE 1: AM1000 – MOS Parameter Comparison

PARAMETER	AM1000	MOS ANALOG SWITCH
$R_{DS(on)}$ (Max)	30Ω	400Ω
$R_{DS(on)}$ (Min)	20Ω	150Ω
$R_{DS(on)}$ (Nom)	25Ω	275Ω
C_{iss} (Nom)	15 pF	7 pF
Breakdown Volts	40V	35V

$R_{DS(on)}$ and C_{iss} indicate the basic speed capability of the devices assuming low source and load impedance, here the AM1000 has a speed advantage of about 5:1 over the MOS switch.

The parameter that affects toggle rate the most, however is $R_{DS(on)}$ variation with analog signal level. At an analog signal of +10V, the MOS switch has an $R_{DS(on)}$ of 150Ω and for a −10V analog signal it has an on resistance of 400Ω. This variation of ON resistance is caused by the bulk gate to channel voltage modulating the ON resistance of the MOS switch.[5] Thus, the MOS switch has a design on resistance characteristic of 275Ω ±125Ω. The AM1000 has an $R_{DS(on)}$ of 25Ω ±5Ω and its resistance *does not* vary with analog signal level.

For a system of a given accuracy, the load impedance is determined by the variations expected in channel resistance. Assuming a system accuracy of ±0.5%, the AM1000 load resistance could be as low as 1 kΩ; the MOS switch load resistance would have to be 25 kΩ (±125Ω being 0.5% of 25 kΩ).

The capacitance of the AM1000 is about twice that of the MOS switch but the system load resistance is 25 times lower thus giving the AM1000 a toggle rate advantage of about 12 times over the MOS "high speed" analog switch. In order to graphically illustrate the superiority of the AM1000, two simple series switches were constructed; one with the MOS switch and one with an AM1000. The MOS analog switch was set up to sample a +10V DC signal, after being switched off, the output returns to ground level. The AM1000 was set up to sample a portion of the turn off transient of the MOS analog switch, each switch with a 0.5% system accuracy! Figure 5 shows the circuit used to obtain the oscillograph shown in Figure 6A.

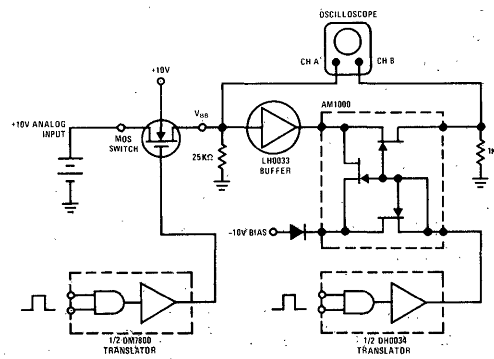

FIGURE 5. Analog Switch Comparison Circuit

A National LH0033 high speed buffer was used to sense the analog voltage at the load resistor of the MOS switch and drive the analog input of the AM1000. Figure 6A shows the oscillogram; the upper trace is the MOS switch turning off; its load voltage heading toward ground; the lower trace (oscilloscope vertical gain reduced slightly for photo clarity) shows the AM1000 sampling this switching transient. Figure 6B shows the timing pulses, the upper trace being the MOS drive timing and the lower is the AM1000 drive timing (positive indicating off for both devices). It is interesting to note that the turn-on delay or "aperture time" of the AM1000 is primarily caused by the DH0034 translator. Maximum specified turn on time is 100 ns and turn off time is specified at 100 ns for the AM1000. Figure 6 shows absolute superiority of the AM1000 in switching ability for a given system accuracy.

AM1000 DRIVE CIRCUITS

Normally, analog switches will be selected by some digital control means which will usually mean 0V add +5V power supply levels. The AM1000 needs a driver capable of handling the full analog voltage swing, plus 10V. Therefore a circuit known as an analog switch translator is normally requried. There are several types available. All of the following circuits feature "break before make" action which is desirable for multiplexing.

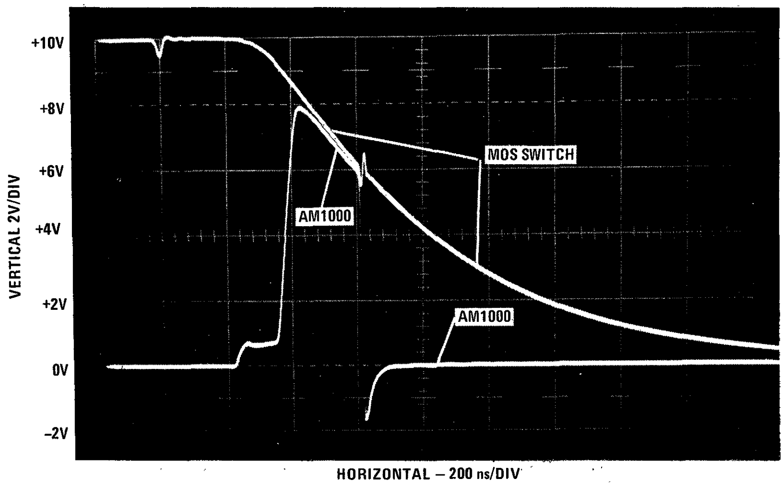

FIGURE 6A. AM1000 Sampling the Switching Transient of an MOS Analog Switch

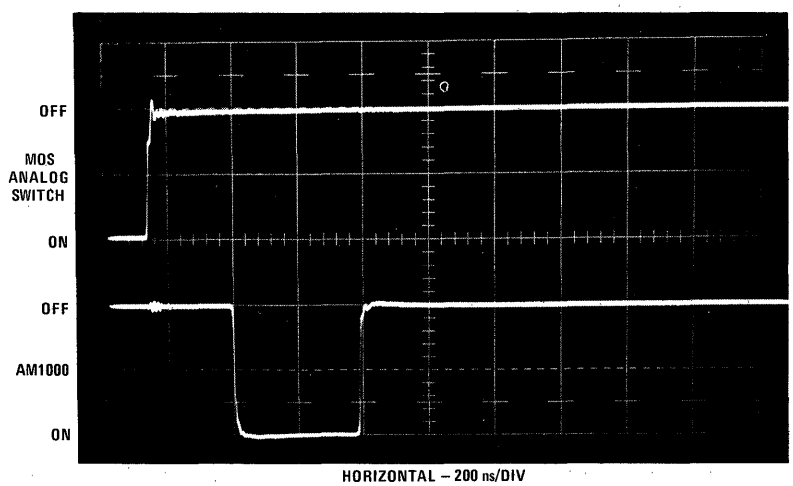

FIGURE 6B. Analog Switch Drive Timing

Analog switch translator-drivers fall into two basic categories. Those with pullups and those without. If the translator-driver has a pullup, such as the National DM7800, then a switching diode must be used to decouple the driver from the AM1000 when the driver goes positive.

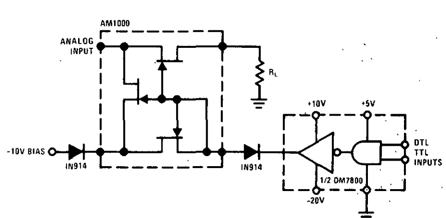

FIGURE 7. Translator-Driver with Voltage Pullup

The AM1000 does not require a driver with a pull-up. Figure 8 shows the circuit for this configuration. Note that the driver decoupling diode is not required. This configuration eliminates one power supply but adds the capacitance of the driver which the AM1000 must charge. Usually this additional capacitance is not excessive.

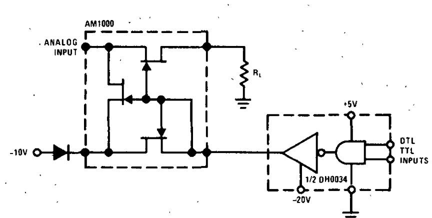

FIGURE 8. Translator-Driver without Pullup

In some systems, the cost of monolithic or hybrid drivers is not worth the space they save. Figure 9 shows a four channel driver using low cost discrete components. The ON channel is selected by binary coding and is DTL-TTL compatible. If A and B are "high" then drive is removed from Q_5 allowing channel 1 AM1001 to pull up and turn on. Q_6, Q_7 and Q_8 have drive applied which pull down on CH2, 3 and 4 thus turning them off. The voltages and devices indicated in Figure 9 allow ±15V analog signals to be handled.

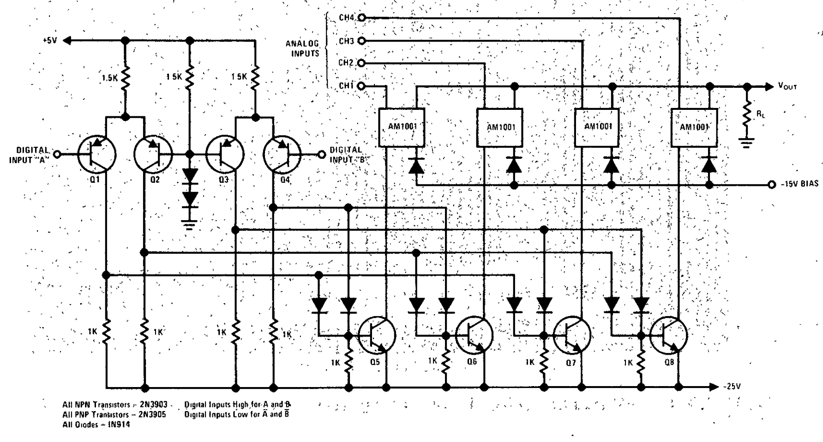

FIGURE 9. Binary Controlled Four Channel Multiplexer

CURRENT MODE MULTIPLEXING

So far, the discussion of multiplexing circuits has been confined to sampling various analog input voltages. Voltage mode analog switching allows maximum toggle rates but limited voltage range (±10V for AM1000, AM1002 and ±15V for AM1001).

If large analog voltages must be handled, current mode multiplexing must be used; toggle rate is reduced because accurate current-voltage converters are not as fast as non-inverting voltage amplifiers. Analog signal loading can also be a problem. Nevertheless current mode multiplexing allows sampling of very high analog voltages. This is accomplished by using scaling resistors and bound limit diodes at the input of the analog switch. Also, in this case the current to voltage converter should be the lowest impedance point in the system, so the AM1000 must be "turned around", so its analog "output" is used for the signal input and *vice versa.*

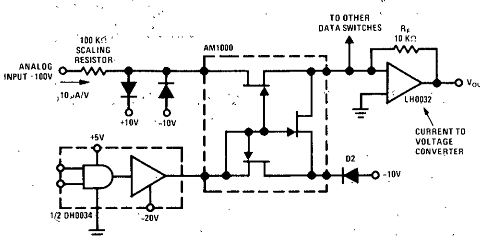

FIGURE 10. Current Mode Multiplexing

The system sensitivity in Figure 10 is determined by R_f in the current to voltage converter op amp. The LH0032 J-FET input op amp is selected because of its high slew rate and low input current. The 10 kΩ feedback resistor shown results in 10V output for 1 mA input. Thus the scaling resistor at the input is selected for 1 mA for 100V input, or 10 µA/V. A 1000V analog signal would use a 1 MΩ scaling resistor. For lower voltage signals, the R_{on} of the AM1000 would have to be considered for precision systems. The bound limit diodes connected to +10V and −10V prevents excessive voltage from appearing at the AM1000. Input impedance to the current to voltage converter is R_f divided by the open loop op amp gain (5000 for the LH0032); the input impedance would be 2Ω in Figure 10.

OTHER APPLICATIONS

Analog computer circuits can make good use of analog switches. A few examples are sample and hold circuits, reset stabilized circuits, integrator reset switches, and chopper stabilized amplifiers.[4]

Video signal switching can be done with a minimum of switching transients. More unusual applications such as double sideband suppressed carrier modulators can be constructed plus double sideband suppressed carrier demodulation and FM quadrature demodulators.[5]

CONCLUSION

Where precision, high speed analog switching is required, the AM1000 series of analog switches "rewrites the book."

Time domain multiplexing can be dramatically improved in channel capability and/or analog signal bandwidth capability. Sample and hold circuits can be improved, chopper stabilized amplifiers can be improved and virtually any other circuit which requires precision, high level, high speed analog switching can be improved.

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March 1969

INSTRUMENTATION AMPLIFIER

The differential input single-ended output instrumentation amplifier is one of the most versatile signal processing amplifiers available. It is used for precision amplification of differential dc or ac signals while rejecting large values of common mode noise. By using integrated circuits, a high level of performance is obtained at minimum cost.

Figure 1 shows a basic instrumentation amplifier which provides a 10 volt output for 100 mV input, while rejecting greater than ±11V of common mode noise. To obtain good input characteristics, two voltage followers buffer the input signal. The LM102 is specifically designed for voltage follower usage and has 10,000 MΩ input impedance with 3 nA input currents. This high of an input impedance provides two benefits: it allows the instrumentation amplifier to be used with high source resistances and still have low error; and it allows the source resistances to be unbalanced by over 10,000 ohms with no degradation in common mode rejection. The followers drive a balanced differential amplifier, as shown in Figure 1, which provides gain and rejects the common mode voltage. The gain is set by the ratio of R_4 to R_2 and R_5 to R_3. With the values shown, the gain for differential signals is 100.

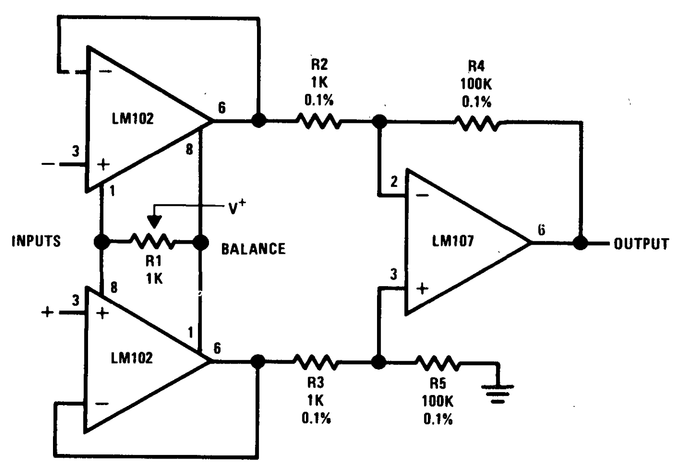


FIGURE 1. Differential-Input Instrumentation Amplifier

Figure 2 shows an instrumentation amplifier where the gain is linearly adjustable from 1 to 300 with a single resistor. An LM101A, connected as a fast inverter, is used as an attenuator in the feedback loop. By using an active attenuator, a very low impedance is always presented to the feedback resistors, and common mode rejection is unaffected by gain changes. The LM101A, used as shown, has a greater bandwidth than the LM107, and may be used in a feedback network without instability. The gain is linearly dependent on R_6 and is equal to $10^{-4} R_6$.

To obtain good common mode rejection ratios, it is necessary that the ratio of R_4 to R_2 match the ratio of R_5 to R_3. For example, if the resistors in circuit shown in Figure 1 had a total mismatch of 0.1%, the common mode rejection would be 60 dB times the closed loop gain, or 100 dB. The circuit shown in Figure 2 would have constant common mode rejection of 60 dB, independent of gain. In either circuit, it is possible to trim any one of the resistors to obtain common mode rejection ratios in excess of 100 dB.

For optimum performance, several items should be considered during construction. R_1 is used for zeroing the output. It should be a high resolution, mechanically stable potentiometer to avoid a zero shift from occurring with mechanical disturbances. Since there are several ICs operating in close proximity, the power supplies should be bypassed with .01 μF disc capacitors to insure stability. The resistors should be of the same type to have the same temperature coefficient.

A few applications for a differential instrumentation amplifier are: differential voltage measurements, bridge outputs, strain gauge outputs, or low level voltage measurement.

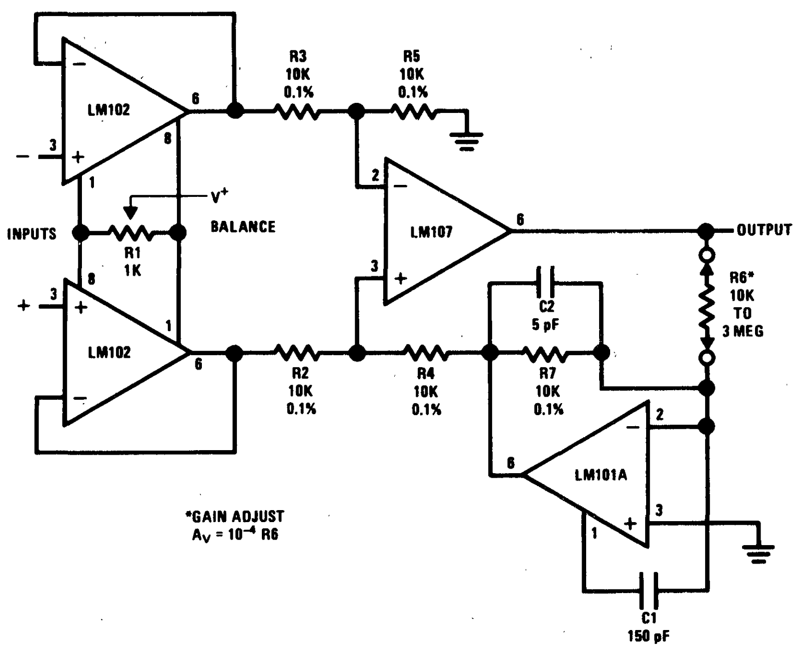


FIGURE 2. Variable Gain, Differential-Input Instrumentation Amplifier

March 1969

FEEDFORWARD COMPENSATION SPEEDS OP AMP

A feedforward compensation method increases the slew rate of the LM101A from 0.5/μs to 10V/μs as an inverting amplifier. This extends the usefulness of the device to frequencies an order of magnitude higher than the standard compensation network. With this speed improvement, IC op amps may be used in applications that previously required discretes. The compensation is relatively simple and does not change the offset voltage or current of the amplifier.

In order to achieve unconditional closed loop stability for all feedback connections, the gain of an operational amplifier is rolled off at 6 dB per octave, with the accompanying 90 degrees of phase shift, until a gain of unity is reached. The frequency compensation networks shape the open loop response to cross unity gain before the amplifier phase shift exceeds 180 degrees. Unity gain for the LM101A is designed to occur at 1 MHz. The reason for this is the lateral PNP transistors used for level shifting have poor high frequency response and exhibit excess phase shift about 1 MHz. Therefore, the stable closed loop bandwidth is limited to approximately 1 MHz.

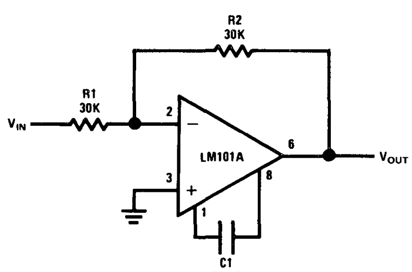


FIGURE 1. Standard Frequency Compensation

Usually, the LM101A is frequency compensated by a single 30 pF capacitor between Pins 1 and 8, as shown in Figure 1. This gives a slew rate of 0.5V/μs. The feedforward is achieved by connecting a 150 pF capacitor between the inverting input, Pin 2, and one of the compensation terminals, Pin 1, as shown in Figure 2. This eliminates the lateral PNP's from the signal path at high frequencies. Unity gain bandwidth is 10 MHz and the slew rate is 10V/μs. The diode can be added to improve slew with high speed input pulses.

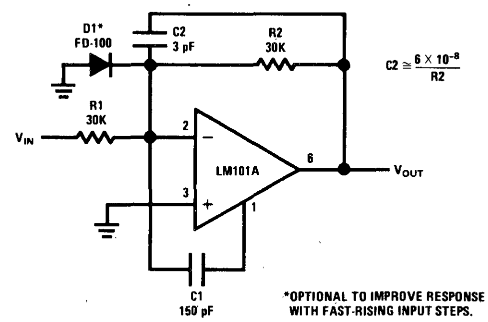


FIGURE 2. Feedforward Frequency Compensation

Figure 3 shows the open loop response in the high and low speed configuration. Higher open loop gain is realized with the fast compensation, as the gain rolls off at about 6 dB per octave until a gain of unity is reached at about 10 MHz. Figures 4 and 5 show the small signal and large signal transient response. There is a small amount of ringing; however, the amplifier is stable over a −55°C to +125°C temperature range. For comparison, large signal transient response with 30 pF frequency compensation is shown in Figure 6.

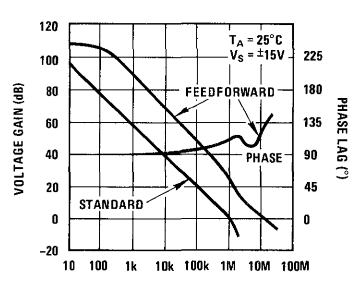


FIGURE 3. Open Loop Response for Both Frequency Compensation Networks

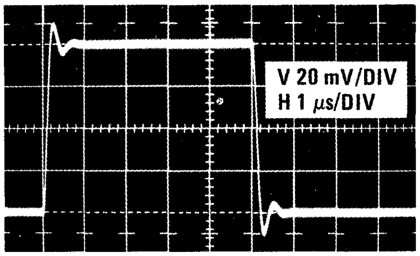


FIGURE 4. Small Signal Transient Response with Feedforward Compensation

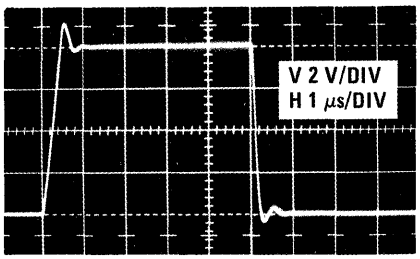


FIGURE 5. Large Signal Transient Response with Feedforward Compensation

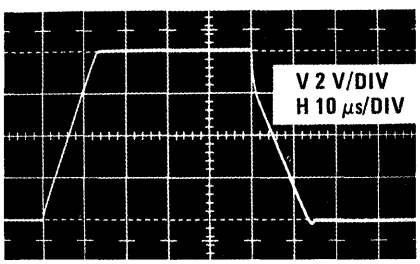


FIGURE 6. Large Signal Transient Response with Standard Compensation

As with all high frequency, high-gain amplifiers, certain precautions should be taken to insure stable operation. The power supplies should be bypassed near the amplifier with .01 µF disc capacitors. Stray capacitance, such as large lands on printed circuit boards, should be avoided at Pins 1, 2, 5, and 8. Load capacitance in excess of 75 pF should be decoupled, as shown in Figure 7; however, 500 pF of load capacitance can be tolerated without decoupling at the expense of bandwidth by the addition of 3 pF between Pins 1 and 8. A small capacitor C_2 is needed as a lead across the feedback resistor to insure that the rolloff is less than 12 dB per octave at unity gain. The capacitive reactance of C_2 should equal the feedback resistance between 2 and 3 MHz. For integrator applications, the lead capacitor is isolated from the feedback capacitor by a resistor, as shown in Figure 8.

Feedforward compensation offers a marked improvement over standard compensation. In addition to having higher bandwidth and slew, there is vanishingly small gain error from DC to 3 kHz, and less than 1% gain error up to 100 kHz as a unity gain inverter. The power bandwidth is also extended from 6 kHz to 250 kHz. Some applications for this type of amplifier are: fast summing amplifier, pulse amplifier, D/A and A/D systems, and fast integrator.

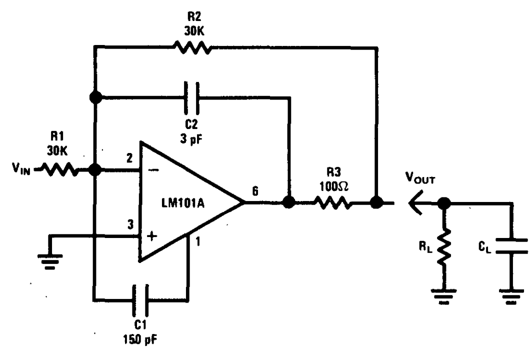


FIGURE 7. Capacitive Load Isolation

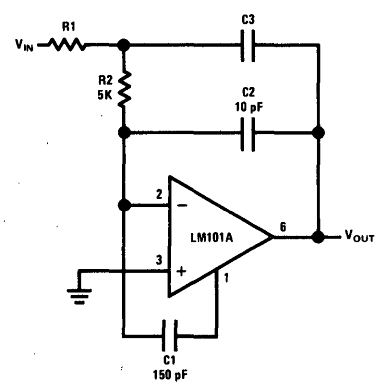


FIGURE 8. Fast Integrator

April 1969

WORST CASE POWER DISSIPATION IN LINEAR REGULATORS

The most frequent cause of failures of voltage regulators is excessive dissipation in the semiconductor components. Regulators using integrated circuits are no exception to this. In fact, IC regulators are more prone to overdissipation because they are not generally available in power packages, because complete integrated circuits must be operated at a lower, maximum junction temperature than silicon power transistors, and because the package must be able to dissipate the quiescent operating power of the control circuitry in addition to the power in the pass transistor.

The problems and solutions presented here give examples of the worst case calculations that should be used in designing voltage regulators with ICs. These questions were used in a contest sponsored by National Semiconductor. The entries received clearly showed that engineers have a marked tendency to be overly optimistic about the dissipation capability of the IC regulators as well as the power ratings of the external power transistors used with them. In a surprising number of cases the errors were of such a magnitude to cause almost certain, premature failure of the regulator under the conditions specified. The questions and answers follow:

1. What is the power limited full-load current for a 24V regulator using the LM100 (without a heat sink) when the worst case operating conditions are 125°C ambient and 40V input voltage?

   The maximum chip temperature of the LM100 is 150°C, and the thermal resistance of the TO-5 package is 150°C/W when no heat sink is used. The permissable, junction-to-ambient temperature rise is 25°C with a 125°C ambient, so the maximum allowable package dissipation is 167 mW.

   The worst case quiescent current of the LM100 is 3.0 mA. With a 40V input voltage, this produces an internal dissipation of 120 mW, even with no load. Therefore, the device can only dissipate another 47 mW in supplying the load current. With 40V in and 24V out, the input-output voltage differential is 16V. This means that 2.95 mA can be supplied through the internal pass transistor without exceeding the ratings.

   The divider resistors required on the LM100 feedback to give a 24V output are 26.6k and 2.1k. For a 1.8V sense voltage on the feedback terminal, the divider current will be 0.85 mA. Since this current must be supplied by the integrated circuit, it must be subtracted from the available load current. Hence the maximum output current, taking into account worse case conditions, is *2.1 mA*.

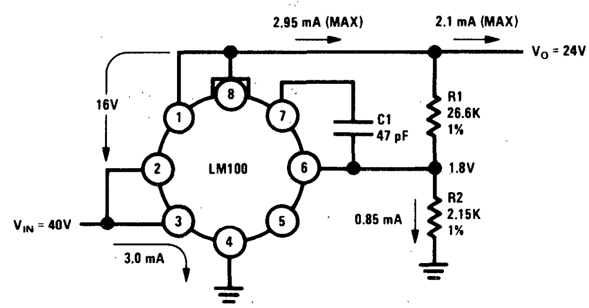


FIGURE 1. Circuit Used in the Solution of Question 1.

2. What is the maximum allowable short-circuit current for an LM104 regulator circuit, with a 2N2905A series pass transistor (without a heat sink) when the worst case input is 20V at an ambient of 85°C?

   The 2N2905A, without a heat sink, can dissipate a maximum of 0.6W at 25°C. However, this must be derated by 3.42 mW/°C for operation at higher temperatures. Since an 85°C ambient is 60°C higher than the temperature at which the transistors are specified, the maximum power rating must be reduced by 205 mW, to 395 mW. With a shorted output, the voltage dropped across the current limit sense resistor is 0.5V, so the voltage across the external pass transistor will be 19.5V for 20V input. This means that the 395 mW maximum dissipation rating will be exceeded for short-circuit currents greater than *20.2 mA*.

3. In the previous example, what is the maximum current when the case temperature of the 2N2905A is held to 100°C?

The maximum dissipation of the 2N2905A is 3W at 25°C case temperature, but this must be derated by 17.2 mW/°C for higher case temperatures. With a 100°C case temperature, the allowable dissipation is reduced by 1.29W to 1.71W.

As in the previous example, the voltage across the pass transistor will be 19.5V. This gives a dissipation-limited short-circuit current of *88 mA*.

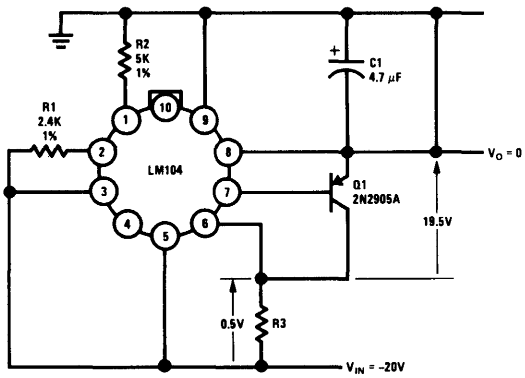


FIGURE 2. Circuit Used in the Solution of Questions 2 and 3.

4. In the negative regulator with foldback current limiting, what will be the worst case dissipation in the PNP driver, Q_1, with full load and a 24V input voltage?

   The 2N3772 is specified to have a minimum current gain of 15 at 10A and 25°C. It would be reasonable to assume a minimum current gain of 15 at 5A for elevated temperatures where dissipation is most significant. This means that the base current for a 5A load current will be 0.33A. The worst case emitter-base voltage of the 2N3772 at 5A will be about 1V, so the current through the 68Ω emitter-base resistor will be 15 mA. Hence, the PNP driver must supply a total current of 345 mA.

   The voltage dropped across the PNP driver will be the 12V input output voltage differential, less the 1V dropped across the current sense resistor and the 1V dropped across the emitter-base junction of the 2N3772. Therefore, the PNP driver operates with 10V across it and dissipates about *3.5W*.

5. Could a 2N2905A be used in the example above if the maximum ambient were 85°C?

   Even with an infinite heat sink, the 2N2905A can dissipate only 2W at 85°C. *Therefore, it cannot be used.*

The answers to these questions show that the maximum output current of a regulator can be substantially less than might be expected from a cursory analysis of the circuit. Detailed analysis under worst case conditions is necessary to insure a reliable design. These calculations are more important than most other design calculations because errors do not result in somewhat degraded performance that usually shows up in checking out the equipment. Instead, these errors cause failures that do not always show up during checkout, but can occur in field operation.

Additional information on the design of reliable voltage regulators is given in application notes AN-21 and AN-23, available from National Semiconductor.

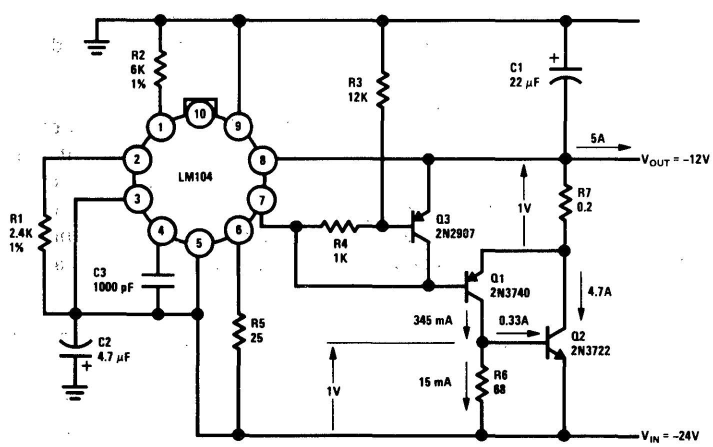


FIGURE 3. Circuit Used in the Solution of Questions 4 and 5.

April 1969

FAST COMPENSATION EXTENDS POWER BANDWIDTH

In all IC operational amplifiers the power bandwidth depends on the frequency compensation. Normally, compensation for unity gain operation is accompanied by the lowest power bandwidth. A technique is presented which extends the power bandwidth of the LM101A for non-inverting gains of unity to ten, and also reduces the gain error at moderate frequencies.

In order to achieve unconditional stability, an operational amplifier is rolled off at 6 dB per octave, with an accompanying 90 degrees of phase shift, until a gain of unity is reached. Unity gain in most monolithic operational amplifiers is limited to 1 MHz, because the lateral PNP's used for level shifting have poor frequency response and exhibit excess phase shift at frequencies above 1 MHz. Hence, for stable operation, the closed loop bandwidth must be less than 1 MHz where the phase shift remains below 180 degrees.

For high closed loop gains, less severe frequency compensation is necessary to roll the open loop gain off at 6 dB per octave until it crosses the closed loop gain. The frequency where it crosses must, as previously mentioned, be less than 1 MHz. For closed loop gains between 1 and 10, more frequency compensation must be used to insure that the open loop gain has been rolled off soon enough to cross the closed loop gain before 1 MHz is reached.

The power bandwidth of an operational amplifier depends on the current available to charge the frequency compensation capacitors. For unity gain operation, where the compensation capacitor is largest, the power bandwidth of the LM101A is 6 kHz. Figure 1 shows an LM101A with unity gain

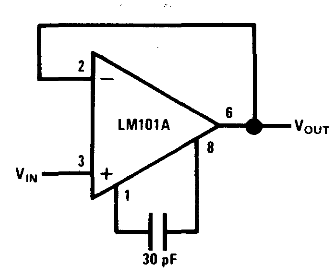


FIGURE 1. LM101A With Standard Frequency Compensation.

compensation and Figure 3 shows the open loop gain as a function of frequency.

A two-pole frequency compensation network, as shown in Figure 2, provides more than a factor of

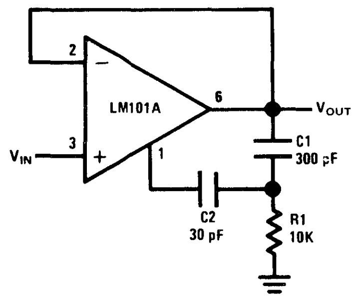


FIGURE 2. LM101A with Frequency Compensation to Extend Power Bandwidth.

two improvement in power bandwidth and reduced gain error at moderate frequencies. The network consists of a 30 pF capacitor, which sets the unity gain frequency at 1 MHz, along with a 300 pF capacitor and a 10k resistor. By dividing the ac output voltage with the 10k resistor and 300 pF capacitor, there is less ac voltage across the 30 pF capacitor and less current is needed for charging. Since the voltage division is frequency sensitive, the open loop gain rolls off at 12 dB per octave until a gain of 20 is reached at 50 kHz. From 50 kHz to 1 MHz the 10k resistor is larger than the impedance of the 300 pF capacitor and the gain rolls off at 6 dB per octave. The open loop gain plot is shown in Figure 3. To insure sufficient drive to the 300 pF capacitor, it is connected to the output, Pin 6, rather than Pin 8. With this frequency compensation method, the power bandwidth is typically 15–20 kHz as a follower, or unity gain inverter.

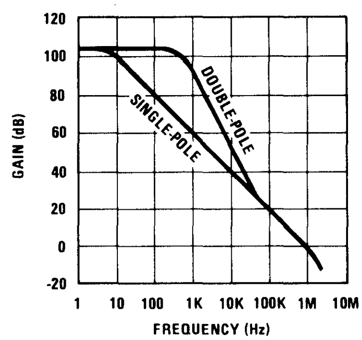


FIGURE 3. Open Loop Response for Both Frequency Compensation Networks.

This frequency compensation, in addition to extending the power bandwidth, provides an order of magnitude lower gain error at frequencies from DC to 5 kHz. Some applications where it would be helpful to use the compensation are: differential amplifiers, audio amplifiers, oscillators, and active filters.

March 1969

HIGH Q NOTCH FILTER

The twin "T" network is one of the few RC filter networks capable of providing an infinitely deep notch. By combining the twin "T" with an LM102 voltage follower, the usual drawbacks of the network are overcome. The Q is raised from the usual 0.3 to something greater than 50. Further, the voltage follower acts as a buffer, providing a low output resistance; and the high input resistance of the LM102 makes it possible to use large resistance values in the "T" so that only small capacitors are required, even at low frequencies. The fast response of the follower allows the notch to be used at high frequencies. Neither the depth of the notch nor the frequency of the notch are changed when the follower is added.

Figure 1 shows a twin "T" network connected to an LM102 to form a high Q, 60 Hz notch filter.

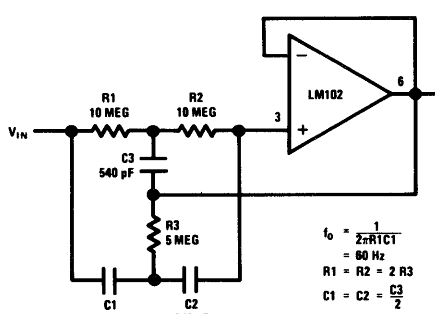


FIGURE 1. High Q Notch Filter

The junction of R_3 and C_3, which is normally connected to ground, is bootstrapped to the output of the follower. Because the output of the follower is a very low impedance, neither the depth nor the frequency of the notch change; however, the Q is raised in proportion to the amount of signal fed back to R_3 and C_3. Figure 2 shows the response of a normal twin "T" and the response with the follower added.

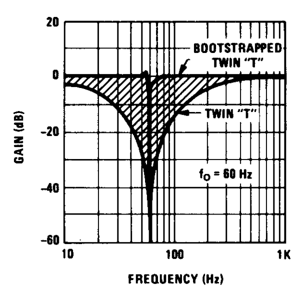


FIGURE 2. Response of High and Low Q Notch Filter

In applications where the rejected signal might deviate slightly from the null of the notch network, it is advantageous to lower the Q of the network. This insures some rejection over a wider range of input frequencies. Figure 3 shows a circuit where the Q may be varied from 0.3 to 50. A fraction of the output is fed back to R_3 and C_3 by a second voltage follower, and the notch Q is dependent on the amount of signal fed back. A second follower is necessary to drive the twin "T" from a low-resistance source so that the notch frequency and depth will not change with the potentiometer setting. Depending on the potentiometer setting, the circuit in Figure 3 will have a response that falls in the shaded area of Figure 2.

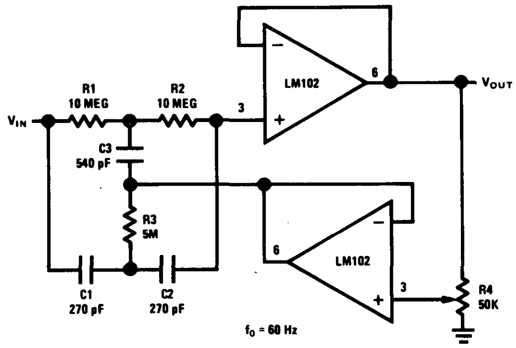


FIGURE 3. Adjustable Q Notch Filter

An interesting change in the high Q twin "T" occurs when components are not exactly matched in ratio. For example, an increase of 1 to 10 percent in the value of C_3 will raise the Q, while degrading the depth of the notch. If the value of C_3 is raised by 10 to 20 percent, the network provides voltage gain and acts as a tuned amplifier. A voltage gain of 400 was obtained during testing. Further increases in C_3 cause the circuit to oscillate, giving a clipped sine wave output.

The circuit is easy to use and only a few items need be considered for proper operation. To minimize notch frequency shift with temperature, silver mica, or polycarbonate, capacitors should be used with precision resistors. Notch depth depends on component match, therefore, 0.1 percent resistors and 1 percent capacitors are suggested to minimize the trimming needed for a 60 dB notch. To insure stability of the LM102, the power supplies should be bypassed near the integrated circuit package with .01 μF disc capacitors.

May 1969

FAST VOLTAGE COMPARATORS WITH LOW INPUT CURRENT

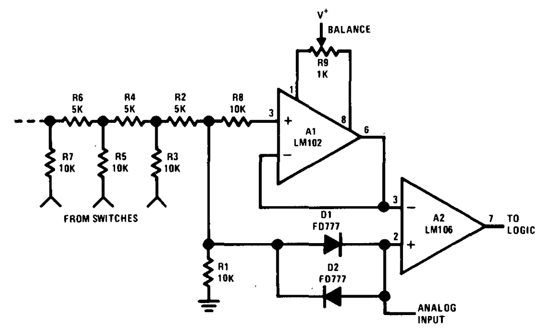
Monolithic voltage comparators are available today which are both fast and accurate. They can detect the height of a pulse with a 5 mV accuracy within 40 ns. However, these devices have relatively high input currents and low input impedances, which reduces their accuracy and speed when operating from high source resistances. This is probably a basic limitation since the input transistors of the integrated circuit must be operated at a relatively high current to get fast operation. Further, the circuit must be gold doped to reduce storage time, and this limits the current gain that can be obtained in the transistors. High gain transistors operating at low collector currents are necessary to get good input characteristics.

One way of overcoming this difficulty is to buffer the input of the comparator. A voltage follower is available which is ideally suited for this job. This device, the LM102*, is both fast and has a low input current. It can reduce the effective input current of the comparator by more than three orders of magnitude without greatly reducing speed.

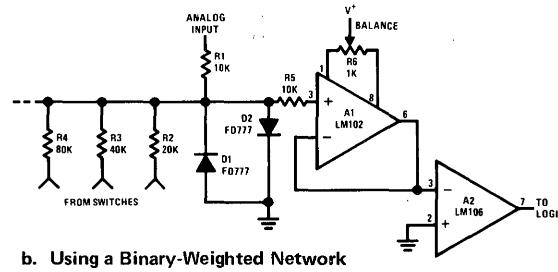
A comparator circuit for an A/D converter which uses this technique is shown in Figure 1a. An LM102 voltage follower buffers the output of a ladder network and drives one input of the comparator. The analog signal is fed to the other input of the comparator. It should come from a low impedance source such as the output of a signal processing amplifier, or another LM102 buffer amplifier.

Clamp diodes, D_1 and D_2, are included to make the circuit faster. These diodes clamp the output of the ladder so that it is never more than 0.7V different from the analog input. This reduces the voltage excursion that the buffer must handle on the most significant bit and keeps it from slewing. If fast, low-capacitance diodes are used, the signal to the comparator will stabilize approximately 200 ns after the most significant bit is switched in. This is about the same as the stabilization time of the ladder network alone, as its speed is limited by stray capacitances. The diodes also limit the voltage swing across the inputs of the comparator, increasing its operating speed and insuring that the device is not damaged by excessive differential input voltage.

The buffer reduces the loading on the ladder from 45 μA to 20 nA, maximum, over a -55°C to 125°C temperature range. Hence, in most applications the input current of the buffer is totally insignificant. This low current will often permit



a. Using a Ladder Network



b. Using a Binary-Weighted Network

FIGURE 1. Comparator Circuits for Fast A/D Converters

the use of larger resistances in the ladder which simplifies design of the switches driving it.

It is possible to balance out the offset of the LM102 with an external 1 kΩ potentiometer, R_9. The adjustment range of this balance control is large enough so that it can be used to null out the offset of both the buffer and the comparator. A 10 kΩ resistor should be installed in series with the input to the LM102, as shown. This is required to make the short circuit protection of the device effective and to insure that it will not oscillate. This resistor should be located close to the integrated circuit.

A similar technique can be used with A/D converters employing a binary-weighted resistor network. This is shown in Figure 1b. The analog input is fed into a scaling resistor, R_1. This resistor is selected so that the input voltage to the LM102 is zero when the output of the D/A network corresponds to the analog input voltage. Hence, if the D/A output is too low, the output of the LM106 will be a logical zero; and the output will change to a logical one as the D/A output exceeds the analog signal.

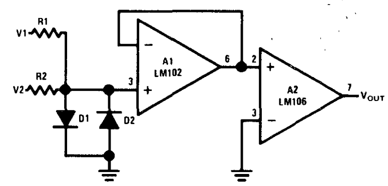
The analog signal must be obtained from a source impedance which is low by comparison to R_1. This can be either another LM102 buffer or the output of the signal-processing amplifier. Clamp diodes, D_1 and D_2, restrict the signal swing and speed up the circuit. They also limit the input signal seen by the LM106 to protect if from overloads. Operating speed can be increased even further by using silicon backward diodes (a degenerate tunnel diode) in place of the diodes shown, as they will clamp the signal swing to about 50 mV. The offset voltage of both the LM102 and the LM106 can be balanced out, if necessary, with R_6.

The binary weighted network can be driven with single pole, single-throw switches. This will result in a change in the output resistance of the network when it switches, but circuit performance will not be affected because the input current of the LM102 is negligible. Hence, using the LM102 greatly simplifies switch design.

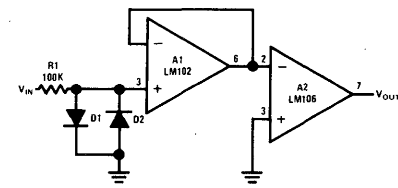
Although it is possible to use a 710 as the voltage comparator in these circuits, the LM106 offers several advantages. First, it can drive a fan out of 10 with standard, integrated DTL or TTL. It also has two strobe terminals available which disable the comparator and give a high output when either of the terminals is held at a logical zero. This adds logic capability to the comparator in that it makes it equivalent to a 710 and a two-input NAND gate. If not needed, the strobe pins can be left unconnected without affecting performance. The voltage gain of the LM106 is about 45,000, which is 30 times higher than that of the 710. The increased gain reduces the error band in making a comparison. The LM106 will also operate from the same supply voltage as the LM102, and other operational amplifiers, for ±12V supplies. However, it can also be operated from ±15V supplies if a 3V zener diode is connected in series with the positive supply lead.

It is necessary to observe a few precautions when working with fast circuits operating from relatively high impedances. A good ground is necessary, and a ground plane is advisable. All the individual points in the circuit which are to be grounded, including bypass capacitors, should be returned separately to the same point on the ground so that voltages will not be developed across common lead inductance. The power supply leads of the integrated circuits should also be bypassed with low inductance 0.01 μF capacitors. These capacitors, preferably disc ceramic, should be installed with short leads and located close to the devices. Lastly, the output of the comparator should be shielded from the circuitry on the input of the buffer, as stray coupling can also cause oscillation.

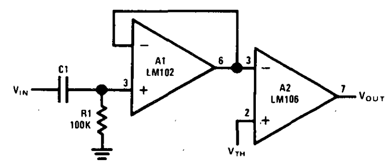
Although the circuits shown so far were designed for use in A/D converters, the same techniques apply to a number of other applications. Figure 2 gives examples of circuits which can put stringent input current requirements on the comparator. The first is a comparator for signals of opposite



a. Comparator for Signals of Opposite Polarity



b. Zero Crossing Detector



c. Comparator for AC Coupled Signals

FIGURE 2. Applications Requiring Low Input Current Comparators

polarity. Resistors (R_1 and R_2) are required to isolate the two signal sources. Frequently, these resistors must be relatively large so that the signal sources are not loaded. Hence, the input current of the comparator must be reduced to prevent inaccuracies. Another example is the zero-crossing detector in Figure 2b. When the input signal can exceed the common mode range of the comparator (±5V for the LM106), clamp diodes must be used. It is then necessary to isolate the comparator from the input with a relatively large resistance to prevent loading. Again, bias currents should be reduced. A third example, in Figure 2c, is a comparator with an ac coupled input. An LM106 will draw an input current which is twice the specified bias current when the signal is above the comparison threshold. Yet, it draws no current when the signal is below the threshold. This asymmetrical current drain will charge any coupling capacitor on the input and produce an error. This problem can be eliminated by using a buffer, as the input current will be both low and constant.

The foregoing has shown how two integrated circuits can be combined to provide state-of-the-art performance in both speed and input current. Equivalent results will probably not be achievable in a single circuit for some time, as the technologies required are not particularly compatible. Further, considering the low cost of monolithic circuits, approaches like this are certainly economical.

August 1969

TRACKING VOLTAGE REGULATORS

Integrated circuit voltage regulators are available today which are economical and offer a high degree of performance. There are both positive and negative regulators capable of achieving better than 0.1% regulation under normal fluctuations in input supply and load. Due to production variations, the internal reference voltage in these regulators may vary as much as 10% from unit to unit. Normally, this causes no problems as most power supply circuits have an adjustment potentiometer which is varied to obtain the correct output voltage. In systems with more than one regulated output voltage, it is sometimes desirable to adjust all supplies with a single potentiometer. This results in savings by eliminating one or more potentiometers as well as eliminating the need to adjust the supplies individually.

Figure 1 shows a 5V and a 15V regulator with both outputs adjusted with a single potentiometer. Although the technique is not exact, the error is typically under 2%. As shown in Figure 1, the internal reference voltages for the LM105* regulators, available at pin 5, are tied together. This insures that both regulators operate with the same reference voltage. The lower resistors of the output divider, R_2, are connected through a common adjustment potentiometer to ground. R_5 adjusts both regulators for variations in the 1.8V reference. Note that the wiper of R_5 is connected to one side of the potentiometer. If a rheostat connection were used, the arm might open circuit during adjustment, causing large transients on the output.

The calculations of resistor values for the output divider resistors are made with the consideration that the adjustment is not exact and that two regulators are adjusted. The bottom resistor of the divider, R_2, is fixed at 2K. The top of the divider, R_1, is then calculated for the output voltage using 1.6V as the reference voltage. To help compensate for the inaccuracies in the adjustment, output voltages are calculated slightly off from the desired values. For the 5 and 15V regulators, R_1 is calculated to give a 2% low output voltage on the 5V regulator and a 2% high output voltage on the 15V regulator.

$$R_1 = \frac{(V_{OUT} - 1.6V)\, 2000\Omega}{1.6V}$$

R_5 will now adjust both regulators to within 2% of the desired output for reference variations from 1.6V to 2.0V. From the previous calculations, a 1.6V reference yields outputs of 4.9V and 15.3V. If the reference is 2.0V, R_5 is adjusted to 324 ohms and the output voltages are 5.1V and 14.9V. If the reference is near the typical value of 1.8V, both outputs are within 1% of nominal.

These calculations do not account for resistor inaccuracies. If 1% resistors are used there is an additional worst case error of 2% for each regulator. Resistor errors are inherent in any type of tracking regulator system, even if the adjustment is theoretically exact.

Actually, any number of regulators may be connected to a single adjustment resistor. The adjustment accuracy of this technique depends on the output voltage differences among the regulators. The previous example was a severe difference, and had only 2% accuracy. With close output voltages, such as 12V and 15V, the error is much smaller. The 12V regulator is calculated to 1/2% low and 15V regulator 1/2% high with the 1.6V reference. Both regulators are then within 1/2% for reference variations of 1.6 to 2.0 volts. This adjustment method is, of course, exact if two regulators have the same output.

*R. J. Widlar, "The LM105—An Improved Positive Regulator," National Semiconductor Corporation, AN 23, January, 1969.

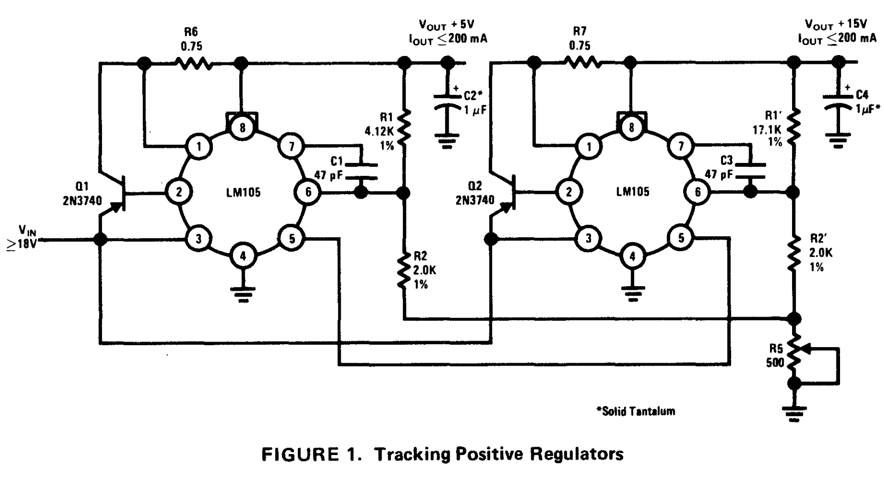


FIGURE 1. Tracking Positive Regulators

Using a negative regulator to track a positive regulator is a somewhat easier task. An inverting operational amplifier may be used to provide a negative output voltage while using a positive voltage as a reference. The LM104† negative regulator is easily adapted for use as an inverting amplifier and provides several advantages over conventional operational amplifiers. It is designed to drive boost transistors for higher output current as well as providing a convenient method of current limiting the output. Further, the frequency compensation used on the LM104 is optimized for transient response to line and load changes. Figure 2 shows tracking ±15V regulators.

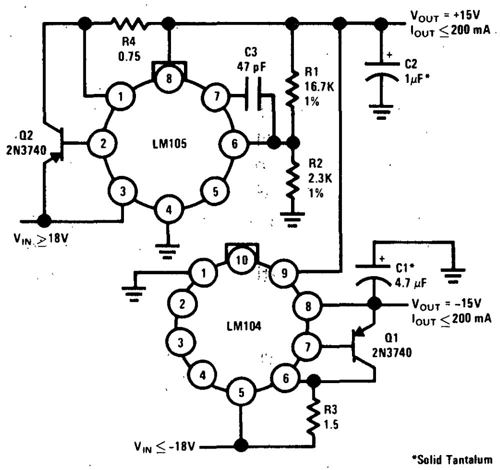


FIGURE 2. Tracking Positive and Negative Regulators

Operation is most easily understood by referring to the functional schematic of the LM104 in Figure 3. The non-inverting input of the internal amplifier, pin 1, is connected to ground. The positive 15V reference is connected through an internal 15K ohm input resistor, R_{16}, to the inverting input. Feedback resistor, R_{15}, is also 15K ohm. This forms a unity gain inverting amplifier with a negative output voltage equal to the positive input voltage. The 15K ohm resistors in the LM104 are typically matched to 1%. This means that the output of both regulators may be adjusted with 1% accuracy by changing R_1 in Figure 2.

†R. J. Widlar, "Designs for Negative Regulators," National Semiconductor Corporation, AN-21, December, 1968.

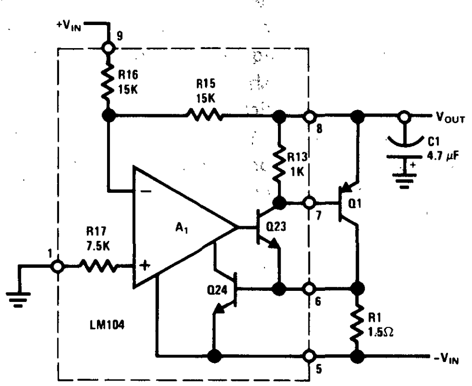


FIGURE 3. Functional Diagram of the LM104 Used as an Amplifier

The LM104 may also be used with inverting gain for negative output voltages greater than the positive reference voltage. Figure 4 shows a circuit where the −15V supply tracks a +5V supply. In this configuration the non-inverting input is not grounded, but tied to divider, R_5, R_6, between the negative output and ground. The output voltage equals

$$V_{OUT} = V^+ \left[\frac{R_5 + R_6}{R_6 - R_5}\right]$$

where V^+ is the positive reference.

The line regulation and temperature drift are determined primarily by the positive reference, with the negative output tracking. The reference must be a low impedance source, such as an LM105 regulator, to insure that current drawn by pin 9 of the LM104 does not affect the reference voltage. Since the LM104 is connected to a positive voltage instead of ground, it sees a total voltage equal to the sum of the unregulated negative input and the positive reference voltage. This reduces the maximum unregulated negative input voltage allowable, and should be considered during design. If the negative output voltage must be less than the positive reference or the decrease in maximum unregulated input voltage cannot be tolerated, an alternate method of constructing tracking regulators is given elsewhere†. Of course, many negative regulators may be slaved to a single positive regulator.

Using standard linear integrated circuits, multiple output positive and negative supplies may be adjusted to within 2% or less by a single resistor. Although the absolute output is not exact, the regulation accuracy is still within 0.1%. These techniques can result in savings by the elimination of both time and materials when used.

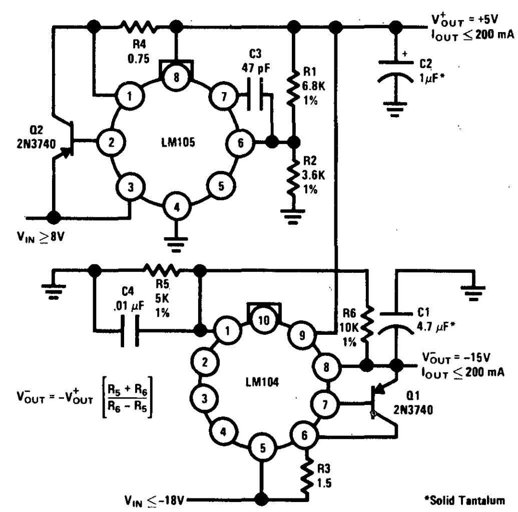


FIGURE 4. Tracking Regulators With Different Output Voltages

August 1969

PRECISION AC/DC CONVERTERS

Although semiconductor diodes available today are close to "ideal" devices, they have severe limitations in low level applications. Silicon diodes have a 0.6V threshold which must be overcome before appreciable conduction occurs. By placing the diode in the feedback loop of an operational amplifier, the threshold voltage is divided by the open loop gain of the amplifier. With the threshold virtually eliminated, it is possible to rectify millivolt signals.

Figure 1 shows the simplest configuration for eliminating diode threshold potential. If the voltage at the non-inverting input of the amplifier is positive,

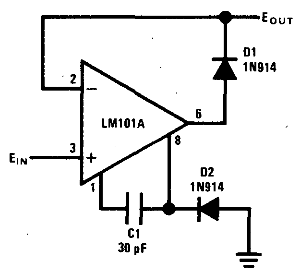


FIGURE 1. Precision Diode

the output of the LM101A swings positive. When the amplifier output swings 0.6V positive, D_1 becomes forward biased; and negative feedback through D_1 forces the inverting input to follow the non-inverting input. Therefore, the circuit acts as a voltage follower for positive signals. When the input swings negative, the output swings negative and D_1 is cut off. With D_1 cut off no current flows in the load except the 30 nA bias current of the LM101A. The conduction threshold is very small since less than 100 μV change at the input will cause the output of the LM101A to swing from negative to positive.

A useful variation of this circuit is a precision clamp, as is shown in Figure 2. In this circuit the output is precisely clamped from going more positive than the reference voltage. When E_{IN} is more positive than E_{REF}, the LM101A functions as a summing amplifier with the feedback loop closed through D_1. Neglecting offsets, negative feedback keeps the summing node, and therefore the output, within 100 μV of the voltage at the non-inverting input. When E_{IN} is about 100 μV more negative than E_{REF}, the output swings positive, reverse biasing D_1. Since D_1 now prevents negative feedback from controlling the voltage at the inverting input, no clamping action is obtained. On both of the circuits in Figures 1 and 2 an output clamp diode is added at pin 8 to help speed response. The clamp prevents the operational amplifier from saturating when D_1 is reverse biased.

When D_1 is reverse biased in either circuit, a large differential voltage may appear between the inputs of the LM101A. This is necessary for proper operation and does no damage since the LM101A is designed to withstand large input voltages. These circuits will not work with amplifiers protected with back to back diodes across the inputs. Diode protection conducts when the differential input voltage exceeds 0.6V and would connect the input and output together. Also, unprotected devices such as the LM709, are damaged by large differential input signals.

The circuits in Figures 1 and 2 are relatively slow. Since there is 100% feedback for positive input signals, it is necessary to use unity gain frequency compensation. Also, when D_1 is reverse biased, the feedback loop around the amplifier is opened and the input stage saturates. Both of these conditions cause errors to appear when the input frequency exceeds 1.5 kHz. A higher performance precision half wave rectifier is shown in Figure 3. This circuit will provide rectification with 1% accuracy at frequencies from dc to 100 kHz. Further, it is easy to extend the operation to full wave rectification for precision ac/dc converters.

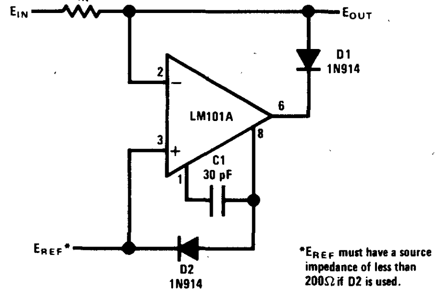


FIGURE 2. Precision Clamp

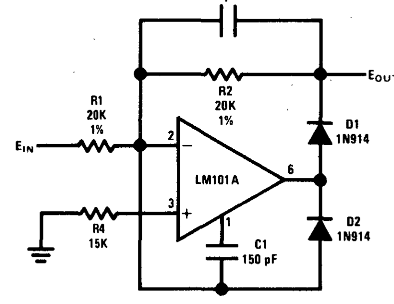


FIGURE 3. Fast Half Wave Rectifier

This precision rectifier functions somewhat differently from the circuit in Figure 1. The input signal is applied through R_1 to the summing node of an inverting operational amplifier. When the signal is negative, D_1 is forward biased and develops an output signal across R_2. As with any inverting amplifier, the gain is R_2/R_1. When the signal goes positive, D_1 is non-conducting and there is no output. However, a negative feedback path is provided by D_2. The path through D_2 reduces the negative output swing to −0.7V, and prevents the amplifier from saturating.

Since the LM101A is used as an inverting amplifier, feedforward* compensation can be used. Feedforward compensation increases the slew rate to 10V/µs and reduces the gain error at high frequencies. This compensation allows the half wave rectifier to operate at higher frequencies than the previous circuits with no loss in accuracy.

The addition of a second amplifier converts the half wave rectifier to a full wave rectifier. As is shown in Figure 4, the half wave rectifier is connected to inverting amplifier A_2. A_2 sums the half wave rectified signal and the input signal to provide a full wave output. For negative input signals the output of A_1 is zero and no current flows through R_3. Neglecting for the moment C_2, the output of A_2 is $-\frac{R_7}{R_6} E_{IN}$. For positive input signals, A_2 sums the currents through R_3 and R_6; and

$$E_{OUT} = R_7 \left[\frac{E_{IN}}{R_3} - \frac{E_{IN}}{R_6}\right].$$

If R_3 is 1/2 R_6, the output is $\frac{R_7}{R_6} E_{IN}$. Hence, the output is always the absolute value of the input.

Filtering, or averaging, to obtain a pure dc output is very easy to do. A capacitor, C_2, placed across R_7 rolls off the frequency response of A_2 to give an output equal to the average value of the input. The filter time constant is R_7C_2, and must be much greater than the maximum period of the input signal. For the values given in Figure 4, the time constant is about 2.0 seconds. This converter has better than 1% conversion accuracy to above 100 kHz and less than 1% ripple at 20 Hz. The output is calibrated to read the rms value of a sine wave input.

As with any high frequency circuit some care must be, taken during construction. Leads should be kept short to avoid stray capacitance and power supplies bypassed with .01 µF disc ceramic capacitors. Capacitive loading of the fast rectifier circuits must be less than 100 pF or decoupling becomes necessary. The diodes should be reasonably fast and film type resistors used. Also, the amplifiers must have low bias currents.

*R. C. Dobkin, "Feedforward Compensation Speeds Op Amp," *National Semiconductor Corporation, LB-2*, April, 1969.

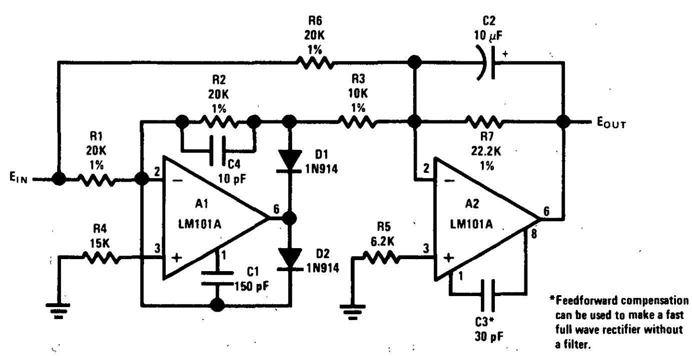


FIGURE 4. Precision AC to DC Converter

August 1969

UNIVERSAL BALANCING TECHNIQUES

IC op amps are widely accepted as a universal analog component. Although the circuit designs may vary, most devices are functionally interchangeable. However, offset voltage balancing remains a personality trait of the particular amplifier design. The techniques shown here allow offset voltage balancing without regard to the internal circuitry of the amplifier.

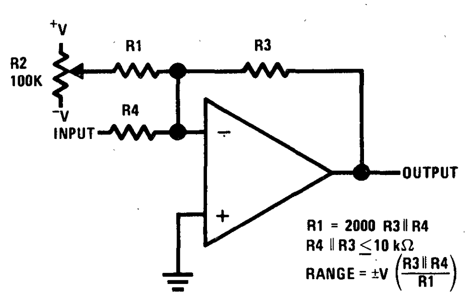


FIGURE 1. Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less

The circuit shown in Figure 1 is used to balance out the offset voltage of inverting amplifiers having a source resistance of 10 kΩ or less. A small current is injected into the summing node of the amplifier through R_1. Since R_1 is 2000 times as large as the source resistance the voltage at the arm of the pot is attenuated by a factor of 2000 at the summing node. With the values given and ±15V supplies the output may be zeroed for offset voltages up to ±7.5 mV.

If the value of the source resistance is much larger than 10 kΩ, the resistance needed for R_1 becomes too large. In this case it is much easier to balance out the offset by supplying a small voltage at the non-inverting input of the amplifier. Figure 2 shows such a scheme. Resistors R_1 and R_2 divide the voltage at the arm of the pot to supply a ±7.5 mV adjustment range with ±15V supplies. This adjustment method is also useful when the feedback element is a capacitor or non-linear device.

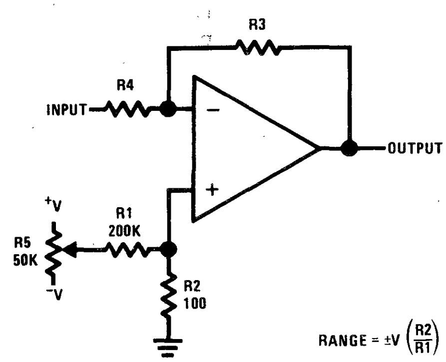


FIGURE 2. Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element

This technique of supplying a small voltage effectively in series with the input is also used for adjusting non-inverting amplifiers. As is shown in Figure 3, divider R_1, R_2 reduces the voltage at the arm of the pot to ±7.5 mV for offset adjustment. Since R_2 appears in series with R_4, R_2 should be considered when calculating the gain. If R_4 is greater than 10 kΩ the error due to R_2 is less than 1%.

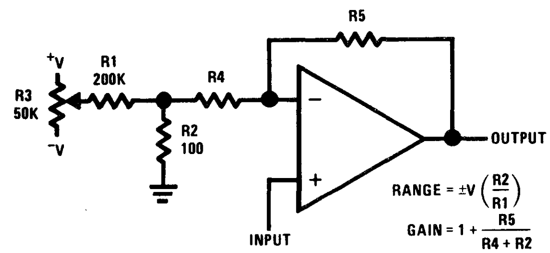


FIGURE 3. Offset Voltage Adjustment for Non-Inverting Amplifiers

A voltage follower may be balanced by the technique shown in Figure 4. R_1 injects a current which produces a voltage drop across R_3 to cancel the offset voltage. The addition of the adjustment resistors causes a gain error, increasing the gain by 0.05%. This small error usually causes no problem. The adjustment circuit essentially causes the offset voltage to appear at full output, rather than at low output levels, where it is a large percentage error.

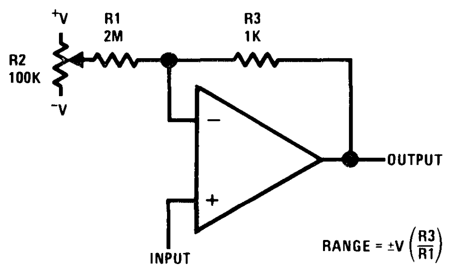


FIGURE 4. Offset Voltage Adjustment for Voltage Followers

Differential amplifiers are somewhat more difficult to balance. The offset adjustment used for a differential amplifier can degrade the common mode rejection ratio. Figure 5 shows an adjustment circuit which has minimal effect on the common mode rejection. The voltage at the arm of the pot is divided by R_4 and R_5 to supply an offset correction of ±7.5 mV. R_4 and R_5 are chosen such that the common mode rejection ratio is limited by the amplifier for values of R_3 greater than

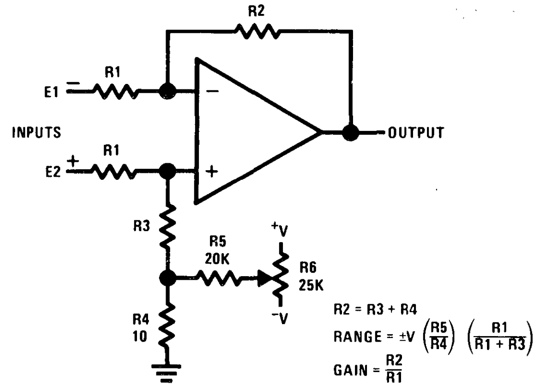


FIGURE 5. Offset Voltage Adjustment for Differential Amplifiers

1 kΩ. If R_3 is less than 1K the shunting of R_4 by R_5 must be considered when choosing the value of R_3.

The techniques described for balancing offset voltage at the input of the amplifier offer two main advantages: First, they are universally applicable to all operational amplifiers and allow device interchangeability with no modifications to the balance circuitry. Second, they permit balancing without interfering with the internal circuitry of the amplifier. The electrical parameters of the amplifiers are tested and guaranteed without balancing. Although it doesn't usually happen, balancing could degrade performance.

January 1970

IC REGULATORS SIMPLIFY POWER SUPPLY DESIGN

Although power supply requirements vary, IC voltage regulators can fulfill the majority of needs. Power supplies designed with ICs can give predictable regulation better than 0.1% with a minimum of engineering effort. Output voltages between 0 and 40V at currents of 10A are easily achieved. Further, with a minimum of changes, a single regulator circuit can be used for a wide variety of output voltages and currents.

A basic 200 mA positive regulator circuit is shown in Figure 1. The LM105[1] contains the voltage reference and control circuitry while the external

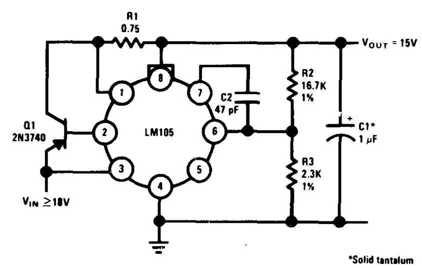


FIGURE 1. 200 mA Positive Regulator

components set the output voltage, current limit and increase power handling capacity of the IC. The output voltage is set by R_2 and R_3. A fraction of the output voltage is compared by an error amplifier with an internal 1.8V reference. Any error is amplified and used to drive the 2N3740 power transistor. Since the open loop gain is large, there is little error and a high degree of regulation.

Current limiting is set by R_1. The voltage drop across R_1 is applied to the emitter base junction of a transistor in the IC. When the transistor is turned on, it removes drive from the series pass transistor; and the regulator output exhibits a constant current characteristic. Since the turn on voltage of a transistor is temperature dependent, so is the current limit. The current limit sense voltage is about 0.4V at 25°C decreasing linearly to 0.3V at 125°C. Therefore, the current limit resistor must be chosen to provide adequate output current at the maximum operating temperature.

To regulate negative voltages, the circuit in Figure 2 is used. An LM104[2] contains the voltage reference and control circuitry while an external

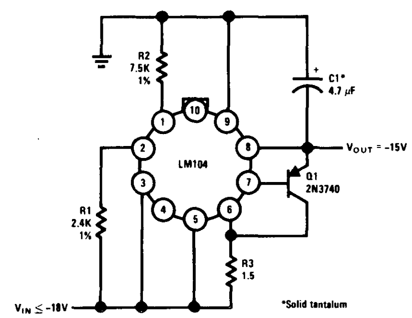


FIGURE 2. 200 mA Negative Regulator

transistor is used to increase the power handling capacity. A reference voltage is generated by driving a constant current, determined by R_1, through R_2. The voltage across this resistor is fed into an error amplifier. The error amplifier controls the output voltage at twice the voltage across R_2. The output voltage is resistor programmable with R_2 and adjustable down to zero.

Current limit in the LM104 is similar to the LM105. Voltage across R_3 turns on an internal transistor that decreases drive to the output transistors. This current limit sense voltage is also temperature dependent, decreasing from 0.65V at 25°C to 0.45V at 125°C.

Boosting the available output current from 200 mA is relatively simple. Figure 3 shows posi-

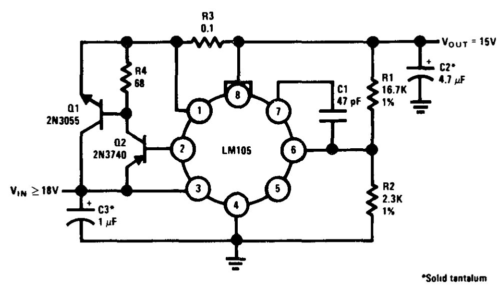


FIGURE 3a. 2A Positive Regulator

tive and negative 2A regulators. An additional power transistor increases the current handling capability of the regulator. Adding the boost tran-

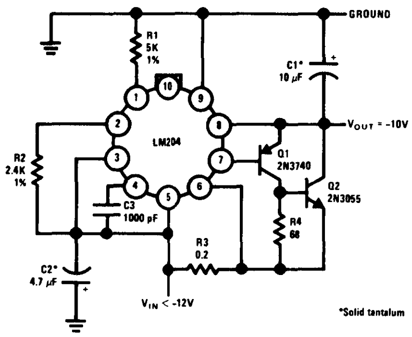


FIGURE 3b. 2A Negative Regulator

sistors increases the output current without increasing the minimum input-output voltage differential. The minimum differential will be 2 to 3V, depending on the drive current required from the integrated circuit and operating temperature. Low input-output voltage differential allows more efficient regulation.

Although the regulators are relatively simple, some precautions must be taken to eliminate possible problems. First, when the regulator is used with boost transistors, a solid tantalum output capacitor is needed. Unlike electrolytics, solid tantalum capacitors have low internal impedance at high frequencies. This suppresses possible high frequency minor loop oscillations as well as providing low output impedance at high frequency. Also, for the LM104, the output capacitor frequency compensates the regulator and must have good frequency characteristics.

The power transistors recommended are single-diffused, wide-base devices. These devices have fewer oscillation problems than double-diffused, planar transistors. Also, they seem less prone to failure under overload conditions. Of course, like the power transistors in any regulator, adequate heat sinking is necessary. The heat sink should keep the transistor junction temperature at an acceptable level for worst case conditions of maximum input voltage, maximum ambient temperature and shorted output. By far, the major cause of regulator failures is inadequate heat sinking.

Good construction techniques are also important for regulator performance. If proper care is not taken, ground loop errors and lead resistance drops can easily become greater than regulator errors. For example, 0.05″ wide, 2 oz. printed circuit conductor has a resistance of about 0.007Ω per inch. For a 200 mA, 15V regulator, ten inches of conductor would decrease the regulation by a factor of 2.

Ground loops are worst yet, since voltage drops can be amplified and appear at the regulator's output. In Figure 3, voltage drops between Pin 4 of the LM105 and the bottom of R_3 are amplified by the ratio of R_2/R_3 and appear at the output.

When the regulator is powered from ac that is rectified and filtered, current flowing in the filter can sometimes cause an unusual ground loop problem. For capacitor input filters, the peak charging current is many times the average load current. Even a few milliohms of resistance can cause appreciable voltage drop during the peak of the charging. When the charging current produces a voltage drop between R_3 and Pin 4 of the LM105, it appears as excessive ripple on the output of the regulator.

Of course, single point grounding eliminates these problems, but this is not always possible. Usually it is sufficient to insure that load current does not generate a voltage drop between the ground side of the voltage setting resistor and the ground of the IC.

In most cases, short circuit protection is the only fault protection needed. However, for some regulator circuits, such as positive and negative regulators used together, additional protection is necessary. If the positive and negative supplies are shorted together, it is possible to cause the output voltage of one of the supplies to reverse, blowing the IC. This is especially true if the current capabilities are different, such as a 200 mA negative supply and a 2A positive supply. A clamp diode between the output and ground of each supply will prevent such polarity reversals. Also, clamp diodes should be used to prevent input polarity reversal and input-output voltage differential reversal.

The use of ICs in regulator circuits can enhance power supply performance while minimizing cost and engineering time. Since only one IC is needed for a wide range of outputs, the part cost, board space and purchasing problems are less when compared to discrete designs. Also engineering time is saved since typical and worst case performance data, as well as application data, is available from the manufacturer before design is begun.

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1. R.J. Widlar, "An Improved Positive Regulator," *National Semiconductor AN-23*, January, 1969.
2. R.J. Widlar, "Designs for Negative Regulators," *National Semiconductor AN-21*, October, 1968.

March 1970

THE LM110—AN IMPROVED IC VOLTAGE FOLLOWER

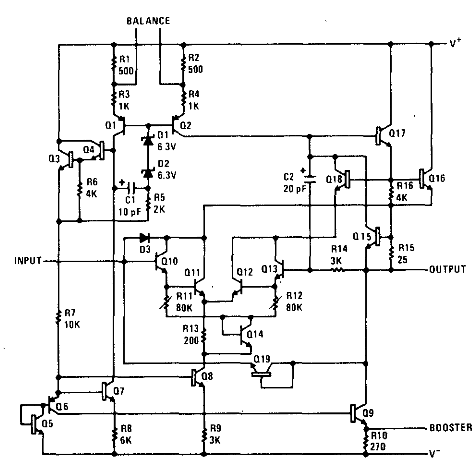
There are quite a few applications where op amps are used as voltage followers. These include sample and hold circuits and active filters as well as general purpose buffers for transducers or other high-impedance signal sources. The general usefulness of such an amplifier is particularly enhanced if it is both fast and has a low input bias current. High speed permits including the buffer in the signal path or within a feedback loop without significantly affecting response or stability. Low input current prevents loading of high impedance sources, which is the reason for using a buffer in the first place.

The LM102, introduced in 1967, was designed specifically as a voltage follower. Therefore, it was possible to optimize performance so that it worked better than general purpose IC amplifiers in this application. This was particularly true with respect to obtaining low input currents along with high-speed operation.

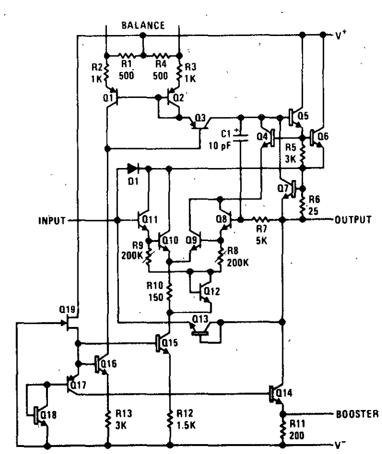
One secret of the LM102's performance is that followers do not require level shifting. Hence, lateral PNP's can be eliminated from the gain path. This has been the most significant limitation on the frequency response of general purpose amplifiers. Secondly, it was the first IC to use super-gain transistors. With these devices, high speed operation can be realized along with low input currents.

The LM110 is a voltage follower that has been designed to supersede the LM102. It is considerably more flexible in its application and offers substantially improved performance. In particular, the LM110 has lower offset-voltage drift, input current and noise. Further, it is faster, less prone to oscillations and operates over a wider range of supply voltages.

The advantages of the LM110 over the LM102 are described by the following curves. Improvements not included are increased output swing under load, larger small-signal bandwidth, and elimination of oscillations with low-impedance sources. The performance of these devices is also compared with general-purpose op amps in Tables I and II. The advantages of optimizing an IC for this particular slot are clearly demonstrated. Lastly, some typical applications for voltage followers with the performance capability of the LM110 are given.

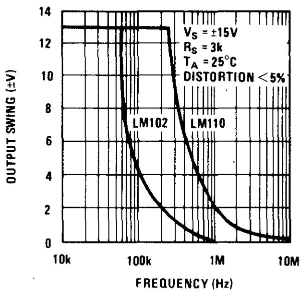


LM102

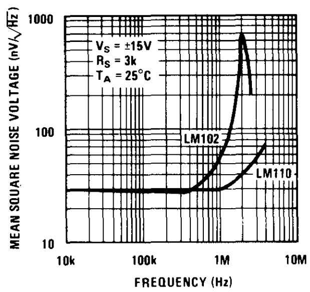


LM110

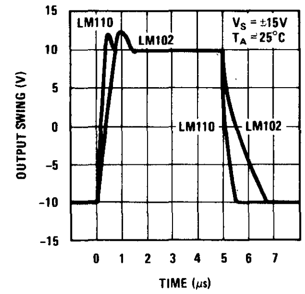
Biggest design difference between the LM102 and LM110 is the elimination of the zener diodes (D1 and D2) in the biasing circuit. This reduces noise and permits operation at low supply voltages.



Power bandwidth of the LM110 is five times larger than the LM102.



Eliminating zeners reduces typical high frequency noise by nearly a factor of 10. Worst case noise is reduced even more. High frequency noise of LM102 has caused problems when it was included inside feedback loop with other IC op amps.



Large signal pulse response shows 40V/μs slew for LM110 and 10V/μs for LM102. Leading edge overshoot on LM110 is virtually eliminated, so external clamp diode frequently required on the LM102 is not needed.

DEVICE	OFFSET** VOLTAGE (mV)	BIAS** CURRENT (nA)	SLEW† RATE (V/μs)	BANDWIDTH† (MHz)	SUPPLY* CURRENT (mA)
LM110	6.0	10	40	20	5.5
LM102	7.5	100	10	10	5.5
MC1556	6.0	30	2.5	1	1.5
μA715	7.5	4000	20	10	7.0
LM108	3.0	3	0.3	1	0.6
LM108A	1.0	3	0.3	1	0.6
LM101A	3.0	100	0.6	1	3.0
μA741	6.0	1500	0.6	1	3.0

**Maximum for $-55°C \leq T_A \leq 125°C$

*Maximum at 25°C

†Typical at 25°C

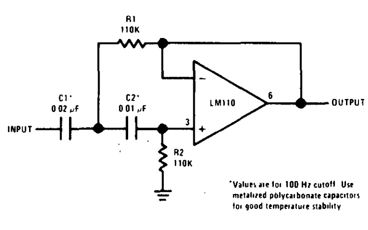
Table I. Comparing Performance of Military Grade IC Op Amps in the Voltage-Follower Connection.

DEVICE	OFFSET* VOLTAGE (mV)	BIAS* CURRENT (nA)	SLEW† RATE (V/μs)	BANDWIDTH† (MHz)	SUPPLY* CURRENT (mA)
LM310	7.5	7.0	40	20	5.5
LM302	15	30	20	10	5.5
MC1456	10	30	2.5	1	1.5
μA715C	7.5	1500	20	10	10
LM308	7.5	7.0	0.3	1	0.8
LM308A	0.5	7.0	0.3	1	0.8
LM301A	7.5	250	0.6	1	3.0
μA741C	6.0	500	0.6	1	3.0

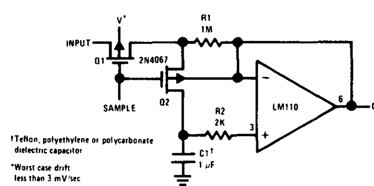
*Maximum at 25°C

†Typical at 25°C

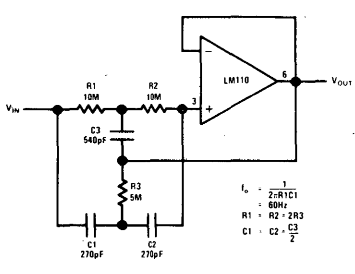
Table II. Comparison of Commercial Grade Devices.



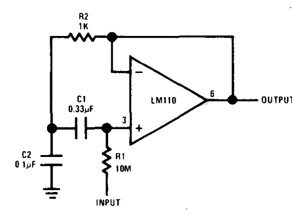
High Pass Active Filter



Low Drift Samp'e and Hold*



High Q Notch Filter



Bandpass Filter

January 1970

AN IC VOLTAGE COMPARATOR FOR HIGH IMPEDANCE CIRCUITRY

The IC voltage comparators available in the past have been designed primarily for low voltage, high speed operation. As a result, these devices have high input error currents, which limit their usefulness in high impedance circuitry. An IC is described here that drastically reduces these error currents, with only a moderate decrease in speed.

This new comparator is considerably more flexible than the older devices. Not only will it drive RTL, DTL and TTL logic; but also it can interface with MOS logic and FET analog switches. It operates from standard ±15V op amp supplies and can switch 50V, 50 mA loads, making it useful as a driver for relays, lamps or light-emitting diodes. A unique output stage enables it to drive loads referred to either supply or ground and provide ground isolation between the comparator inputs and the load.

Another useful feature of the circuit is that it can be powered from a single 5V supply and drive DTL or TTL integrated circuits. This enables the designer to perform linear functions on a digital-circuit card without using extra supplies. It can, for example, be used as a low-level photodiode detector, a zero crossing detector for magnetic transducers, an interface for high-level logic or a precision multivibrator.

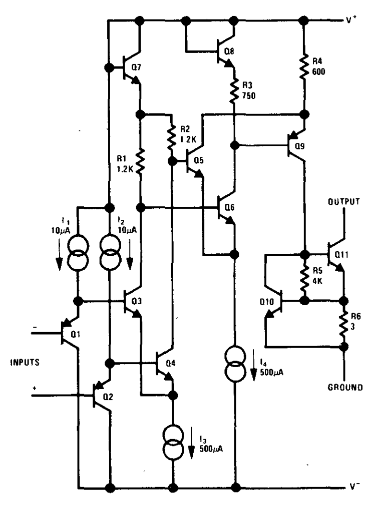


FIGURE 1. Simplified Schematic of the LM111

Figure 1 shows a simplified schematic of this versatile comparator. PNP transistors buffer the differential input stage to get low input currents without sacrificing speed. Because the emitter base breakdown voltage of these PNPs is typically 70V, they can also withstand a large differential input voltage. The PNPs drive a standard differential stage. The output of this stage is further amplified by the Q_5-Q_6 pair. This feeds a lateral PNP, Q_9, that provides additional gain and drives the output stage.

The output transistor is Q_{11} which is driven by the level shifting PNP. Current limiting is provided by R_6 and Q_{10} to protect the circuit from intermittent shorts. Both the output and the ground lead are isolated from other points within the circuit, so either can be used as the output. The V^- terminal can also be tied to ground to run the circuit from a single supply. The comparator will work in any configuration as long as the ground terminal is at a potential somewhere between the supply voltages. The output terminal, however, can go above the positive supply as long as the breakdown voltage of Q_{11} is not exceeded.

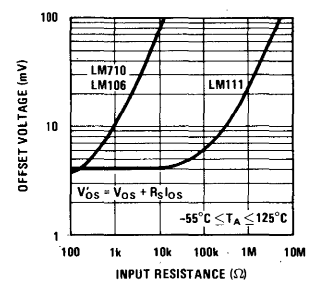


FIGURE 2. Illustrating the Influence of Source Resistance on Worst Case, Equivalent Input Offset Voltage.

Figure 2 shows how the reduced error currents of the LM111 improve circuit performance. With the LM710 or LM106, the offset voltage is degraded for source resistances above 200Ω. The LM111, however, works well with source resistances in excess of 30 kΩ. Figure 2 applies for equal source resistances on the two inputs. If they are unequal, the degradation will become pronounced at lower resistance levels.

Table I gives the important electrical characteristics of the LM111 and compares them with the specifications of older ICs.

A few, typical applications of the LM111 are illustrated in Figure 3. The first is a zero crossing detector driving a MOS analog switch. The ground terminal of the IC is connected to V^-; hence, with ±15V supplies, the signal swing delivered to the gate of Q_1 is also ±15V. This type of circuit is useful where the gain or feedback configuration of

Table I. Comparing the LM111 with earlier IC comparators. Values given are worst case over a –55°C to 125°C temperature range, except as noted.

Parameter	LM111	LM106	LM710	Units
Input Offset Voltage	4	3	3	mV
Input Offset Current	0.02	7	7	μA
Input Bias Current	0.15	45	45	μA
Common Mode Range	±14	±5	±5	V
Differential Input Voltage Range	±30	±5	±5	V
Voltage Gain†	200	40	1.7	V/mV
Response Time†	200	40	40	ns
Output Drive				
Voltage	50	24	2.5	V
Current	50	100	1.6	mA
Fan Out (DTL/TTL)	8	16	1	
Power Consumption	80	145	160	mW

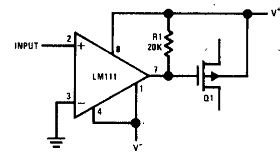
†Typical at 25°C.

an op amp circuit must be changed at some precisely-determined signal level. Incidentally, it is a simple matter to modify the circuit to work with junction FETs.

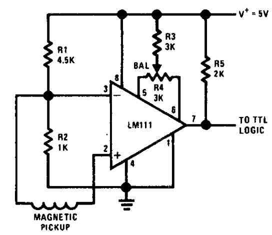
The second circuit is a zero crossing detector for a magnetic pickup such as a magnetometer or shaft-position pickoff. It delivers the output signal directly to DTL or TTL logic circuits and operates from the 5V logic supply. The resistive divider, R_1 and R_2, biases the inputs 0.5V above ground, within the common mode range of the device. An optional offset balancing circuit, R_3 and R_4, is included.

The next circuit shows a comparator for a low-level photodiode operating with MOS logic. The output changes state when the diode current reaches 1 μA. At the switching point, the voltage across the photodiode is nearly zero, so its leakage current does not cause an error. The output switches between ground and –10V, driving the data inputs of MOS logic directly.

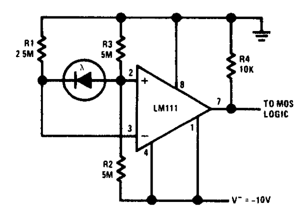
The last circuit shows how a ground-referred load is driven from the ground terminal of the LM111. The input polarity is reversed because the ground terminal is used as the output. An incandescent lamp, which is the load here, has a cold resistance eight times lower than it is during normal operation. This produces a large inrush current, when it is switched on, that can damage the switch. However, the current limiting of the LM111 holds this current to a safe value.



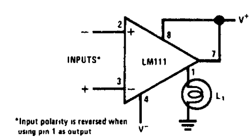
a. Zero Crossing Detector Driving Analog Switch



b. Detector for Magnetic Transducer



c. Comparator for Low Level Photodiode



d. Driving Ground–Referred Load

FIGURE 3. Typical Applications of the LM111.

The applications described above show that the output-circuit flexibility and wide supply-voltage range of the LM111 opens up new fields for IC comparators. Further, its low error currents permit its use in circuits with impedance levels above 1 kΩ. Although slower than older devices, it is more than an order of magnitude faster than op amps used as comparators.

The LM111 has the same pin configuration as the LM710 and LM106. It is interchangeable with these devices in applications where speed is not of prime concern.

November 1970

APPLICATIONS OF THE LM173/LM273/LM373

The LM173 family of multi-mode IF amplifier/detectors has been designed for AM, FM and SSB applications in the communications market. It consists of two amplifier sections, a gain control stage, a fully balanced FM/SSB detector, and an active AM/SSB peak detector whose output matches the AGC input characteristics.

FM OPERATION

Grounding the AGC input, pin 1, closes the switch connecting the quadrature capacitor to the quadrature network terminal pin 6. This network, tuned to the nominal center frequency of the IF strip gives a phase shift that varies with frequency at pin 6 (input A of the quadrature detector) with respect to the signal at input B. This produces a

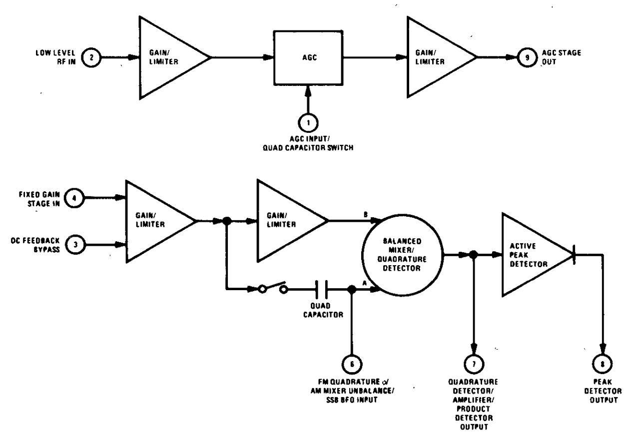


FIGURE 1. Block Diagram of LM173

To convert between modes of operation, one simply makes the appropriate dc connections and takes the recovered signal from the output of the desired detector. Two pins are involved in programming the mode of operation, pin 1 and pin 6. Since AGC is not normally used for FM, grounding pin 1 closes the quad capacitor switch to enable the balanced mixer to function as an FM quadrature detector. Since the balanced mixer is not required for AM, connecting a resistor from pin 6 to ground unbalances the mixer allowing it to pass signal. Also, this transfers the balance sensing circuitry from the input of the balanced mixer in FM (or SSB) mode to the input of the AM detector. For example, FM operation is achieved as shown in Figure 2.

pulse duration modulation of the detector output current which is integrated by the capacitor on pin 7. This capacitor may also be used for de-emphasis. A considerable range for compromise exists in the choice of Q of the quadrature network. Increasing the Q results in greater output level and distortion for a given frequency deviation. Also, the parallel resonant impedance of the network should be such that $\geq$50 mV rms signal appears on the quadrature phase terminal to ensure switching action of the detector and maximum output. An alternate higher level audio signal may be taken from the peak detector output pin 8.

Precise dc balance of input B of the quadrature detector is maintained by an active dc feedback

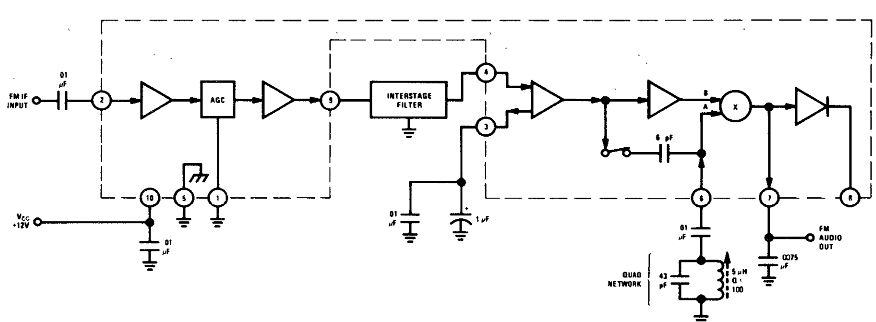


FIGURE 2. FM IF Connection

network. The dc feedback bypass pin must be decoupled at low frequencies to ensure stability of this loop. A 1.0 μF shunted by a .01 μF for good high frequency decoupling is quite adequate. Note that a dc path through the input or interstage filter is not necessary (or desirable).

AM OPERATION

In Figure 3, the LM173 functions as an AM IF amplifier and detector by unbalancing the balanced mixer and connecting the peak detector network to the input of the active peak detector for optimum AM performance. Pin 6 should not be grounded directly or excessive device current drain may result. Lifting the AGC input from ground opens the quad capacitor switch, as described earlier.

An improvement in signal to noise ratio may be obtained when interstage filtering is not used, or is fairly broad, by connecting a parallel resonant circuit in shunt with the signal path at pin 7.

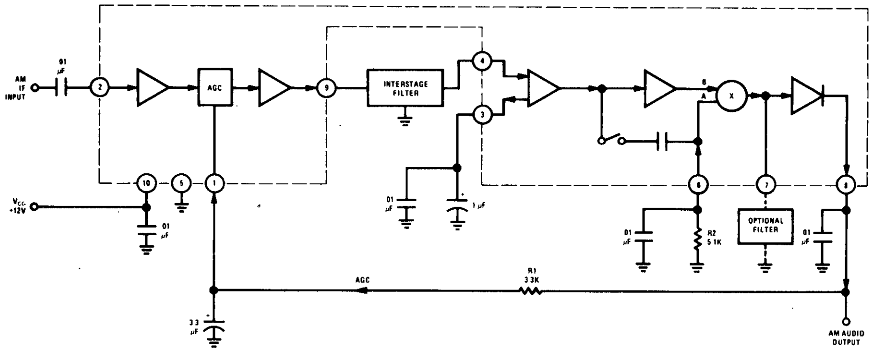


FIGURE 3. AM IF Connection

output to the AGC input through an RC network with a suitable attack/decay time constant. Decreasing the value of R_1 will increase the AGC range of the system at the expense of recovered output level due to the reduced dc drop across R_1. This voltage drop results from the AGC bias current.

The balanced mixer is disabled by applying an offset voltage to input A with resistor R_2 to ground. This also transfers the active dc balance

SSB OPERATION

In single sideband operation, we require both AGC and balanced mixer functions and therefore we do not ground pin 1 or pin 6. By injecting 25 mV rms or greater BFO signal into balanced mixer input A at pin 6, the mixer acts as a product detector, and we obtain our recovered audio at pin 7. The peak detector may then be used to generate an audio derived AGC voltage as shown in Figure 4. The connection of a manual gain control for CW operation is also illustrated.

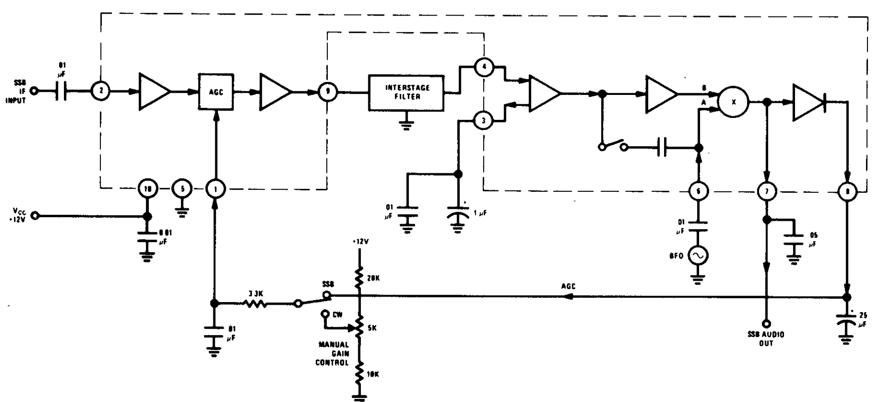


FIGURE 4. SSB and CW IF Connection

November 1970

SPEED UP THE LM108 WITH FEEDFORWARD COMPENSATION

Feedforward frequency compensation of operational amplifiers can provide a significant increase in slew rate and bandwidth over standard lag compensation. When feedforward compensation is applied to the LM101A operational amplifier,[1] an order of magnitude increase in bandwidth results. A simple feedforward network has also been developed for use with the LM108 micropower amplifier to give a factor of five improvement in speed. It uses no active components and does not degrade the excellent dc characteristics of the LM108.

Figure 1 shows a schematic of an LM108 using the new compensation. The signal from the inverting input is fed forward around the input stage by a 500 pF capacitor, C_1. At high frequencies it provides a phase lead. With this lead, overall phase

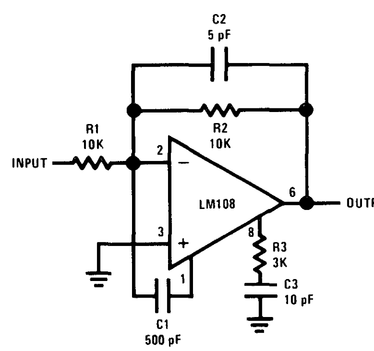


FIGURE 1. LM108 with Feedforward Compensation

shift is reduced and less compensation is needed to keep the amplifier stable. The $C_2 - R_1$ network provides lag compensation, insuring that the open loop gain is below unity before 180° phase shift occurs. The open loop gain and phase as a function of frequency is compared with standard compensation in Figure 2.

The slew rate is increased from 0.3V/μs to about 1.3V/μs and the 1 kHz gain is increased from 500 to 10,000. Small signal bandwidth is extended to 3 MHz. The bandwidth must be limited to 3 MHz because the phase shift through the lateral PNP transistors used in the second stage becomes excessive at higher frequencies. With the LM101A, 10 MHz bandwidth was possible since the signal was bypassed around the low frequency lateral PNP's. Nonetheless, 3 MHz is very respectable for a micropower amplifier drawing only 300 μA quiescent current.

When the LM108 is used with feedforward compensation, it is less tolerant of capacitive loading and stray capacitance. Precautions must be taken

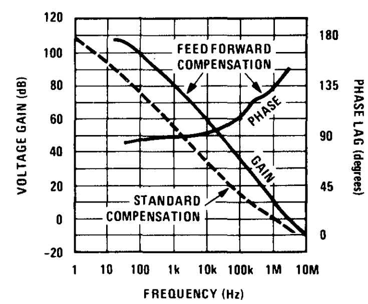


FIGURE 2. Open Loop Voltage Gain

to insure stability. If load capacitance is greater than about 75 to 100 pF, it must be isolated as shown in Figure 3. A small capacitor is always needed to provide a lead across the feedback resistor to compensate for strays at the input. About 3 to 5 pF is the minimum value capacitor. Care must be taken to minimize stray capacitance at Pins 1, 2 and 8 when feedforward compensation is used. Additionally, when the source resistance on the noninverting input is greater than 10k, it should be bypassed with a .01 μF capacitor.

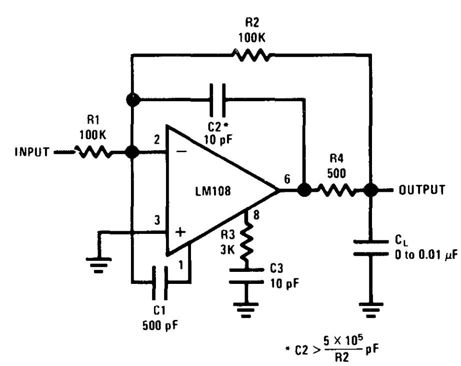


FIGURE 3. Decoupling Load Capacitance

As with any externally compensated amplifier, increasing the compensation of the LM108 increases the stability at the expense of slew and bandwidth. The circuit shown is for the fastest response. Increasing the size of C_2 to 20 or 30 pF will provide 2 or 3 times greater stability and capacitive load tolerance. Therefore, the size of the compensation capacitor should be optimized for the bandwidth of the particular application.

The stability of the LM108 with feedforward compensation is indicated by the small signal transient responses shown in Figure 4. It is quite stable since there is little overshoot and ringing even though the amplifier is loaded with a 50 pF capacitor. Large signal transient response for a 20V square wave is shown in Figure 5. The small positive overshoot is not severe and usually causes no problems.

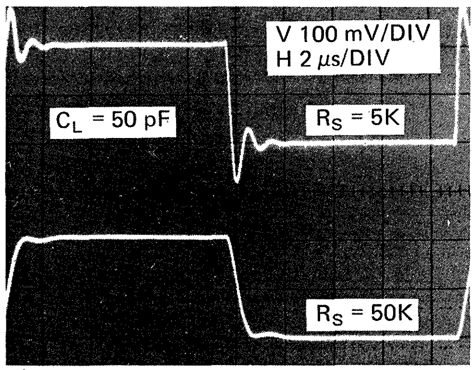


FIGURE 4. Small Signal Transient Response of LM108 with Feedforward Compensation

The LM108 is unusually insensitive to power supply bypassing with the new compensation. Even with several feet of wire between the device and power supply, it does not become unstable. However, it is still wise to bypass the supplies for drill since noise on the V^+ line can be injected to the summing junction by the 500 pF feedforward capacitor.

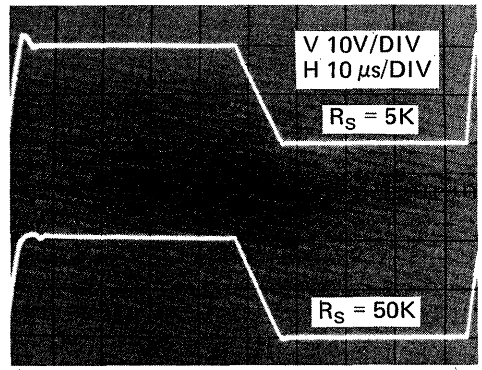


FIGURE 5. Large Signal Transient Response of LM108 with Feedforward Compensation

The new feedforward compensation is easy to use and offers a factor of five improvement over standard compensation. Slew rate is increased to 1.3V/μs and power bandwidth extended to 20 kHz. Also, gain error at high frequencies is reduced. This makes the LM108 more useful in precision applications where low dc error as well as low ac error is desired.

REFERENCE:

1. Robert C. Dobkin, "Feedforward Compensation Speeds Op Amp," *National Semiconductor LB-2,* March, 1969.

January 1971

HIGH STABILITY REGULATORS

Monolithic IC's have greatly simplified the design of general purpose power supplies. With an IC regulator and a few external components 0.1% regulation with 1% stability can be obtained. However, if the application requires better performance, it is advisable to use some other design approach.

Precision regulators can be built using an IC op amp as the control amplifier and a discrete zener as a reference, where the performance is determined by the reference. Figures 1 and 2 show schematics of simple positive and negative regulators. They are capable of providing better than 0.01% regulation for worst case changes of line, load and temperature. Typically, the line rejection is 120 dB to 1 kHz; and the load regulation is better than 10 μV for a 1A change. Temperature is the worst source of error; however, it is possible to achieve less than a 0.01% change in the output voltage over a –55°C to +125°C range.

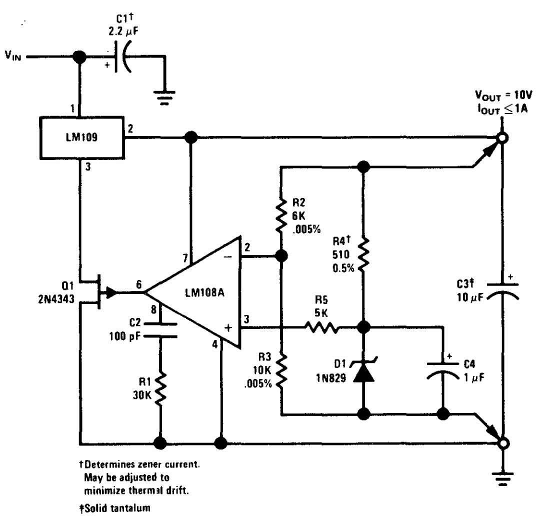


FIGURE 1. High Stability Positive Regulator

The operation of both regulators is straightforward. An internal voltage reference is provided by a high-stability zener diode. The LM108A[1] operational amplifier compares a fraction of the output voltage with reference. In the positive regulator, the output of the op amp controls the ground terminal of an LM109[2] regulator through source follower, Q_1. Frequency compensation for the regulator is provided by both the $R_1 C_2$ combination and output capacitor, C_3.

The negative regulator shown in Figure 2 operates similarly, except that discrete transistors are used for the pass element. A transistor, Q_1, level shifts the output of the LM108 to drive output transistors, Q_3 and Q_4. Current limiting is provided by Q_2. Capacitors C_3 and C_4 frequency compensate the regulator.

In the positive regulator the use of an LM109 instead of discrete power transistors has several advantages. First, the LM109 contains all the biasing and current limit circuitry needed to supply a 1A load. This simplifies the regulator. Second, and probably most important, the LM109 has thermal overload protection, making the regulator virtually burn-out proof. If the power dissipation becomes excessive or if there is inadequate heat sinking, the LM109 will turn off when the chip temperature reaches 175°C, preventing the device from being destroyed. Since no such device is available for use in the negative regulator, the heat sink should be large enough to keep the junction temperature of the pass transistors at an acceptable level for worst case conditions of maximum ambient temperature, maximum input voltage and shorted output.

Although the regulators are relatively simple, some precautions must be taken to eliminate possible problems. A solid tantalum output capacitor must be used. Unlike electrolytics, solid tantalum capacitors have low internal impedance at high frequencies. Low impedance is needed both for frequency compensation and to eliminate possible minor loop oscillations. The power transistor recommended for the negative regulator is a single-diffused wide-base device. This transistor type has fewer oscillation problems than double diffused transistors. Also, it seems less prone to failure under overload conditions.

Some unusual problems are encountered in the construction of a high stability regulator. Component choice is most important since the resistors, amplifier and zener can contribute to temperature drift. Also, good circuit layout is needed to eliminate the effect of lead drops, pickup, and thermal gradients.

The resistors must be low-temperature-coefficient wirewound or precision metal film. Ordinary 1% carbon film, tin oxide or metal film units are not suitable since they may drift as much as 0.5% over temperature. The resistor accuracy need not be 0.005% as shown in the schematic; however, they should track better than 1 ppm/°C. Additionally, wirewound resistors usually have lower thermoelectric effects than film types. The resistor driving

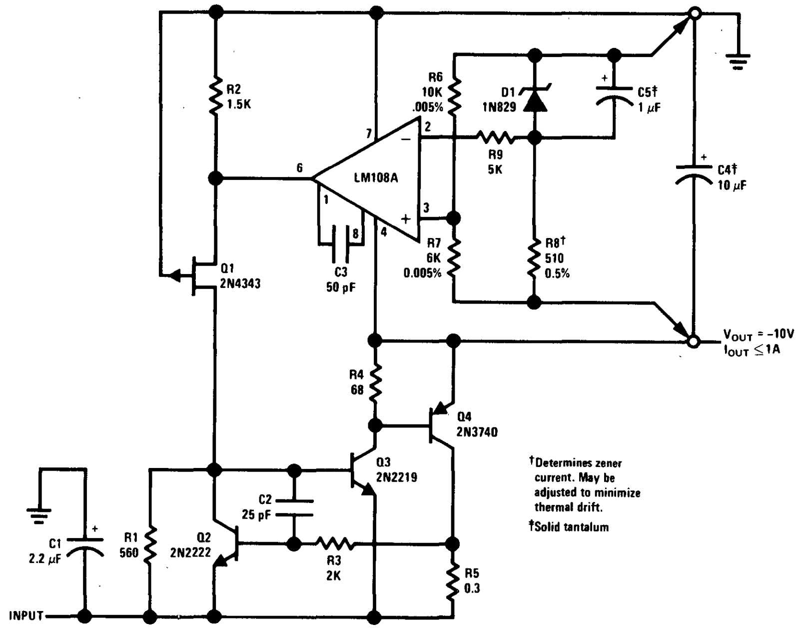


FIGURE 2. High Stability Negative Regulator

the zener is not quite as critical; but it should change less than 0.2% over temperature.

The excellent dc characteristics of the LM108A make it a good choice as the control amplifier. The offset voltage drift of less than 5 μV/°C contributes little error to the regulator output. Low input current allows standard cells to be used for the voltage reference instead of a reference diode. Also the LM108 is easily frequency compensated for regulator applications.

Of course, the most important item is the reference. The IN829 diode is representative of the better zeners available. However, it still has a temperature coefficient of 0.0005%/°C or a maximum drift of 0.05% over a –55°C to 125°C temperature range. The drift of the zener is usually linear with temperature and may be varied by changing the operating current from its nominal value of 7.5 mA. The temperature coefficient changes by about 50 μV/°C for a 15% change in operating current. Therefore, by adjusting the zener current, the temperature drift of the regulator may be minimized.

Good construction techniques are important. It is necessary to use remote sensing at the load, as is shown on the schematics. Even an inch of wire will degrade the load regulation. The voltage setting resistors, zener, and the amplifier should also be shielded. Board leakages or stray capacitance can easily introduce 100 μV of ripple or dc error into the regulator. Generally, short wire length and single-point grounding are helpful in obtaining proper operation.

REFERENCES:

1. R.J. Widlar, "IC Op Amp Beats FETs on Input Current," *National Semiconductor AN-29,* December, 1969.

2. R.J. Widlar, "New Developments in IC Voltage Regulators," in *1970 International Solid-State Circuits Conference Digest of Technical Papers,* Vol. XIII, pp. 158-159.

March 1971

EASILY TUNED SINE WAVE OSCILLATORS

One approach to generating sine waves is to filter a square wave. This leaves only the sine wave fundamental as the output. Since a square wave is easily amplitude stabilized by clipping, the sine wave output is also amplitude stabilized. A clipping oscillator eliminates the problems encountered with agc stablized oscillators such as those using Wein bridges. Additionally, since there is no slow agc loop, the oscillator starts quickly and reaches final amplitude within a few cycles.

amplitude of the square wave fed back to the filter input. Starting is insured by R_6 and C_5 which provide dc negative feedback around the comparator. This keeps the comparator in the active region.

If a lower distortion oscillator is needed, the circuit in Figure 2 can be used. Instead of driving the tuned circuit with a square wave, a symmetrically clipped sine wave is used. The clipped sine wave, of course, has less distortion than a square wave and yields a low distortion output when filtered.

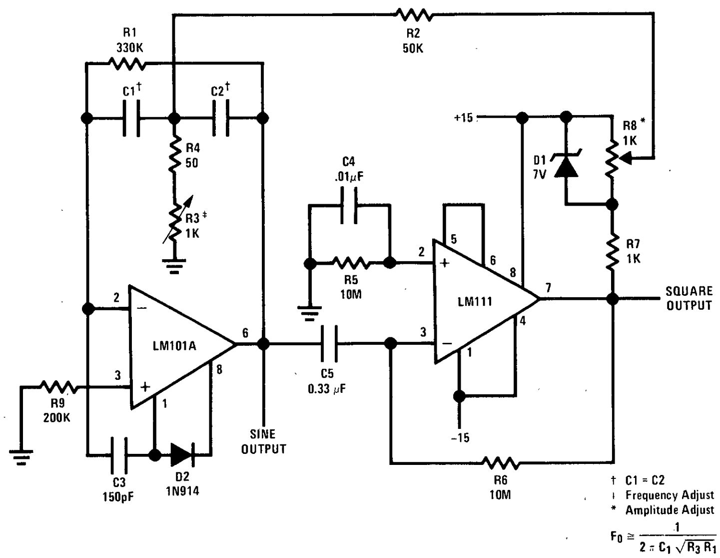


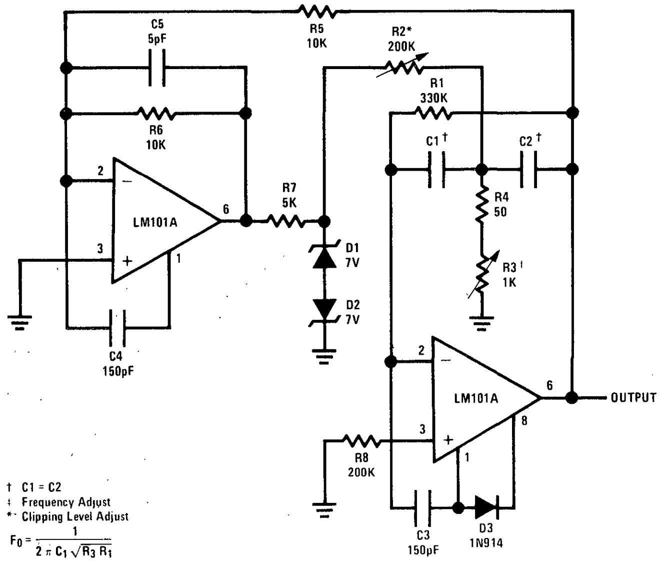
FIGURE 1. Easily Tuned Sine Wave Oscillator

The circuit in Figure 1 will provide both a sine and square wave output for frequencies from below 20 Hz to above 20 kHz. The frequency of oscillation is easily tuned by varying a single resistor. This is a considerable advantage over Wein bridge circuits where two elements must be tuned simultaneously to change frequency. Also, the output amplitude is relatively stable when the frequency is changed.

An operational amplifier is used as a tuned circuit, driven by square wave from a voltage comparator. Frequency is controlled by R_1, R_2, C_1, C_2, and R_3, with R_3 used for tuning. Tuning the filter does not affect its gain or bandwidth so the output amplitude does not change with frequency. A comparator is fed with the sine wave output to obtain a square wave. The square wave is then fed back to the input of the tuned circuit to cause oscillation. Zener diode, D_1, stabilizes the

This circuit is not as tolerant of component values as the one shown in Figure 1. To insure oscillation, it is necessary that sufficient signal is applied to the zeners for clipping to occur. Clipping about 20% of the sine wave is usually a good value. The level of clipping must be high enough to insure oscillation over the entire tuning range. If the clipping is too small, it is possible for the circuit to cease oscillation due to tuning, component aging, or temperature changes. Higher clipping levels increase distortion. As with the circuit in Figure 1, this circuit is self-starting.

Table 1 shows the component values for the various frequency ranges. Distortion from the circuit in Figure 1 ranges between 0.75% and 2% depending on the setting of R_3. Although greater tuning range can be accomplished by increasing the size of R_3 beyond 1kΩ, distortion becomes



$$F_0 = \frac{1}{2\pi C_1 \sqrt{R_3 R_1}}$$

FIGURE 2. Low Distortion Sine Wave Oscillator

excessive. Decreasing R_3 lower than 50Ω can make the filter oscillate by itself. The circuit in Figure 2 varies between 0.2% and 0.4% distortion for 20% clipping.

About 20 kHz is the highest usable frequency for these oscillators. At higher frequencies the tuned circuit is incapable of providing the high Q band-pass characteristic needed to filter the input into a clean sine wave. The low frequency end of oscillation is not limited except by capacitor size.

TABLE 1

C_1, C_2	MIN. FREQUENCY	MAX. FREQUENCY
0.47 μF	18 Hz	80 Hz
0.1 μF	80 Hz	380 Hz
.022 μF	380 Hz	1.7 kHz
.0047 μF	1.7 kHz	8 kHz
.002 μF	4.4 kHz	20 kHz

In both oscillators, feedforward compensation[3] is used on the LM101A amplifiers to increase their bandwidth. Feedforward increases the bandwidth to over 10 MHz and the slew rate to better than 10V/μs. With standard compensation the maximum output frequency would be limited to about 6 kHz.

Although these oscillators are not particularly tricky, good construction techniques are important. Since the amplifiers and the comparators are both wide band devices, proper power supply bypassing is in order. Both the positive and negative supplies should be bypassed with a 0.1μF disc ceramic capacitor. The fast transition at the output of the comparator can be coupled to the sine wave output by stray capacitance, causing spikes on the output. Therefore the output of the comparator with the associated circuitry should be shielded from the inputs of the op amp.

Component choice is also important. Good quality resistors and capacitors must be used to insure temperature stability. Capacitor should be mylar, polycarbonate, or polystyrene – electrolytics will not work. One percent resistors are usually adequate.

The circuits shown provide an easy method of generating a sine wave. The frequency of oscillation can be varied over greater than a 4 to 1 range by changing a single resistor. The ease of tuning as well as the elimination of critical agc loops make these oscillators well suited for high volume production since no component selection is necessary.

References:

1. N.P. Doyle, "Swift, Sure Design of Active Bandpass Filters," *EDN*, Vol. 15, No. 2, January 15, 1970.
2. R.J. Widlar, "Precision IC Comparator Runs from 5V Logic Supply," *National Semiconductor AN-41*, October, 1970.
3. Robert C. Dobkin, "Feedforward Compensation Speeds Op Amp," *National Semiconductor LB-2*, March, 1969.

September 1971

LM118 OP AMP SLEWS 70 V/μs

One of the greatest limitations of today's monolithic op amps is speed. With unity gain frequency compensation, general purpose op amps have 1 MHz bandwidth and 0.3 V/μs slew rate. Optimized compensation as well as feedforward compensation can improve op amp speed for some applications. Specialized devices such as fast, unity-gain buffers are available which provide partial solutions. This paper will describe a new high speed monolithic amplifier that offers an order of magnitude increase in speed with no loss in flexibility over general purpose devices.

The LM118 is constructed by the standard six mask monolithic process and features 15 MHz bandwidth and 70 V/μs slew rate. It operates over a ±5 to ±18V supply range with little change in speed. Additionally, the device has internal unity-gain frequency compensation and needs no external components for operation. However, unlike other internally compensated amplifiers, external feedforward compensation may be added to approximately double the bandwidth and slew rate.

DESIGN CONCEPTS

In general purpose amplifiers the unity-gain bandwidth is limited by the lateral PNP transistors used for level shifting. The response above 2 MHz is so poor that they cannot be used in a feedback amplifier. If the PNP transistors are used for level shifting only at DC or low frequencies and the signal is fed forward around the PNP transistors at high frequencies, wide bandwidth can be obtained without the excessive phase shift of the PNP transistors.

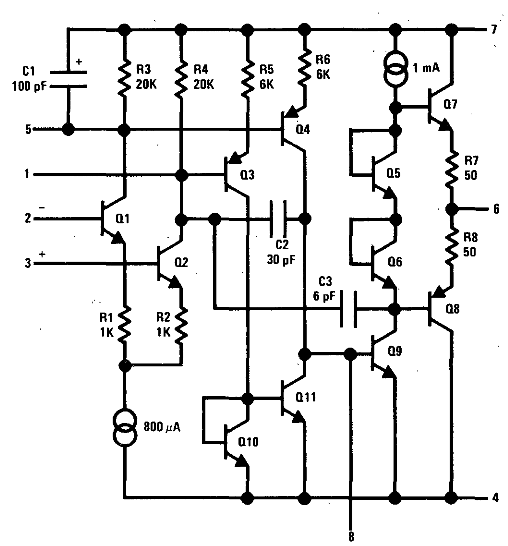


FIGURE 1. Simplified Circuit of the LM118

Figure 1 shows a simplified schematic of the LM118. Transistors Q_1 and Q_2 are a conventional differential input stage with emitter degeneration and resistive collector loads. Q_3 and Q_4 form the second stage which further amplify the signal and level shift the signal towards V^-. The collectors of Q_3 and Q_4 drive a current inverter, Q_{10} and Q_{11} to convert from differential to single ended. Q_9, which has a current source load for high gain, drives a class B output. The collectors of the input stage and the base of Q_9 are available for offset balancing and external compensation.

Frequency compensation is accomplished with three internal capacitors. C_1 rolls off on half the differential input stage so that the high frequency signal path is single-ended. Also, at high frequencies, the signal is fed forward around the lateral PNP transistors by a 30 pF capacitor, C_2. This eliminates the excessive phase shift. Overall frequency response is then set by capacitor, C_3, which rolls off the amplifier at 6 dB/octive. As previously mentioned feedforward compensation for inverting applications can be applied to the base of Q_9. Figure 2 shows the open loop frequency response of an LM118. Table 1 gives typical specifications for the new amplifier.

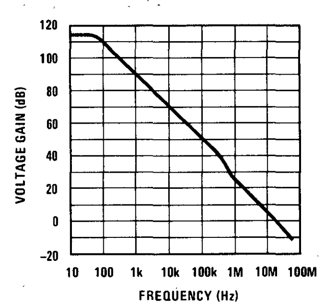


FIGURE 2. Open Loop Voltage Gain as a Function of Frequency for LM118.

TABLE 1. Typical Specifications for the LM118

Input Offset Voltage	2 mV
Input Bias Current	200 nA
Offset Current	20 nA
Voltage Gain	200K
Common Mode Range	±11.5V
Output Voltage Swing	±13V
Small Signal Bandwidth	15 MHz
Slew Rate	70 V/μs

OPERATING CONFIGURATION

Although considerable effort was taken to make the LM118 trouble free, high frequency amplifiers are more prone to oscillations than low frequency devices such as the LM101A. Care must be taken to minimize the stray capacitance at the inverting input and at the output; however the LM118 will drive a 100 pF load. Good power supply bypassing is also in order—0.1 μF disc ceramic capacitors should be used within a few inches of the amplifier. Additionally, a small capacitor is usually necessary across the feedback resistor to compensate for unavoidable stray capacitance.

Figure 3 shows feedforward compensation of the LM118 for fast inverting applications. The signal is fed from the summing junction to the output stage driver by C_1 and R_4. Resistors R_5, R_6 and R_7 have two purposes: they increase the internal operating current of the output stage to increase slew rate and they provide offset balancing. The current boost is necessary to drive internal stray capacitance at the higher slew rate. Mismatch of the external resistors can cause large voltage offsets so offset balancing is necessary. For supply voltages other than ±15V, R_5 and R_6 should be selected to draw about 500 μA from Pins 1 and 5.

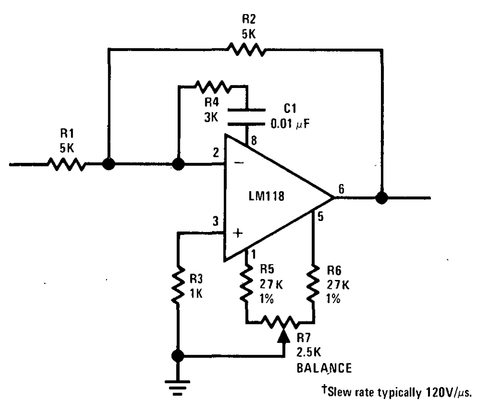


FIGURE 3. Feedforward Compensation for Greater Inverting Slew Rate†

When using feedforward, resistor R_4 should be optimized for the application. It is necessary to have about 8 kΩ in the path from the output of the amplifier through the feedback resistor and through feedforward network to Pin 8 of the device. The series resistance is needed to limit the bandwidth and prevent minor loop oscillation. At high gains, or with high value feedback resistors R_4 can be quite low—but not less than 100Ω. When the LM118 is used a fast integrator, with a large feedback capacitor or with low values of feedback resistance, R_4 must be increased to 8 kΩ to insure stability over a full −55°C to 125°C temperature range.

One of the more important considerations for a high speed amplifier is settling time. Poor settling time can cancel the advantages of having high slew rate and bandwidth. For example—an amplifier can have severe ringing after a step input. A relatively long time is then needed before the output voltage can be read accurately. Settling time is the time necessary for the output to slew through a defined voltage change and settle to within a defined error of its final output voltage. Figure 4 shows optimized compensation for settling to

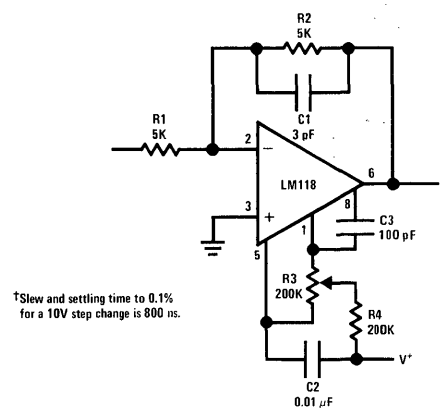


FIGURE 4. Compensation for Minimum Settling† Time

within 0.1% error. Typically the settling time is 800 ns for a simple inverter circuit as shown. Settling time is, of course, subject to operating conditions external to the IC such as closed loop gain, circuit layout, stray capacitance and source resistance. An optional offset balancing circuit, R_3 and R_4 is included.

The LM118 opens up new fields for IC operational amplifiers. It is more than an order of magnitude faster than general purpose amplifiers while retaining the ease of use features. It is ideally suited for analog to digital converters, active filters, sample and hold circuits and wide band amplification. Further, the LM118 has the same pin configuration as the LM101A or LM741 and is interchangeable with these devices when speed is of prime concern.

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